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Abstract—This brief presents an ultralow-voltage multistage rectifier built with standard threshold CMOS for energy-harvesting applications. A threshold-compensated diode (TCD) is developed to minimize the forward voltage drop while maintaining low reverse leakage flow. In addition, an interstage compensation scheme is proposed that enables efficient power conversion at input amplitudes below the diode threshold. The new rectifier also features an inherent temperature and process compensation mechanism, which is achieved by precisely tracking the diode threshold by an auxiliary dummy. Although the design is optimized for an ac input at 13.56 MHz, the presented enhancement techniques are also applicable for low- or ultrahigh-frequency energy scavengers. The rectifier prototype is fabricated in a 0.35-μm four-metal two-poly standard CMOS process with the worst-case threshold voltage of 600 mV/780 mV for nMOS/pMOS, respectively. With a 13.56 MHz input of a 500 mV amplitude, the rectifier is able to deliver more than 35 μW at 2.5 V DD, and the measured deviation in the output voltage is as low as 180 mV over 100 °C for a cascade of ten TCDs.

Index Terms—Energy-harvesting, interstage compensation (ISC), standard threshold CMOS, temperature and process compensation, threshold-compensated diode (TCD), ultralow-voltage rectifier.

I. INTRODUCTION

LIGHT-WEIGHT small-size miniaturized systems, such as passive radio-frequency identification (RFID) tags, wireless distributed sensor networks, and wearable/implantable body area networks (BANs), are getting more and more important in industrial supply chain management, environmental monitoring, and medical/health care support services. However, sustainable and efficient power supply has set up a major challenge in the development of these size-constrained systems, as conventional solutions with onboard battery do not only overburden the device volume and raise the manufacture cost, but also the reduced battery size implies a short device operation time. For example, a 1 cm³ primary lithium battery typically has an energy storage capacity of 2800 J; although this is able to supply a system consuming an electrical power of 100 μW for about one year [1], it is not sufficient for systems, e.g., [2], where device access is prohibited after its initial installation. Therefore, energy-harvesting techniques, by means of which the surrounding environment is exploited as the energy source and the system functionality can be self-sustained for the full device lifetime, have been widely investigated.

Energy automation can be provided by scavenging of mechanical vibrations or reception of radio-frequency (RF) radiation. Although the selection of the energy source ultimately depends on its application, the output from the transducer presents to be diminutive ac power. Thus, the development of a highly efficient ac–dc converter appears to be the key for energy-harvesting systems, as any loss in the power interface directly translates to a reduction in the available power for the system functionality. Moreover, unlike traditional sources, the ac voltage generated by the transducer can be very small. This has addressed an even greater challenge in the rectifier design, as for conventional diode-based structures, the threshold voltage does not only set up a bottleneck in voltage conversion efficiency (VCE) and power conversion efficiency (PCE) but also establishes a fundamental limit for the minimum input that can be possibly rectified. In addition, design difficulty also originates from the stringent temperature stress, to which the energy harvester may be exposed. For example, an environmental monitor may experience a temperature variation from −40 °C to +60 °C. This necessitates not only the design of functional blocks that can operate over a wide temperature range but also a robust power interface, since both the diode threshold voltage and the ON-resistance depend on the temperature.

Up to date, a variety of ac–dc converters has been investigated. Efficient power rectification has been published for active approaches by [3] and [4]. However, the application of these active solutions is limited to low-frequency transducers, as the power dissipation on the active control circuitry significantly raises with frequency. For energy harvesters that may interface with RF radiation, passive rectifiers dominate in the published designs. A gate cross-coupled rectifier [5] was proposed to reduce the dropout voltage, and the threshold cancellation techniques are further developed to boost the efficiency [6], [7]. In order to lower the minimum input threshold for the passive rectifier, native transistors with low threshold are widely utilized. However, the reverse leakage current in these devices is high, and the performance improvement is at the cost of more process steps. Nevertheless, even with native transistors, efficient power rectification below the device threshold has not been reported.
In this brief, we focus on the design of an ultralow-voltage rectifier for RF-powered wireless systems. The proposed rectifier is able to efficiently operate at low subthreshold input levels and features an implicit temperature and process compensation mechanism. The rest of this brief is organized as follows: The analysis and design of the threshold-compensated diode (TCD) is presented in Section II, and Section III describes the principle of the proposed voltage multiplier. Measurement results are discussed in Section IV, and this brief is concluded in Section V.

II. ANALYSIS AND DESIGN OF THE THRESHOLD-COMPENSATED PASSIVE DIODE

The diode serves as the fundamental building block for passive rectifiers of all kinds. As the technology we are using offers devices only with standard threshold, ultralow-voltage operation is only possible with TCDs. If a TCD is considered in a half-wave rectifier (see Fig. 1), the gate bias voltage is preferably the same as the diode threshold, as the static voltage conversion equation [6] implies

\[ V_{DD} = V_{RF} - |V_T| + V_B, \quad V_B \leq |V_T| \]  

and general opinion acquiesces the maximum output voltage produces the best efficiency (In (1), \( V_{RF} \) describes the ac input amplitude, \( V_T \) is the diode threshold, and \( V_B \) is the gate bias voltage.). However, as we scale down to the micropower generation regime, this empirical speculation must be reconsidered, because as we compensate for the threshold dropout in the forward direction, the reverse leakage current will increase as well. For energy-harvesting devices that only output a few microwatts in power, a leakage current in the microampere range is detrimental enough to destroy the performance. Therefore, in this brief, a two-port model is used for an ideal TCD, and the different gate bias voltages are analyzed in terms of \( V_{CE} \) and PCE. It should be noted that as we alter the threshold compensation, the diode will work at different regions. Thus, the analytical derivation of the \( ON \)-resistance, conduction angle, reverse leakage, etc., for individual situations will lead to a too complicated procedure, and simulation-based analysis should be performed.

The proposed model of the nMOS TCD (n-TCD) is schematically shown in Fig. 2(a). Transistor \( M_{N1} \) serves as the main rectifying diode, and voltage source \( V_{BN} \) describes the threshold compensation that pulls up the gate potential of \( M_{N1} \) by a constant dc offset. In order to avoid latch-up problems, an isolated nMOS transistor is employed for \( M_{N1} \) (isolated nMOS within a separated p-well within a deep n-well within the p-substrate), and the bulk regulation technique [5] is utilized for the isolated wells. This is achieved by auxiliary switching transistors \( M_{N2} \) and \( M_{N3} \) for the p-well and \( M_{P1} \) and \( M_{P2} \) for the deep n-well, respectively.

The VCE and PCE of the half-wave rectifier are simulated at an input frequency of 13.56 MHz and an amplitude of 500 mV. A load resistor of 50 k\( \Omega \) is used in the simulation. As shown in Fig. 3, both VCE and PCE substantially increase compared with the conventional uncompensated diode (\( V_{BN} = 0 \)), and the variation of VCE features a monotonous increase with \( V_{BN} \), whereas PCE features a peak value at approximately 425 mV and a sharp rolloff afterward. The drop in PCE at a large gate bias voltage results from the reverse leakage charge, and a further breakdown into the power consumption reveals that the diode occupies only 17% of the total input power during the negative phase at \( V_{BN} = 425 \) mV, whereas this number dramatically increases to 40% at \( V_{BN} = 500 \) mV.

The different behavior of VCE and PCE can be understood as follows: For VCE, as long as the ON/OFF current ratio keeps on increasing as we scale up \( V_{BN} \), the charges being transferred in the forward direction will outnumber these being transferred backward that still yields an increase in the output voltage. However, the power consumed by the leakage charges is becoming more and more essential in PCE, not only due to the increasing value in the leakage current but also because \( M_{N1} \) stays in the reverse region for a longer time and \( V_{DS} \) across \( M_{N1} \) becomes larger. Therefore, for ultralow-power converters,
conventional designs based on a voltage-optimized strategy are no longer valid, since as we adopt the compensation voltage the same as the diode threshold, PCE would drop by approximately 25%. The tradeoff between VCE and PCE can be balanced at a VIN value that is slightly greater than the power optimum (depicted in dark gray in Fig. 3), as the variation in this area for both curves is low.

For the sizing of the diode transistor, special consideration also needs to be taken. Unlike conventional ac–dc converters where W/L is set large to minimize the overdrive related voltage drop, small transistors are preferred in energy-harvesting devices. This is because of the following reasons: 1) In an ultralow-power regime, the dc current delivered by the rectifier is typically small, resulting in a minor influence of the overdrive related dropout; and 2) a large aspect ratio introduces not only increased area consumption but also high parasitic losses and a large reverse leakage current.

To complete the analysis, a pMOS TCD (p-TCD) has been also investigated. Using the model depicted in Fig. 2(b), which is composed of a threshold-compensated pMOS diode with bulk regulation for the n-well, similar results are derived from simulation, and the optimum VBP is at 525 mV.

In order to understand the circuit implementation for the TCD, a Greinacher doubler is employed [see Fig. 4(a)], which also serves as the unit cell in the proposed voltage multiplier, as is shown later. Fig. 4(b) provides the schematic of the rectifier, where, for simplicity, all bulk regulation transistors from Fig. 2 are omitted. For the n-TCD side, an isolated nMOS diode is added to main device MN with its source connected to the anode and the drain to the gate. The threshold compensation voltage is presented by the VDS of MBN. Serial resistor RBP serves as the biasing, and the desired compensation voltage can be achieved by scaling the current feeding through MBN. With an expected R-variation of ±20%, only a -7 mV/+8 mV deviation in VIN is shown from its desired value. In addition, the power overhead imposed by this auxiliary circuit is negligible, because the desired bias stays below the diode threshold and the resistance of RBP is typically large. In addition, due to the large RBP, the circuit stability is improved as the variation in VDD induced by the input alternation will mostly drop over this resistor. A decoupling capacitor CBP is included to reduce the ac input that couples through the CGS of MN. The same topology is adopted to realize the p-TCD, and only MBP is implemented by a pMOS transistor.

An added advantage of this topology is an inherent temperature and process compensation mechanism, which is achieved by the auxiliary bias transistors. As MBN and MBP are selected to match the main diodes, they automatically track the threshold drift in MN and MP. Although the thermal stress and the process corners on the bias resistor will introduce a slight variation in VIN, the generated gate bias voltage still closely follows the deviations in the main devices. This compensation scheme is particularly interesting for energy-harvesting devices, as with a low output current, the deviation in the output voltage over temperature and process is dominated by the threshold.

III. PROPOSED ULTRALOW-VOLTAGE RECTIFIER

The development of an energy harvester commonly requires a CMOS-compatible output voltage in the range of 2–3 V. With input amplitudes around 500 mV, a voltage multiplier must be used. Fig. 5 shows a conventional n-stage rectifier based on the Dickson charge pump, and it can be understood as a cascade of n unit cells of the Greinacher doubler [see Fig. 4(a)]. Detailed analysis of the Dickson multiplier can be found in [8], and the static voltage conversion equation is given as

\[ V_{DD} = 2n \cdot \frac{C}{C + C_{\text{para}}} \cdot V_{RF} - 2n \cdot V_D = \frac{2n \cdot I}{C \cdot f} \]  

(2)

assuming all capacitors share the same capacitance C, and C\text{para} describes the parasitic capacitance at the input node of each stage, VD is the diode voltage drop, I is the loading current, and f is the input frequency.

To implement the multistage rectifier, the circuit shown in Fig. 4(b) could be used as the unit cell. However, when the input signal shrinks toward the diode threshold, the start-up of the rectifier becomes difficult. This is because by simply cascading the Greinacher topology [see Fig. 4(b)], the correct initialization of threshold compensation will depend on the sufficient dc voltage at the output of the respective stage. However, with input signals in the subthreshold region, the generated dc voltage of a single stage will be smaller than the required gate bias for effective compensation. This situation

![Fig. 4. Greinacher doubler. (a) Circuit configuration. (b) Schematic for TCD implementation.](image1)

![Fig. 5. Multistage rectifier based on Dickson topology (i, n > 1, integer).](image2)
will be even worse if the resistive current source is taken into consideration.

Therefore, in this work, an interstage compensation (ISC) scheme is proposed, and the circuit schematic is shown in Fig. 6. The idea of ISC is based on decoupling of the threshold compensation generation from the single-stage output and exploiting the maximum and minimum supply in the multiplier, so that even with a limited voltage gain per stage, the optimum bias can be still realized. More specifically, for the \( i \)th stage, transistors \( M_{NI,P1} \) and \( M_{BN,BP_i} \) are functionally the same as these in the Greinacher rectifier; however, unlike the connection depicted in Fig. 4(b), bias resistors \( R_{BN_i} \) and \( R_{BP_i} \) are now being tied to the overall generated \( V_{DD} \) and \( V_{SS} \), instead of the output \( V_{2i} \) and \( V_{2i−2} \) from the \( i \)th stage. In doing so, the voltage available for threshold compensation in the \( i \)th stage will increase from \( V_{2i} − V_{2i−2} \) for both diodes to \( V_{DD} − V_{2i−2} \) for the \( n \)-TCD and \( V_{2i} − V_{SS} \) for the \( p \)-TCD, respectively. Due to this improvement, the desired compensation can be generated with a smaller input, and the VCE of a single stage can be enhanced as well.

Further simulation on a four-stage voltage multiplier proves this argument. With a 13.56 MHz input of a 500 mV amplitude and a load resistor of 500 kΩ, the desired 425 mV/525 mV \( V_{BN}/V_{BP} \) can be generated for almost all TCDs in the ISC-based structure (the only exceptions are the pMOS diode \( M_{P1} \) in the first stage with approximately 450 mV \( V_{BP} \) and the nMOS diode \( M_{N4} \) in the last stage with 400 mV \( V_{BN} \)). As compared with 317 mV/372 mV \( V_{BN}/V_{BP} \), which could be obtained without ISC by using each single-stage output for threshold compensation, the improvement with ISC is up to 34% and 41%. Hence, the added effect of all diodes ensures the rectifier having efficient operation at this low input amplitude, as 2.2 V \( V_{DD} \) is achieved by the proposed structure, and only 1.63 V is obtained by the standard one without ISC. It should be noted that by the ISC approach, the voltage across different compensation branches will significantly differ. Thus, bias resistor \( R_{BN_i}/R_{BP_i} \) requires being individually adjusted to achieve the desired bias condition. For this purpose, the available voltage for threshold compensation is first estimated by simulation using the ideal TCD model (see Fig. 2) for each biasing branch, and dc analysis is then applied for the resistor in scaling its resistance.

IV. RESULTS AND DISCUSSIONS

The proposed rectifier is fabricated in a 0.35-μm four-metal two-poly standard CMOS process with typical and worst-case threshold voltages of 500 mV/−680 mV and 600 mV/−780 mV for nMOS/pMOS, respectively. A five-stage multiplier is designed in order to generate a minimum dc output voltage of 2.5 V from the specified input of 500 mV. In addition, all capacitors were sized 80 pF in order to balance the tradeoff between conversion efficiency and silicon area. For testing purposes on this prototype, all flying capacitors were implemented off-chip.

The measured output voltage of the multiplier is plotted against the input amplitude in Fig. 7. With a capacitive load of 1 nF, the voltage conversion starts from approximately 200 mV, and at 350 mV, the rectifier is able to generate 1 V dc. In addition, the operation of the rectifier features two phases: Below 400 mV, the initialization of threshold compensation is in progress, and the raise in the output voltage attributes not only to the increase in the input but also to better threshold compensation due to the proposed ISC. Beyond 400 mV, the TCD is well in working order, and the conversion curve appears to be flattened, which is dominated only by input \( V_{RF} \). With a 220 kΩ load resistor, a similar trend can be observed: only rectification starts at an elevated level.

In order to evaluate the effectiveness of ISC, a similarly sized multistage rectifier using the TCD in Fig. 4(b) without ISC is simulated, and the result is also shown in Fig. 7. As shown, the proposed rectifier with ISC starts efficient rectification at a lower input level, and this is attributed to the enlarged compensation headroom, as discussed in Section III.

The performance of the rectifier is further investigated in terms of resistive loads (see Fig. 8). The rectified voltage decreases with decreasing resistance. In addition, below
The output power of the rectifier is also plotted in Fig. 8. The maximum output power is found at \( R_L = 150 \, \text{k}\Omega \) with 36.3 \( \mu \text{W} \) and 2.34 V \( V_{DD} \). By using a load resistor of 180 k\( \Omega \), the rectifier is able to provide a dc voltage above 2.5 V with an output power of 35.8 \( \mu \text{W} \); there, the simulated PCE is 37.8\%. (Only the simulation result is shown here for PCE.) Since the proposed voltage multiplier is composed of five single-stage Greinacher doubler built with standard CMOS diodes is simulated, but due to its incapability to operate at ultralow voltage, the input amplitude is more than tripled to 1.8 V, which provides a comparable \( V_{DD} \) at 2.7 V. As shown in Fig. 9, by a thermal stress from \(-40^\circ \text{C}\) to \(+60^\circ \text{C}\) (temperature range limited by the specified operation condition of the supply cable), the maximum output deviation for the proposed rectifier is measured to be 5.6\% among five devices under test (DUTs). Since the proposed voltage multiplier is composed of five Greinacher stages with ten diodes, the equivalent sensitivity for a single-stage rectifier would be as low as 1.12\%. In comparison to 26\% of the standard uncompensated rectifier, the improvement is by a factor of 20.

The different polarity in the temperature coefficient is easily understood: For the proposed rectifier, the output drift is mainly caused by the variation in the carrier mobility, which features a negative coefficient with temperature. However, for the standard uncompensated rectifier, the threshold voltage dominates in the output deviation; hence, a positive coefficient results.

V. CONCLUSION

In this brief, the design of an ultralow-voltage rectifier in standard threshold CMOS has been presented. With voltage- and power-optimized threshold-compensated diodes and an ISC scheme, the proposed rectifier is able to generate a 2.5 V supply from a 13.56 MHz input of a 500 mV amplitude while delivering more than 35 \( \mu \text{W} \) with 37.8\% PCE. The presented rectifier also features an inherent temperature and process compensation mechanism, which improves the circuit stability in terms of the static dc output voltage by a factor of 20. In addition, the proposed topology can be redesigned to use arbitrarily low or high generator frequencies as it does not employ any active switching and the minimum input can be enhanced to a lower level by using low-threshold devices. Therefore, it is greatly advantageous for energy harvesters that interface with small ac magnitudes at variable environmental conditions.

REFERENCES