A Low-Power RF Front-End of Passive UHF RFID Transponders

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Abstract—This paper presents in details the architecture and most of RF front-end building blocks of a fully integrated passive radio frequency identification (RFID) transponder operating at UHF 902MHz to 928MHz. A novel architecture for the transponder IC and a new low power on-off keying (OOK) demodulator are proposed in this paper. For realizing the system, a low power CMOS full-wave rectifier achieving a power conversion efficiency of 31.9% has been integrated in this transponder. Simulation results show that the global input power of front-end circuits is only about 21µw in order to drive a load of 1.8µA at the rectifier output and the power consumption of the proposed demodulator is less than 0.4µw. The transponder is fabricated in a 0.18µm mixed-mode CMOS technology and has the area of 0.70 mm².

I. INTRODUCTION

In recent years automatic identification procedures (Auto-ID) have become very popular in many applications, such as service industries, purchasing and distribution logistics, transportation management, security, inventory tracking and supply chain management [1]. RFID tags can be classified into active tag, semi-passive tag and passive tag, depending on their source of electrical power [2]. Considering the advantages in terms of low cost, small size and long operation lifetime, etc, passive tag is a good choice for RFID application. Without battery as power supply, low-power operation is a challenge faced in passive RFID tag design.

In order to achieve a low power operation, many technologies, such as SOI [3], SOS [4], organic TFT technology [5], and CMOS [2], [6], [7], have been selected for RFID transponder fabrication. Except for the traditional architecture [6], an architecture used in a a long-range telemetry device, incorporating an on-chip ADC, and employing active telemetry for data transmission is proposed for transponder implementation [8]. Moreover, studies about rectifier design methodology are very popular recently. Analysis, modeling and design strategy of UHF rectifier [9], [10] and Voltage Multiplier [11] and design criteria for UHF passive RFID transponder [11] are reported in recent years. And some innovations about rectifier, such as voltage threshold cancellation in rectifier [2], rectifier with dynamic gate-drain biasing [7], also have been proposed to improve communication range.

Figure 1. (a)Block diagram of the proposed architecture, (b)Diagram of communication session.
presents the architecture of the transponder. Section III details most of the building blocks of transponder. And, Section IV describes simulation result. Conclusion is given in Section V.

II. TRANSPONDER ARCHITECTURE

The block diagram of the transponder is shown in Fig. 1. Transponder retrieves its energy stored in a storage capacitor by rectifying the incoming electromagnetic RF signal. Rectifier supplies power for analog front-end circuits, digital baseband processor and memory. And OOK demodulator demodulates the input OOK modulated signal. Then the clock generator generates clock Clk and clock Clk_D which is about 1µs delay to the clock Clk, by delaying the demodulated signal Dem. These two clocks are needed for digital baseband processing. Furthermore, by delaying clock Clk_D, modulator generates a modulated signal Mo and a signal Mo,CLK. Signal Mo is used to switch the modulated transistor, and signal Mo,CLK is used to disable the clock generator circuit to avoid regenerating clock during the return link backscatter modulation. If enough energy powers up the transponder, the power-on-reset circuit generates a signal POR to reset the registers of the digital baseband processor and memory.

III. TRANSPONDER BUILDING BLOCKS

A. Full-wave AC/DC rectifier

Typical AC/DC Rectifier circuit architecture used in common is composed of N-stage capacitor-diode network [6]. Owing to low series resistance, little threshold voltage, and low junction capacitance, Silicon-Titanium Schottky diodes are generally used in AC/DC rectifier [6]. However, the particularity of processes for Schottky diodes and the inconsistency in quality between different processes often make the integration of Schottky rectifier incompatible with standard CMOS circuits and then handicap its application. So, various junction diodes, such as diode-connected MOS FETs [2], [4], [7], instead of the Schottky diodes are used in rectifier.

The schematic of full-wave AC/DC rectifier is shown in Fig.2. The rectifier is composed by a three stages cascade full-wave voltage doubler. Diode-connected ultra low threshold voltage transistors whose I-V characteristics are shown in Fig.3 are used to rectify the RF signal instead of Schottky diode. To the same output voltage, the number of stage of full-wave voltage doubler is usually less than that of half-wave voltage doubler. Moreover, the less stages, the more power efficiency of rectifier [11], [13]. So, cascade full-wave voltage doubler is expected to achieve higher power efficiency at the cost of needing a differential structure for the other blocks [4].

In order to avoid a high DC voltage at the rectifier output in the near field, a voltage limiter is needed.

B. Demodulator

The demodulator consists of the detector which uses one stage voltage doubler as envelope detector, a comparator and converter shown in Fig. 4. The diodes in the detector are realized by diode-connected transistor with ultra low threshold voltage. The demodulating process is fulfilled by comparison with signal Vdp and signal Vdn. Signal Vdp is the output of the detector and signal Vdn derives from the voltage of the second negative stage of rectifier as the

![Figure 2. Full-wave MOS AC/DC rectifier circuit](image)

![Figure 3. The I-V characteristic of the diode-connected ultra low threshold transistor.](image)

![Figure 4. Demodulator circuit](image)
From the I-V characteristic shown in Fig. 3, there is about 5µA reverse current through the diode-connected ultra low threshold transistor. When the unmodulated RF signal input, the detector serves as a rectifier, and during the modulated stage, this detector is equivalent to a low pass filter, C_s discharges through transistors M7 and M8 by their reverse current. Due to the capacitance of C_s is only one tenth of that of C_C, the ripple voltage of V_dn is much smaller than that of V_dp.

As for this demodulator only one stage of detector has been used, so the power consumption is relatively small. Considering the low bit rate of the input signal, the transient current of the comparator is set to only 120 nA. In order to increase the drive strength of the output demodulated signal, a converter is added at the output of the comparator.

C. Delay element

Fig. 5 shows the schematics of the delay elements. The terminals V_N is connected to the output of the voltage reference circuit. Thus the currents in the transistors M_n1 is constant.

As for the delay element, when the input is low, the transistor M_n2 turns off, so the output is high and there are no charges on capacitor C_1 and C_2. At the start of the rising edge of input signal, node A discharges via the constant current I_d provided by M_n1. Thus the voltage on node A decreases. Once the voltage on node A decrease to the threshold of the subsequent inverter made up by transistor M_p2 and M_n3, the output OUT reverses to low immediately, then the node A also turns to low for the positive feedback of capacitor C_2. And the discharging process stops. During this discharging process, the change of charge on the node A is (C_1+C_2)(V_C - V_inv,th). The delay time T_dr can be roughly calculated by the following equation:

\[ T_{dr} = (C_1 + C_2)(V_C - V_{inv,th}) / I_d \]  

Where V_{inv,th} is the threshold voltage of the inverter made up by M_p2 and M_n3, and I_d is the drain current of the transistor M_n1.

D. Power on reset (POR)

The power-on-reset circuit shown in Fig. 6 is composed of a delay element and a converter. The delay element delays the rising edge of the output voltage of rectifier as indicated in Fig. 1(b). In order to ensure the reliability of the reset function, the delay time is set to be no less than 50µs.

E. Clock Generator

The block diagram of clock generator is shown in Fig. 7 (a). Through the simple logic circuits, clock Clk is obtained from the Dem signal, whose rising edge is delayed about 7 µs. Another clock Clk_D whose rising edge is delayed 1 µs from that of clock Clk may be obtained by the same circuit with different component parameters. The signal Mo_Clk controls the operation of the clock generator. When Mo_Clk is low, clock generator is enabled and generates two clocks for digital circuits, and when Mo_Clk is high during the return link backscatter modulation process, the clock generator circuit turns off avoiding clock regeneration and malfunction of digital circuits.

F. Modulator

The block diagram of modulator is shown in Fig. 7 (b). The input signal Dex controls whether delay clock Clk_D to generate two signals for modulation. The backscatter modulator is divided into two separate delay paths composed by several delay elements with different timing parameters. One of the delay paths generates signal Mo which switches the modulated transistor to perform backscatter modulation, the other delay path generates signal Mo_Clk serving as enabling signal for clock generator which has been described above. In the delay path relating Mo signal, the rising edge of clock Clk_D has been delayed about 7 µs, and then the second delay element delays 1µs again. Through a NOR gate, these two delayed signal with two different delay time is synthesized to a pulse whose width is 1µs. The signal

Figure 5. Delay element circuit

Figure 6. POR (Power on reset) circuit using the delay element

Figure 7. (a) Clock generator circuit using the delay element, (b) Modulator circuit using the delay element
Mo_Clk generation is the same as signal Mo, but the delay parameter of the relevant two delay elements are different in order to ensure that the pulse of Mo is in the middle of the pulse of Mo_Clk, which controls clock generator operation.

The system requirements about the delay time of the Mo signal with respect to the signal Dem is from 8 µs to 20 µs. The typical delay time of this design is about 14 µs.

IV. IMPLEMENTATION AND SIMULATION RESULTS

The transponder has been fabricated in a 0.18µm CMOS process. Connect all the relevant building blocks as Fig. 1(a) shown and perform a system simulation. The result as shown in Fig. 8 indicates that the front-end of transponder is functionally correct, the timing performance of demodulated signal Dem and clock Clk_D, Mo and Mo_Clk meet the systematic requirement. Furthermore, in order to obtain 1.8V power supply, an OOK modulated RF signal with amplitude of 380mv and about 21µW input power is enough.

TABLE I. POWER CONSUMPTION OF RECTIFIER

<table>
<thead>
<tr>
<th>Input Power</th>
<th>Output Power</th>
<th>Power efficiency</th>
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<tbody>
<tr>
<td>21.07µW</td>
<td>6.72µW</td>
<td>31.9%</td>
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TABLE II. POWER CONSUMPTION OF OTHER CIRCUITS

<table>
<thead>
<tr>
<th>Demodulator</th>
<th>Bias</th>
<th>Other circuits</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Static</td>
</tr>
<tr>
<td>0.38µW</td>
<td>0.22µW</td>
<td>0.14µW</td>
</tr>
</tbody>
</table>

Figures 8 (a) and (b) show the system simulation result (a) Rectifier output, (b) the output of modulator, clock generator and demodulator.

REFERENCES