Abstract — An IC\textsuperscript{1} for consumer electronics TV sets performing 100 Hz interlaced / 60 Hz progressive scan rate conversion has been designed. Picture-in-picture, split screen and picture improvement capabilities are also integrated. It applies a motion-compensating algorithm for high-quality scan rate conversion. PIP processing is performed using a full frame based scan rate conversion method. Split screen and multi-picture applications with two asynchronous input sources are supported. All field memories are included using a high performance embedded DRAM technology. Therefore the IC, which is compatible with current TV concepts, meets economical demands with increased functionality.

1. INTRODUCTION

Increased demands on video image quality in consumer TV sets result in higher complexity of video signal processing algorithms. Nevertheless the success on market highly depends on the costs of the ICs. A system on silicon solution, however, like the here described IC combines low cost and high quality processing.

A today’s high end TV set as illustrated in figure 1 comprises color decoding and A/D converter ICs for main and second channel. Additional ICs perform scan rate conversion including motion estimation, picture scaling, picture improvement and enhancement, Picture-in-Picture processing, D/A conversion and RGB and Deflection processing. External field memory chip sets are necessary to fulfil the demands of the high performance scan rate conversion, motion estimation and picture enhancement techniques. In fact this configuration is used only for high-end TV sets due to the high cost for the whole chip sets. Therefore the demand for an integration of the above mentioned chip sets is very high. The existing IC presented in this paper includes all digital processing elements like scan rate conversion, motion estimation, picture improvement and enhancement, PIP-processing, D/A conversion and field memories. Figure 2 shows the new digital TV system configuration using the described IC. It can be used within numerous other system configurations, whenever digital scan rate conversion has to be performed.

\textsuperscript{1} The IC is available commercially as SDA9410
- High performance 3-D-predictive motion estimation
- Special scan rate conversion for film mode
- Frame based scan rate conversion for slave channel
- Split screen (Double window) display of two independent sources (SSC operation mode)
- Manifold configurations of multi picture displays (MUP operation mode)
- Flexible horizontal (step size of 4 pixels) and vertical scaling (step size of one line) of both input channels, vertical peaking
- 3-D spatial-temporal noise reduction picture enhancement technique for master channel
- Automatic detection of letter box formats
- Digital luminance and chrominance transition improvement (DLTI, DCTI), horizontal peaking, YUV 8:8:8 interpolation
- Three high quality 9bit D/A converters
- 6Mbit eDRAM memory on-chip with flexible data configuration for displaying various output combinations of master and slave channel
- Additional on-chip eDRAM and SRAM for storing vector information, conversions and line memories
- Flexible clock and synchronization concept

The following chapters describe the facilities of the operation modes in more detail.

2.1. SRC mode
In the SRC mode the IC supports a high performance motion compensation scan rate conversion. It bases on a 3-D predictive motion estimation. The conversion is performed from 50 Hz interlaced to 100 Hz interlaced or from 60 Hz interlaced to 60 Hz progressive. This kind of algorithm preserves a continuous motion portrayal from the input material at the output side. Especially for the 50 Hz interlaced to 100 Hz interlaced conversion for every two incoming fields two additional fields are generated considering the correct motion phases located in between the original phases. The motion estimation block supplies motion vectors, which enable an exact calculation of the two missing motion phases (vector based motion compensation). The existing IC supports the scan rate conversion for camera mode sources (recorded with an interlaced camera and broadcast as interlaced signal) as well as for film mode material (recorded with a progressive camera and broadcast as an interlaced signal). The technical details especially for the conversion from 60 Hz interlaced film mode (NTSC 2-3 pull down) to 60 Hz progressive output signals are explained in more detail in section 3.

Figure 3: Functional block diagram of the IC

Figure 4: SRC mode with PIP
Additionally, a high resolution joint line free PIP insertion of a second asynchronous channel is possible (on a joint line free display the slave channel is synchronized also vertically to the main channel.) The advantage compared to conventional 100 Hz PIP displays is the really frame based independent conversion of the slave picture. An example configuration is illustrated in figure 4.

2.2. SSC mode
In the SSC mode the two asynchronous input signals can be displayed in any size and at any position. In this case field based scan rate conversion methods are allowed due to the different organization of the internal memory. Figure 5 displays a typical application of the SSC mode. The picture sizes of the two channels are free programmable using a high performance vertical and horizontal scaler. In fact the flexible architecture of the scaler in the input processing stages allows a continuous zoom adjustment of the input picture size down to 1/32x1/32 of the input picture size. Figure 6 illustrates a typical zoom in / zoom out animation.

2.3. MUP mode
In the MUP mode a maximum of two live input signal sources and a multitude of additional still pictures can be displayed. Figure 7 shows a typical configuration. Due to the scalability of the picture sizes the user of the IC can generate his own preferred multi-picture application.

3. TECHNICAL DESCRIPTION
The new chip combines well known picture processing with newly developed high performance algorithms. The following chapters describe the most important algorithms. For better understanding figure 3 can be used as thread.

3.1. Vertical And Horizontal Scaling
The flexible scaling algorithm enables a continuous picture scaling including horizontal panorama mode. Picture sizes down-to 1/32x1/32 of the original size are possible. The
chip consists of two identical scaling units. This allows an independent compression or expansion for the master and the slave channel. Each scaling unit consists of two separate blocks for horizontal and vertical scaling. The vertical scaling enables a compression of the input picture. It is split into three subblocks, a continuous scaler, a vertical peaking and a final decimation unit. Figure 8 demonstrates the basic processing flow.

First a continuous scaler is used to compress the input picture in vertical direction between factor 1 to \( \frac{1}{2} \) (in steps of \( \frac{1}{512} \)). After the continuous filter processing, a vertical high pass filter (peaking) is implemented to improve the picture sharpness. Finally a decimation block compresses the picture with the factor \( \frac{1}{N} \) with \( N \in \{1, 2, 4, 8, 16\} \). The combination enables a continuous compression of the input picture in steps of one line. The horizontal scaling principle is similar. The input signal is interpolated with factor 2. This allows also expansion of the input signal up to the doubled original horizontal size. A second continuous scaler is used to compress the input picture between the factors 1 and \( \frac{1}{2} \) (in steps of \( \frac{1}{2048} \)). Finally a second decimation block compresses the picture horizontally using the factor \( \frac{1}{N} \) with \( N \in \{1, 2, 4, 8, 16\} \). The combination allows a continuous compression of the input picture in steps of two pixels. In addition nonlinear compression facilities (panorama mode) are supported. The combination of both scaler circuits enable the possibility of a continuous zoom feature. The picture can be scaled down to the size of \( \frac{1}{32} \times \frac{1}{32} \) in small horizontal and vertical steps.

3.2. Spatial and Temporal Noise Reduction
The master channel 3-D-noise reduction comprises two stages. The first stage is a detail preserving spatial filter with low hardware expense. It consists of an image analyzing highpass filter bank and an adaptive lowpass FIR-filter for spatial noise reduction [1]. The second stage is a flexible adjustable motion adaptive temporal noise reduction filter. It uses independent motion detectors for luminance and chrominance [2]. Consequently blurring artifacts in the chrominance signal are suppressed.

3.3. Noise Measurement
Two different noise measurement algorithms are implemented to enable an automatic adjustment of the temporal noise reduction filter. The first one measures the noise during the vertical blanking period, the second one in the active image area. The result is a noise level value which can be tested using the IC bus. The setting of the coefficients of the noise reduction filter is done by the external microcontroller.

3.4. Letterbox Detection
On wide screen 16:9-displays the representation of letterbox sources can be optimized by adapting the horizontal and vertical picture size. Normally the user must switch manually to a special zoom mode. The letterbox detection circuit detects the upper and lower border of the letterbox picture. These values can be read from IC bus by the external microcontroller, which adjusts the vertical zooming and the horizontal decimation to get the best screen utilization.

3.5. Main Memory
The employment of an embedded DRAM for data storage simplifies the design of an application board considerably. On the one hand the external memory devices are saved, on the other hand the IC gets a smaller package with a reduced number of pins. On-chip it is advantageous to enlarge the width of the memory data busses to increase the memory bandwidth and to enable the definition of additional input and output data ports. The implemented eDRAM consists of 24 identical 256 bit cores, which are combined to one module equipped with separate input and output data busses having a width of 128 bit. In SRC mode the capacity enables the storage of two full-scale fields of the master channel and three decimated fields of the slave channel for the insertion of a PIP (maximum \( \frac{1}{9} \) of the original size). The data configuration is programmable. In SSC mode for both channels two down scaled fields can be stored. It is taken care that soft transitions between several display configurations without visible artifacts are possible to achieve the above mentioned animations.
The internal memory controller manages all data transfers. For each input and output port small buffer stages are integrated to interface the memory busses and the connected processing circuits. The buffers also transfer the data to the required clock domain. The controller watches the states of the different buffers and establishes priorities for the memory accesses depending on the requirements of the periphery.

The eDRAM solution (figure 9) enables high internal data rates and the possibility of using only one memory for the realization of a multitude of features resulting in a very cost-effective integration.

3.6. 3-D-predictive motion estimation

The performance of the motion compensated scan rate conversion highly depends on the reliability of the motion vectors. For the calculation of a high quality vector field a 3D-predictive motion estimation is used. The algorithm bases on the modified parallel-predictive block matching [4]. It belongs to the advanced block matching category. Looking at non-predictive block matching algorithms like a full search the result is the best match between two blocks at variable positions in a search area. Every block is estimated separately. The main disadvantage is the low correlation to the motion trajectory in the incoming field sequence. Other non predictive algorithms exist with similar behavior. This category of algorithms is suitable e.g. for MPEG2 applications to reconstruct original fields but not for scan rate conversion to calculate new intermediate fields. Vectors with wrong motion information can cause extremely strong visible artifacts.

For scan rate conversion predictive algorithms are preferred. They use the vector information of previously calculated blocks in advance to calculate the motion vector for the actual block. The source vectors are taken from the same temporal plane (spatial) and the previous temporal plane (temporal) and used as prediction. Combinations of these predictors and the zero-vector build a set of candidate vectors for the actual block. The block positions pointed to by these candidates are now evaluated by comparison criteria. The best match is chosen and its assigned vector is taken as predictor for the next blocks and for use in the scan rate conversion.

In this chip a 3-D-predictive algorithm is implemented. Its key features applied to a frame resolution picture are listed in Table 1.

| Block size (pixels x pixels) | 8 x 8 |
| Wide block size | 8 x 16 |
| Maximum horizontal vector length | −32/+31 |
| Maximum vertical vector length | −24/+23 |
| Estimation data preprocessing | Raster adaptive, Prefiltering |
| Convergence directions | 2, horizontal and vertical |
| Candidates | 2x spatial |
| | 2x temporal |
| | 2x spatial+update |
| | 1x null vector |
| Number of update vectors | 17, pseudo random selection |
| Block matching criteria | Summed Absolute Difference |
| Block subsampling | 2x horizontal |
| | 2x vertical quincunx |
| Iterations per input field | 2 (interlaced) |
| | 1 (progressive) |
| Iterations per block line | 1 (interlaced) |
| | 2 (progressive) |
| Block line processing | Meandering |
| Movie mode detection | True motion on PAL |
| | Smooth motion on NTSC |

Table 1: Motion estimation feature list

The block size is 8 by 8 pixels. Two blocks are compared using the Summed Absolute Difference (SAD) criteria. The absolute difference between the blocks is summed pixel by pixel. To decrease the data rate a horizontal and vertical subsampling is performed. The result is modified by some penalty values which depend on the candidate and resulting vector behavior. If all candidates are rated the best match of each of the two convergence directions is determined. These two intermediate results are stored and used again as predictors for the following blocks. Additionally a decision is made which of these two vectors is qualified for the resulting vector. Each block of a block line is processed in the described way. Reaching the end of a block line two different possibilities occur: on progressive mode the block line is processed a second time before jumping to the next line. In interlaced mode this jump is executed directly. In this case
the processing starts at the last block and ends at the first block of the line. This proceeding is called meandering block line processing and is visualized in figure 10 [3]. For interlaced mode it is possible to estimate the whole field a second time before starting with new field information. This iterative procedure speeds up the convergence rate.

A very important part of the motion estimation circuit is the film (or movie) mode detection, which switches between different processing variants in the scan rate conversion. The different film mode options are explained in chapter 3.8.

3.7. Vector memory

The estimated vectors are stored in a separate vector memory, which is implemented as a 128 kbit eDRAM. The capacity is up to 96 blocks/line x 72 block lines = 6912 vectors. The vector memory block includes an additional vector processing which improves the precision of the actual vector information. A block erosion circuit maps the block based vector information to the pixel based calculation in the scan rate conversion without creating blocking artifacts.

3.7.1 High performance scan rate conversion for master channel

Dependent on the application mode the master channel scan rate conversion uses the vector information to perform motion compensation (SRC mode). SSC and MUP mode apply non motion compensating algorithms[4, 5, 6]. In SRC mode at first a “virtual” progressive frame is calculated. Then a vertical decimation is performed. It is possible to generate interlace as well as progressive display formats with this circuit. Another advantage is the combination of the scan rate conversion with a vertical expansion of the picture (supported factors 1.0…2.0 in 64 steps). The virtual progressive frame ensures a high quality picture expansion because of the increased vertical resolution.

Figure 10: Meandering block line processing

Figure 10: Output sequence generation modes in scan rate conversion
To generate an output sequence with a good motion portrayal the estimated vectors and the actual film mode information are used. Dependent on the film mode different output sequences are generated. The standard mode is camera mode. In this mode the input source provides a new motion phase on every field.

The two other modes are called film modes. They arise from scanning cinematic source material for which only 24 frames per second are available. For film mode material scanned for 50Hz standards always two successive fields have the same motion phase. The film source is reproduced with 25Hz and each image is scanned twice to get an interlaced video signal. On NTSC film mode the 24 frames are scanned using the 2:3-pulldown method resulting in sequences, which contain alternating two and three successive fields with the same motion phase. In figure 10 the three modes are illustrated for a one-dimensional motion.

The aim on motion compensation is to create an output field or frame sequence, which has a good motion portrayal. In figure 11 the ideal motion portrayal is displayed as a dashed line. The output motion (solid line) should approach this ideal case. The deviation is marked as shadowed area.

On camera mode no motion blurring occurs on source material (1: square curve). A simple non motion compensated scan rate converter repeats previous motion phases and causes a motion blurring on 100/120Hz output dependent on motion speed (1: triangle curve). With motion compensation (1: rhomb curve) intermediate motion phases are calculated and the ideal curve is obtained, no motion blurring occurs.

A 50 Hz film mode input sequence already shows a motion blur (2: square curve). This artifact increases on higher velocities. Motion compensation techniques can reduce this effect under a visible threshold. Now the deviation from the ideal curve is minimized (2: rhomb curve). The result is an output motion portrayal, which is visibly smoother compared with the original input sequence.

A 60Hz input field sequence has motion artifacts on higher velocities (3: square curve) like the 50 Hz film mode but the blur is much more irregular caused by the 2:3 pull-down. The preferred application in this case is a 60Hz progressive conversion. Here also the motion portrayal can be improved by creating new motion phases (3: circle curve). Also this conversion results in an clearly improved motion portrayal.

The generation of the output picture is performed by median filter techniques. In SSC and MUP mode the motion compensation is disabled. Simple display techniques like interlaced AABB or progressive A+A’, B’+B are used instead.

### 3.8. Slave Channel Processing

The data processing of the slave channel scan rate conversion depends on the operation mode. In SRC mode a fully frame based joint line free PIP display can be created. The SSC and MUP mode enable larger picture sizes or multiple still pictures. As in master channel simple conversion techniques are used. These modes guarantee the same picture quality for master and slave channel.

### 3.9. Master And Slave Channel Multiplexing

The pictures of master and slave channel can be positioned independently. So picture-in-picture, picture-outside-picture, split screen (double window) or multi-picture displays can be created in various ways. The positioning is adjustable at every field, which enables a multitude of animations (e.g. exchanging master and slave channel, TV channel selection on multi picture displays or a fade out after turning off the TV set.

### 3.10. Display Processing

After mixing master and slave channel final image improvements are performed. A luminance peaking filter improves the over all frequency response of the luminance channel [7] resulting in a better picture sharpness. The peaking algorithm consists of programmable high and band pass filters working in parallel. The following stage applies a new digital algorithm to improve horizontal transitions of the luminance and chrominance signals (DLTI, DCTI). A correction signal proportional to the shape of the detected horizontal transition is added to the original input signal. Before D/A conversion the signal is interpolated from YUV 4:2:2 to YUV 8:8:8 format. The triple D/A converter stage supplies Y, -(R-Y) and -(B-Y) signals. Each converter comprises 9 bit amplitude resolution, a maximum clock frequency of 60MHz and a two-fold oversampling.

### 4. ARCHITECTURE

The economical implementation of the algorithms described above on a single IC including the necessary field and line memories requires an embedded DRAM technology. The key characteristics are listed in Table 2.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35 μm embedded DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor count</td>
<td>10,000,000</td>
</tr>
<tr>
<td>Data clock</td>
<td>13.5 MHz / 27 MHz</td>
</tr>
<tr>
<td>Dissipation</td>
<td>&lt; 2 W</td>
</tr>
<tr>
<td>Package</td>
<td>P-MQFP 100</td>
</tr>
</tbody>
</table>

*Table 2: Key characteristics of the new IC*
The field and line memories are realized with embedded DRAM cores. Two different sizes are implemented, a 128 kbit and a 256 kbit core size. These cores can be combined to create one big memory. In addition some buffers are realized using SRAMs. Table 3 lists all memory on-chip.

<table>
<thead>
<tr>
<th>Memory function</th>
<th>Size</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field memories for master and slave channel</td>
<td>24 x 256 kbit</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Line memories for vertical scaling and spatial noise reduction</td>
<td>2 x 128 kbit</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Line to Block memory for conversion from line based to block based processing</td>
<td>2 x 256 kbit</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Block to Line memory for conversion from block based to line based processing</td>
<td>1 x 256 kbit</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Vector memory for storage of estimated motion vectors</td>
<td>1 x 128 kbit</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Buffer for motion estimation and scan rate conversion</td>
<td>12 x 3 kbit</td>
<td>SRAM</td>
</tr>
<tr>
<td>Buffer for main memory</td>
<td>2.5 kbit</td>
<td>SRAM</td>
</tr>
</tbody>
</table>

Table 3: On-chip memories

5. CONCLUSION

Due to increased need for cost effective functionality and performance in the high end consumer TV market this new system-on-silicon IC has been designed. The 0.35µm DRAM process enables the integration of all field and line memories in combination with the logical elements needed for data processing. The high quality algorithms for motion estimation and motion-compensated scan rate conversion supply an output display without motion blurring artifacts. Clearly visible improvements also on cinematic sources are achieved. The display can be interlaced or progressive. The IC comprises fully frame based joint line free picture-in-picture facilities. Split screen applications with two life pictures are possible as well as any multi-picture displays. The flexible scaling algorithms combined with various positioning possibilities enable countless display configurations. The picture improvement units, motion adaptive spatial-temporal noise reduction, peaking, luminance and chrominance transient improvement are implemented as well as automatic letter box detection and automatic noise measurement. The IC also contains three D/A converters to provide the display units directly with analog signals.

This new system-on-silicon IC has high quality and high performance but only low system cost. It is the first product on the way to a fully integrated high performance flicker free TV single-chip solution.

6. REFERENCES


Markus Schu was born in St.Wendel, Germany, on May 14, 1967. He received the M.Sc. degree from University of Saarland in 1992. In June 1992 he joined the Panasonic European Research and Development Center. In July 1995 he joined the Siemens AG, Semiconductor Group, in Munich, now Infineon Technologies. There he has been working in the field of scan rate conversion, noise reduction, image enhancement, motion detection, motion estimation, letter box detection and sample rate conversion. He was the responsible concept manager for the described IC. Actual he is acting as Concept Manager for the Infineon MEGAVISION® Products.

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