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Design and Control of a Buck–Boost Charger-Discharger for DC-Bus Regulation in Microgrids

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Abstract: In DC and hybrid microgrids (MG), the DC-bus regulation using Energy Storage Devices (ESD) is important for the stable operation of both the generators and loads. There are multiple commercial voltage levels for both ESD and DC-bus; therefore, the ESD voltage may be higher, equal or lower than the DC-bus voltage depending on the application. Moreover, most of the ESD converter controllers are linear-based, hence they ensure stability in a limited operation range. This paper proposes a system to regulate the DC-bus voltage of an MG accounting for any voltage relation between the ESD and the DC-bus voltage. The proposed system is formed by an ESD connected to a DC-bus through a bidirectional Buck–Boost converter, which is regulated by a Sliding-Mode Controller (SMC) to ensure the system stability in the entire operation range. The SMC drives the Buck–Boost charger–discharger to regulate the DC-bus voltage, at the desired reference value, by charging or discharging the ESD. This paper also provides detailed procedures to design the parameters of both the SMC and the charger–dischager. Finally, simulation and experimental results validate the proposed solution and illustrate its performance.

Keywords: DC-bus; voltage regulation; energy storage device; buck–boost; sliding-mode controller

1. Introduction

The participation of renewable energy generators in the electricity market has significantly increased during the last years. They provide around 27% of the global electricity consumption [1], where two of the main renewable generation technologies are wind turbines (WT) and photovoltaic (PV) generators. It is expected that those two technologies produce around 30% of the power generated in 2040 [1].

The power profiles produced by PV generators and WT depend on the environmental conditions (irradiance, wind speed and temperature), which are difficult to predict and may be intermittent [2,3]. Therefore, the use of these renewable generators require, at least, one Energy Storage Device (ESD) to guarantee a stable energy supply to the load when the renewable energy source is not enough, or even when it is not present [3,4].

There are different ESD technologies according to the form of the energy stored: chemical (e.g., batteries), electrical (e.g., supercapacitors and superconducting magnetic storage) and

mechanical (e.g., flywheels and compressed air) [5,6]. In recent literature, there is an increasing interest on supercapacitors [7,8] and hybrid energy storage systems formed by both batteries and supercapacitors [9–11]. Nevertheless, among the ESD technologies, batteries are the most widely used due to its modularity, flexibility and high storage capacity [5,6].

The generators (renewable and conventional) and ESDs must be coordinated in order to supply the energy required by the load with reliability, quality and low cost. This is the main objective of the microgrids (MGs), which can be defined as low voltage distribution networks formed by energetic resources (i.e., distributed generators and ESD) and a control systems to supply the energy requirements of a given application [12,13]. The MG concept can be applied to different scenarios ranging from homes [14,15] or buildings [2,3] to communities [16]. Moreover, MGs can be classified according to the voltage output of its energetic resources as DC [17,18], AC [13] and hybrid [19,20]. Although AC MGs are more common, due to their similarity with the actual grid, DC MGs have recently gained interest due to the penetration of DC generators and loads, like electric vehicles [2]. Hybrid MGs are aimed to combine the benefits of both AC and DC MGs [16].

The regulation of the DC-bus is a determinant for a stable and reliable operation of both DC and hybrid MGs [18,19,21]. Such a regulation is performed by balancing the power produced by the generators and the power consumed by the load. The difference between the power consumed and generated is supplied or stored by the ESD through a bidirectional DC/DC converter. Hence, the bidirectional DC/DC converter fulfills two main tasks: first, managing the charging/discharging of the ESD; second, coupling ESD and DC-bus voltage levels, which are different in most of the cases [21].

The ESD voltage is usually lower than the DC-bus voltage [8,22–25]; thus, a bidirectional step-up converter, like the Boost [8,22,23,26–30] or Buck–Boost (operated as Boost) [24,25], are widely used in literature to couple the ESD to the DC-bus. However, the ESD voltage could change significantly depending on the state-of-charge; thus, the ESD voltage may be higher, equal to or lower than the DC-bus voltage depending on the load conditions [31,32]. Therefore, the authors of [31,32] use bidirectional step-up/down converters to provide a safe connection between the ESD and the DC-bus.

The converters mentioned before are typically controlled using linear techniques to regulate the DC-bus voltage. Some authors propose the use of cascaded controllers to regulate the power delivered or stored in the ESD: on one hand, the cascaded controllers presented in [16,23–25] propose an inner loop to control the ESD current and an outer loop to regulate the DC-bus voltage; on the other hand, the cascaded control introduced in [27] implements an inner loop to control the ESD voltage, while the outer loop regulates the ESD power. Other authors propose linear controllers with a single loop to regulate the DC-bus voltage [22,26]; or two independent linear controllers, one for the discharging process and another one for the charging process [25,29]. This last approach is based on the different dynamics exhibited by the converter in both the discharging (Boost operation) and charging (Buck operation) processes.

Nevertheless, linear controllers are designed from small-signal models linearized around particular operating points, i.e., given input and output voltages and currents. However, the charging/discharging processes of the ESD forces the DC/DC converter to work in a wider range of operating points, which may be far from the small signal region in which the linear controller is designed. Therefore, the performance and stability of those controllers cannot be guaranteed throughout the operating range of the system formed by both the ESD and the DC/DC converter. To overcome this problem, some authors developed nonlinear controllers with wider stability ranges, e.g., the Sliding-Mode Controllers (SMC) reported in [8,30,33] and the Active Disturbance Rejection Controller (ADRC) reported in [31]. Those controllers consider the nonlinear models of the converters, which ensures the global stability of the system, and also improves the robustness to parameters' variations.

The authors of [31] propose a cascaded controller formed by two ADRC regulators for charging/discharging a flywheel ESD. The inner loop regulates the inductor current of a Buck–Boost converter and the outer loop regulates the DC-bus voltage (discharge operation) or the ESD voltage (charge operation). However, the implementation of each ADRC regulator requires high computational

burden in comparison with other nonlinear controllers (e.g., SMC). Moreover, each ADRC regulator has eleven parameters that need to be defined, which makes the controller tuning difficult.

The authors of [8] propose an SMC for a hybrid energy storage system, composed of a fuel cell and a supercapacitor, in order to regulate the voltage of a DC-bus. Both the fuel cell and the supercapacitor are connected to the DC-bus through Boost converters, one unidirectional for the fuel cell and another bidirectional for the supercapacitor. Similarly, the authors of [33] propose an SMC for a system composed by a PV panel and a unidirectional Buck–Boost converter. In that work, the operation voltage of the PV panel could be higher or lower than the DC-bus voltage, depending on the environmental conditions. Therefore, a step up/down converter, like the Buck–Boost topology, is required to ensure the correct connection of the PV panel to the DC-bus. Nonetheless, the authors of [8,33] do not analyze the transversality and reachability (or equivalent control) conditions of the SMC; thus, those works do not provide any method to calculate the controller parameters. Moreover, the solution proposed in [33] can only be used to charge a ESD due to the unidirectional topology adopted. In addition, the validation presented in [33] is performed by replacing the ESD with a resistor; hence, the converter interacts with a linear impedance (the resistor) instead of a nonlinear and realistic one (the ESD).

Instead, the authors of [30] propose a system to regulate the voltage of a DC-bus by charging/discharging an ESD. The system is composed by an ESD connected to a DC-bus through a bidirectional Boost converter, which is controlled by an SMC. The SMC measures the voltage and current of the ESD and calculates the activation signal of the converter's switches by using a Proportional-Integral (PI) type sliding surface. The paper analyzes the transversality and reachability conditions to ensure the global stability of the system. Moreover, the paper also provides a complete design procedure for the controller parameters. Nonetheless, this work does not include a procedure for the design of the DC/DC converter, i.e., the capacitor and the inductor values. Finally, the DC-bus current is not included into the sliding surface, which reduces the dynamic response of the SMC to disturbances in the DC-bus.

The voltage levels of both the ESD and the DC-bus vary, depending on the particular MG, due to the diversity of ESD and power electronics manufacturers available in the market [21]. The following are some ESD and DC-bus voltages reported in literature:

- ESD voltages: 12 V [30], 48 V [25,27,34,35], 0 V to 70 V [31], 200 V [36], 288 V [29], 300 V [8,24], 400 V [22], 500 V [22], 624 V [26], 320 V to 480 V [32],
- DC-bus voltages: 24 V to 48 V [31], 48 V [30], 200 V [37], 400 V [8,25,32], 450 V [36], 500 V [24] 600 V [16], 700 V [23], 790 V [29], 1150 V [26].

As discussed before, step-up converters (e.g., Boost) are commonly used to connect the ESD to the DC-bus, which is the result of selecting ESDs with relative low voltages [8,29,30]. Nevertheless, it could be necessary to connect a relatively high-voltage ESD (e.g., ESD used in [22,26]) to a relatively low-voltage DC-bus (e.g., DC-bus used in [8,36,37]). This could be required to replace a damaged ESD, to increase the storage capacity, or to reduce the ESD currents and power losses. In such cases, it is necessary to adopt bidirectional step-up/down converters [31,32].

In the literature, multiple step-up/down converters are reported [31,32,38,39]. In particular, the work reported in [38] provides a review of non-isolated step-up/down converters, which includes the state-space models of five different topologies. The review also provides a comparison of the converters' mathematical expressions and performance indicators: efficiency, voltage gain, and losses. Similarly, Zhang et al. [39] present a review of three-port DC/DC converters used to interface renewable energy sources and ESD. In those converters, two ports are used to connect a DC power source and an ESD, while the third port is used to connect the load. Some of the three-port topologies presented in [39] are obtained by inserting additional switching element to the Buck–Boost or Sepic topologies [40–42]. Nonetheless, the works presented in [38–42] are focused on analyzing the operation and modulation of the converters. In particular, those references do not discuss the design and control strategies aimed at regulating the voltage of MGs DC-buses.

The works presented in [31,32] propose other step-up/down converters for interfacing the ESD and the DC-bus voltage of an MG. On one hand, the authors of [32] propose an isolated step-up/down topology denominated Bidirectional Soft-Switching Series-Resonant Converter. However, that converter requires a large number of elements in comparison with traditional step-up/down converters. Moreover, the paper does not propose a control strategy to regulate the DC-bus voltage, and it does not discuss the design procedure of the converter. On the other hand, in [31], the authors use a Buck–Boost converter and a nonlinear controller, based on ADRC, to manage the charging/discharging of a flywheel ESD. Nevertheless, such a system is able to regulate the DC-bus voltage only during the discharging of the ESD. Furthermore, the paper does not provide a detailed design procedure for both the controller and the Buck–Boost converter.

This paper proposes a system, formed by an ESD and a bidirectional Buck–Boost converter, controlled by with a single SMC, to regulate the DC-bus voltage of a DC or hybrid MG. The paper provides the analysis of the transversality and reachability conditions of the SMC, to ensure global stability, and it also proportions detailed design procedures for both the controller and DC/DC converter parameters. The proposed solution is validated with simulation and experimental results, which make evident three main advantages with respect to the solutions available in the literature: first, the use of a bidirectional Buck–Boost topology enables the connection of any ESD, i.e., ESD with operation voltages lower or higher than the DC-bus voltage; second, the provided design procedures for both the SMC and the converter are useful to develop a particular application with different voltage and current levels; finally, the implementation of the proposed solution is simple, thus it can be done with analog circuits or low-cost microcontrollers.

2. Charger-Discharger Circuit and Model

The charger–discharger circuit adopted in this paper is presented in Figure 1. This charger–discharger is based on a bidirectional Buck–Boost topology [43]; hence, it is capable of interfacing an ESD and a DC-bus with any voltage relation. In this electrical model, the ESD is represented with a voltage source due to the large capacitance of the ESD [30], while the DC-bus is represented with both a capacitor C and a current source. Such a DC-bus representation aggregates into the current source i_{dc} both the current demand of the loads and the current supply of the energy resources connected to the DC-bus. Hence, i_{dc} could be either positive (power must be extracted from the ESD) or negative (power must be stored into the ESD) depending on the power balance between loads and energy resources.

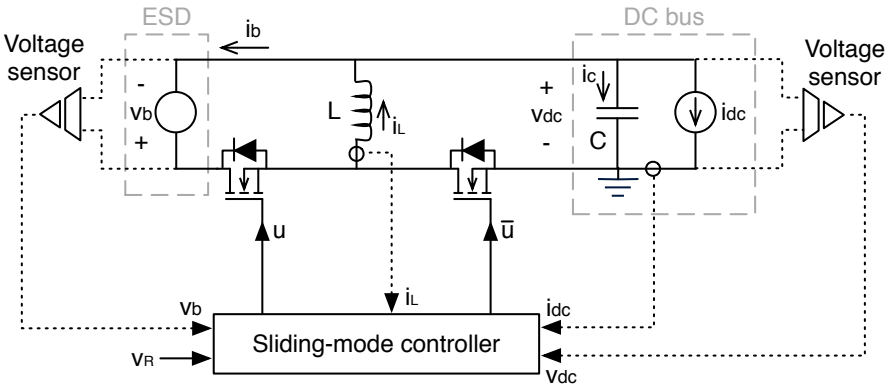


Figure 1. Buck–Boost charger–discharger connected to a DC-bus.

The circuital scheme in Figure 1 defines the physical variables used to design and process the converter controller aimed at regulating the DC-bus voltage: the ESD voltage v_b, the DC-bus voltage v_{dc}, the DC-bus current i_{dc}, the inductor current i_L and the desired (reference) DC-bus voltage V_R. The controller generates the control signal u and the complementary signal $\overline{u} = 1 - u$ in order to

define the states of the MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor). In addition, the scheme also defines the current conventions for both the ESD and capacitor currents, i.e., i_b and i_C, respectively.

The switched differential equations for the inductor current i_L (1) and capacitor (DC-bus) voltage v_{dc} (2) are obtained by using the charge and flux balance principles [43]. In these expressions, L and C are the values of the converter inductance and DC-bus capacitance, respectively:

$$\frac{di_L}{dt} = \frac{1}{L}\left[v_b \cdot u - v_{dc} \cdot (1-u)\right], \tag{1}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C}\left[i_L \cdot (1-u) - i_{dc}\right]. \tag{2}$$

The small-ripple approximation [43] considers averaging the DC/DC converter signals during each switching period T_{sw} to remove the switching ripple. The duty cycle d of the charger–discharger, given in Equation (3), is obtained by applying the small-ripple approximation to the MOSFET signal u. Similarly, the averaged inductor current $\langle i_L \rangle$ and capacitor voltage $\langle v_{dc} \rangle$ differential equations are given in Equations (4) and (5), respectively:

$$d = \frac{1}{T_{sw}} \int_0^{T_{sw}} u \, dt \tag{3}$$

$$\frac{d\langle i_L \rangle}{dt} = \frac{1}{L}\left[v_b \cdot d - \langle v_{dc} \rangle \cdot (1-d)\right], \tag{4}$$

$$\frac{d\langle v_{dc} \rangle}{dt} = \frac{1}{C}\left[\langle i_L \rangle \cdot (1-d) - i_{dc}\right]. \tag{5}$$

The voltage conversion ratio $\frac{\langle v_{dc} \rangle}{v_b}$ and the averaged capacitor current $\langle i_C \rangle$ of the converter are obtained from Equations (4) and (5) as follows:

$$\frac{\langle v_{dc} \rangle}{v_b} = \frac{d}{1-d}, \tag{6}$$

$$\langle i_C \rangle = \langle i_L \rangle \cdot (1-d) - i_{dc}. \tag{7}$$

Finally, from Equation (6), it is possible to define $d = \frac{\langle v_{dc} \rangle}{v_b + \langle v_{dc} \rangle}$, which makes evident that the duty cycle only depends on the averaged values of the capacitor and ESD voltages; hence, it is independent from the sign of both inductor and DC-bus currents.

3. Sliding-Mode Controller

The regulation of the DC-bus voltage must be ensured in any operation condition, i.e., charging the ESD, discharging the ESD or in stand-by mode (null ESD current). This paper proposes a nonlinear controller based on the sliding-mode theory to achieve that goal.

The sliding-mode controller (SMC) must minimize the error between the DC-bus voltage v_{dc} and the desired reference V_R. Moreover, from the circuit in Figure 1, it is observed that the main perturbation for the DC-bus voltage corresponds to the variations in the DC-bus current i_{dc}. Those perturbations, as reported in Equation (2), can be rapidly compensated by acting on the inductor current i_L to avoid large deviations of the DC-bus voltage from V_R. Therefore, the sliding surface governing the closed-loop regime must include the voltage error, the DC-bus current and the inductor current. The switching function Ψ and sliding surface Φ proposed to implement the SMC are reported in Equations (8) and (9), respectively, in which the parameters k_v and k_i must be calculated to provide the desired dynamic response:

$$\Psi = k_v \cdot (v_{dc} - V_R) + k_i \cdot i_L - i_{dc}, \tag{8}$$

$$\Phi = \{\Psi = 0\}. \tag{9}$$

Moreover, the analysis of the SMC requires the calculation of the switching function derivative, which is given in Equation (10). It must be noted that Expression (10) considers a constant reference value V_R, i.e., $\frac{dV_R}{dt} = 0$, which is a correct assumption since the DC-bus voltage of a microgrid must be constant [30]:

$$\frac{d\Psi}{dt} = k_v \cdot \frac{dv_{dc}}{dt} + k_i \cdot \frac{di_L}{dt} - \frac{di_{dc}}{dt}. \tag{10}$$

Finally, the explicit derivative of the switching function is calculated by replacing Equations (1) and (2) into Equation (10) as follows:

$$\frac{d\Psi}{dt} = \frac{k_v}{C}\left[i_L \cdot (1-u) - i_{dc}\right] + \frac{k_i}{L}\left[v_b \cdot u - v_{dc} \cdot (1-u)\right] - \frac{di_{dc}}{dt}. \tag{11}$$

To ensure the existence of the sliding-mode, thus the system global stability, three conditions must be fulfilled [44]: transversality, reachability and equivalent control. However, Sira-Ramirez demonstrated in [45] that equivalent control and reachability conditions are equivalent. Therefore, the following subsections analyze the transversality and reachability conditions of the proposed SMC.

3.1. Transversality Condition

The transversality condition evaluates the capacity of the SMC to modify the system trajectory. The mathematical representation of the transversality test is given in Expression (12) [44], which means that the control signal u must be present into the switching function derivative (11). The fulfillment of condition (12) ensures the controller is able to modify the behavior of the switching function Ψ, which makes it possible to drive Ψ to operate within the sliding surface Φ. Otherwise, if condition (12) is not fulfilled, the switching function is not controllable with u and the closed-loop system will not be stable:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) \neq 0. \tag{12}$$

Replacing Equation (11) into Expression (12) leads to Equation (13), which ensures that an SMC implemented with Equations (8) and (9) fulfills the transversality condition. It must be highlighted that conditions $k_v \neq 0$ and $k_i \neq 0$ are required to ensure the transversality condition (13). Those assumptions are correct since both k_v and k_i parameters must be different from zero to enable the inclusion of the voltage error and inductor current into the switching function:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = -\frac{k_v}{C}\left(i_L\right) + \frac{k_i}{L}\left(v_b + v_{dc}\right) \neq 0. \tag{13}$$

The next step to evaluate the stability of the SMC is to analyze the reachability conditions. Those conditions evaluate the ability of the switching function Ψ to reach the surface $\Phi = \{\Psi = 0\}$: when $\Psi < 0$, the switching function derivative must be positive to reach $\Psi = 0$, i.e., condition (14); when $\Psi > 0$, the switching function derivative must be negative to reach $\Psi = 0$, i.e., condition (15):

$$\Psi < 0 \Rightarrow \frac{d\Psi}{dt} > 0, \tag{14}$$

$$\Psi > 0 \Rightarrow \frac{d\Psi}{dt} < 0. \tag{15}$$

However, the analyses of Expressions (14) and (15) depend on the sign of the transversality value [44]. A positive sign of Equation (13) implies a positive sign of $\frac{d\Psi}{dt}$ for $u = 1$ and a negative sign of $\frac{d\Psi}{dt}$ for $u = 0$. Instead, a negative sign of Equation (13) implies a positive sign of $\frac{d\Psi}{dt}$ for

$u = 0$ and a negative sign of $\frac{d\Psi}{dt}$ for $u = 1$. Those practical reachability conditions are summarized in Expressions (16) and (17):

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) > 0 \quad \Rightarrow \quad \left\{ \lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \quad \text{and} \quad \lim_{\Psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \right\}, \tag{16}$$

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) < 0 \quad \Rightarrow \quad \left\{ \lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=0} > 0 \quad \text{and} \quad \lim_{\Psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=1} < 0 \right\}. \tag{17}$$

Therefore, the selection of the appropriate reachability conditions, between Expressions (16) and (17), requires the analysis of the transversality value (13). Nevertheless, the sign of Equation (13) depends on the signs of k_v and k_i; hence, those parameters are investigated in the following subsection using the equivalent dynamics concept.

3.2. Equivalent Dynamics and Parameters Design

The equivalent dynamics concept analyze the effect of the SMC in the closed-loop behavior [44]. This analysis is performed by assuming stable the closed-loop system, which is mathematically represented by $\Psi = 0$. Thus, the system (the switching function Ψ) is considered operating into the desired sliding surface Φ (9).

Replacing the switching function (8) into the sliding surface (9) gives Equation (18), which enables calculating the closed-loop inductor current given in Equation (19):

$$k_v \cdot (v_{dc} - V_R) + k_i \cdot i_L - i_{dc} = 0, \tag{18}$$

$$i_L = -\frac{1}{k_i}\left[k_v \cdot (v_{dc} - V_R) - i_{dc}\right]. \tag{19}$$

Averaging Equation (19) within the switching period, using the small ripple approximation [43], gives Equation (20). Then, replacing Expression (20) into the averaged differential equation of the DC-bus voltage (5) leads to Equation (21), which describes the dynamic behavior of the averaged DC-bus voltage under the action of the SMC:

$$\langle i_L \rangle = -\frac{1}{k_i}\left[k_v \cdot (\langle v_{dc} \rangle - V_R) - i_{dc}\right], \tag{20}$$

$$\frac{d\langle v_{dc} \rangle}{dt} = \frac{1}{C}\left\{-\frac{(1-d)}{k_i}\left[k_v \cdot (\langle v_{dc} \rangle - V_R) - i_{dc}\right] - i_{dc}\right\}. \tag{21}$$

It must be noted that the difference between $\langle v_{dc} \rangle$ and the DC-bus voltage v_{dc} corresponds to the switching ripple, hence a stable $\langle v_{dc} \rangle$ also ensures a stable v_{dc}.

Expression (21) considers the action of the SMC; hence, the control signal u is not present. Instead, this expression includes the converter duty cycle, which must be almost constant when the controller is operating properly, i.e., the DC-bus voltage is regulated near the desired value. Under the light of such a realistic assumption, the dynamic behavior of Equation (21) is expressed in frequency domain using Laplace transformation as given in Equation (22):

$$\langle V_{dc} \rangle (s) = \frac{1}{1 + \frac{k_i \cdot C}{k_v \cdot (1-d)} s} V_R(s) + \frac{\frac{(1-d) - k_i}{k_v \cdot (1-d)}}{1 + \frac{k_i \cdot C}{k_v \cdot (1-d)} s} I_{dc}(s). \tag{22}$$

From Expression (22), the following conditions are identified:

- k_i and k_v must exhibit the same sign to impose a stable equivalent pole at $-\frac{k_v \cdot (1-d)}{k_i \cdot C}$, which guarantees a stable closed-loop behavior.

- In steady-state, the value of V_R is transferred to $\langle v_{dc} \rangle$ (and v_{dc}) with a gain equal to 1, i.e., without error. Similarly, in steady-state, the value of i_{dc} is transferred to both $\langle v_{dc} \rangle$ and v_{dc} with a gain equal to $\frac{(1-d)-k_i}{k_v \cdot (1-d)}$.

The last condition imposes a steady-state error to the DC-bus voltage when the DC-bus current is different from zero. Therefore, the adaptive value of k_i, given in Equation (23), is calculated from Expression (22), which ensures a rejection of the error introduced by the DC-bus current i_{dc}. Moreover, since k_i is positive, it is concluded that k_v must be also positive to provide a stable closed-loop behavior:

$$k_i = 1 - d = \frac{v_b}{v_b + v_{dc}}. \tag{23}$$

Taking into account the adaptive law for k_i, imposed in Equation (23), the new closed-loop dynamic of the DC-bus voltage is:

$$\frac{\langle V_{dc} \rangle (s)}{V_R(s)} = \frac{1}{1 + \frac{C}{k_v} s}. \tag{24}$$

The closed-loop behavior given in Equation (24) corresponds to a first-order system with a time constant $\tau = \frac{C}{k_v}$. Therefore, the DC-bus voltage reaches the desired value V_R after a settling time $t_s \approx 4 \cdot \tau$ for the 2% criterion [30]. With that information, the value of k_v given in Equation (25) is calculated to impose the desired settling time t_s to the DC-bus voltage:

$$k_v = \frac{4 \cdot C}{t_s}. \tag{25}$$

Finally, since both k_i and k_v parameters have been calculated in Equations (23) and (25), respectively, the design of the proposed SMC is complete. However, the reachability conditions must be analyzed to ensure the sliding function reaches the sliding surface. Those conditions are evaluated in the following subsection.

3.3. Reachability Conditions and Dynamic Restrictions

Taking into account that both k_i and k_v have been designed, the sign of the transversality value (13) must be evaluated to define the correct reachability conditions for the proposed SMC. Moreover, the sign of the transversality value also defines the circuital implementation of the SMC [44]; thus, the sign of the transversality value must be the same for all the operation conditions; otherwise, a realizable circuit will be difficult to synthesize.

The first step for the sign analysis is to replace the values of k_i and k_v, given in Equations (23) and (25), into the transversality value (13):

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = -\frac{4 \cdot i_L}{t_s} + \frac{v_b}{L}. \tag{26}$$

Then, such an expression must be analyzed for each operation condition as follows:

- *Stand-by mode:* the charger–discharger is not exchanging power between the ESD and the DC-bus; hence, the DC-bus and inductor currents are zero, i.e., $i_{dc} = 0$ and $i_L = 0$. This imposes a positive transversality value because both v_b and L are positive:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = \frac{v_b}{L} > 0. \tag{27}$$

Therefore, the transversality value must be positive in the other two operation conditions.

- *Charge mode:* the ESD is charged using power delivered by the DC-bus; hence, the DC-bus and inductor currents are negative, i.e., $i_{dc} < 0$ and $i_L < 0$. This imposes a positive transversality value because v_b, L and t_s are positive:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = -\frac{4 \cdot i_L}{t_s} + \frac{v_b}{L} > 0. \tag{28}$$

- *Discharge mode:* the ESD is discharged to deliver power into the DC-bus, hence the DC-bus and inductor currents are positive, i.e., $i_{dc} > 0$ and $i_L > 0$. In this case, the restriction given in Expression (29) must be fulfilled to ensure a positive transversality sign:

$$t_s > \frac{4 \cdot i_L \cdot L}{v_b}. \tag{29}$$

The most restrictive condition occurs at the maximum value of the inductor current $\max(i_L)$, which is calculated from the steady-state relations (6) and (7) as $\max(i_L) = \max(i_{dc}) \cdot (v_b + v_{dc}) / (v_b)$. Therefore, the most restrictive condition for the closed-loop settling time t_s that ensures a positive transversality value is:

$$t_s > \frac{4 \cdot \max(i_{dc}) \cdot L \cdot (v_b + v_{dc})}{{v_b}^2}. \tag{30}$$

Introducing restriction (30) in the designing of k_v (25) ensures a positive transversality value. Therefore, the reachability conditions given in Expression (16) hold for the SMC proposed in this paper. The first reachability condition is the result of replacing Equation (11) into the first inequality of Expression (16):

$$\lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \quad \Rightarrow \quad \lim_{\Psi \to 0^-} -\frac{k_v \cdot i_{dc}}{C} + \frac{k_i \cdot v_b}{L} - \frac{di_{dc}}{dt} > 0. \tag{31}$$

Replacing k_i (23) and k_v (25) into Expression (31), the following dynamic restriction is obtained:

$$\frac{di_{dc}}{dt} < -\frac{4 \cdot i_{dc}}{t_s} + \frac{{v_b}^2}{L\,(v_b + v_{dc})}. \tag{32}$$

Similarly, the second reachability condition is the result of replacing Equation (11) into the second inequality of Expression (16):

$$\lim_{\Psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \quad \Rightarrow \quad \lim_{\Psi \to 0^+} \frac{k_v\,(i_L - i_{dc})}{C} - \frac{k_i \cdot v_{dc}}{L} - \frac{di_{dc}}{dt} < 0. \tag{33}$$

Replacing k_i, k_v, i_L and d into Expression (33) imposes the following dynamic restriction:

$$\frac{di_{dc}}{dt} > \frac{4 \cdot i_{dc}}{t_s}\left(\frac{v_{dc}}{v_b}\right) - \frac{v_b \cdot v_{dc}}{L\,(v_b + v_{dc})}. \tag{34}$$

Fulfilling the dynamic restrictions given in Expressions (32) and (34) ensure that both reachability conditions (31) and (33) are also fulfilled. Therefore, the maximum and minimum derivatives of the DC-bus current must be constrained by Expressions (32) and (34), respectively. It must be highlighted that he selected t_s value must be tested into Expressions (32) and (34) using the expected derivatives appearing in the DC-bus current, which can be calculated from the dynamic behavior of the energy sources and loads connected to the microgrid.

In addition, the dynamic restrictions (32) and (34), simultaneously with the relation between k_v, t_s and C given in Equation (25), are used to design the charger–discharger: the values of L and C are

calculated to provide the desired settling-time and to ensure the stability of the DC-bus voltage. Such a design process for L and C will be described in Section 5.

4. Controller Implementation

The proposed SMC requires measuring the inductor current i_L, the ESD voltage v_b, the DC-bus voltage v_{dc} and current i_{dc}. Moreover, the SMC produces the activation signals u and $\overline{u} = 1 - u$ for both MOSFETs of the charger–discharger (see Figure 1).

The block diagram of the state-space representation for both the charger–discharger and the SMC is presented in Figure 2. In such a block diagram, the switching function Ψ is synthesized as follows: k_i parameter is dynamically calculated using the values of the ESD and DC-bus voltages as given in Equation (23), while parameter k_v is calculated off-line using Equation (25) to impose the desired settling time t_s. Then, the value of Ψ is calculated as reported in Equation (8).

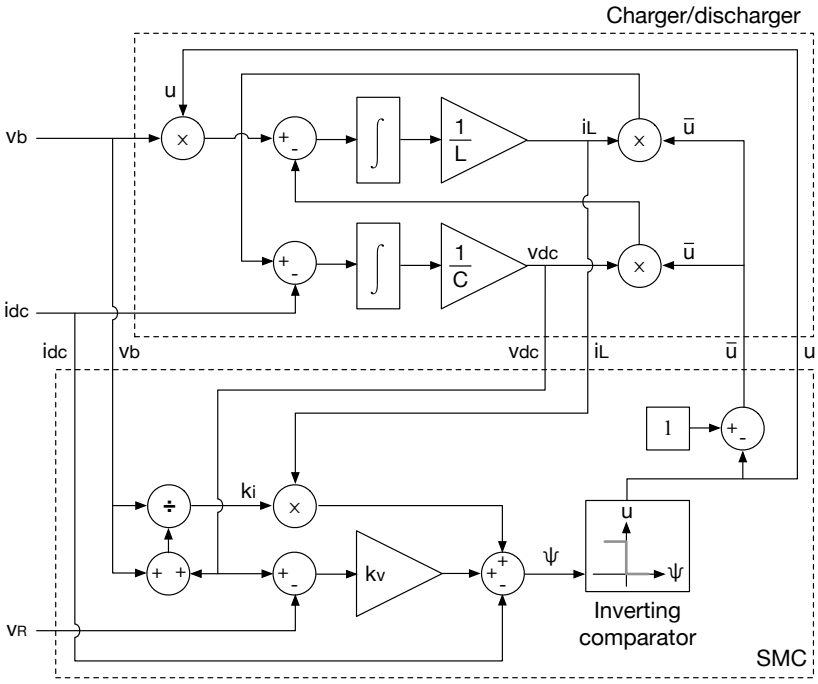


Figure 2. Block diagram of the charger–discharger with the Sliding-Mode Controller (SMC).

The switching law for the MOSFETs is defined by the reachability conditions: from Expression (31), it is recognized that a negative value of Ψ requires $u = 1$ to ensure $\frac{d\Psi}{dt} > 0$; similarly, from Expression (33), it is recognized that a positive value of Ψ requires $u = 0$ to ensure $\frac{d\Psi}{dt} < 0$. That switching law, summarized in Expression (35), corresponds to an inverting comparator, which is also depicted in the block diagram of Figure 2. Finally, the generation of $\overline{u}$ from u is also presented in Figure 2:

$$\Psi < 0 \rightarrow u = 1 \quad \text{and} \quad \Psi > 0 \rightarrow u = 0 \quad , \quad \overline{u} = 1 - u. \tag{35}$$

Unfortunately, the theoretical switching law given in Expression (35) imposes an infinite switching frequency [44], which is impossible to achieve using commercial MOSFETs. This implementation problem is addressed by introducing an hysteresis around the desired condition $\Psi = 0$ to constrain the switching frequency into a practical range [44]. The practical switching law is given in Expression (36), which introduces an hysteresis H into the sliding surface:

$$\Psi < -\frac{H}{2} \rightarrow u = 1 \quad \text{and} \quad \Psi > \frac{H}{2} \rightarrow u = 0 \quad , \quad \overline{u} = 1 - u. \tag{36}$$

The following subsections describe the switching circuit used to implement the practical switching law, the design of the hysteresis band H, the switching frequency and the switching ripples imposed to the charger–discharger.

4.1. Switching Circuit

The implementation of the practical switching law (36) is perfomed with the following conditions:

$$\text{if } \Psi = -\frac{H}{2} \;\rightarrow\; \{u = 1\,,\; \overline{u} = 0\}\,, \tag{37}$$

$$\text{if } \Psi = \frac{H}{2} \;\rightarrow\; \{u = 0\,,\; \overline{u} = 1\}\,. \tag{38}$$

The corresponding circuit is implemented using two classical comparators to detect conditions (37) and (38) as reported in Figure 3. Those comparators act on the SET and RESET signals of a S-R Flop-Flop to generate both u and $\overline{u}$ waveforms: the comparator implementing Expression (37) turns ON (SET) u, while the comparator implementing Expression (38) turns OFF (RESET) u. Finally, the signals u and $\overline{u}$ act on the drivers of the charger–discharger MOSFETs.

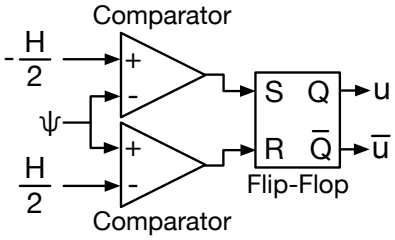


Figure 3. Switching circuit.

4.2. Switching Ripples

The switched operation of the MOSFETs produce ripples in both the inductor current ($\delta i_L(t)$) and the DC-bus voltage ($\delta v_{dc}(t)$) around their averaged values $\langle i_L \rangle$ and $\langle v_{dc} \rangle$, respectively [43]:

$$i_L = \langle i_L \rangle + \delta i_L(t), \tag{39}$$

$$v_{dc} = \langle v_{dc} \rangle + \delta v_{dc}(t). \tag{40}$$

The switched differential Equations (1) and (2) impose the following derivatives to i_L and v_{dc} for $u = 1$:

$$u = 1 \quad \Rightarrow \quad \begin{cases} \dfrac{di_L}{dt} = \dfrac{v_b}{L}, \\ \dfrac{dv_{dc}}{dt} = -\dfrac{i_{dc}}{C}, \end{cases} \qquad \text{at} \quad 0 < t < d \cdot T_{sw}. \tag{41}$$

The standard notation [43] defines $u = 1$ during the time interval $0 < t < d \cdot T_{sw}$. Then, the current ripple waveform of the inductor during $0 < t < d \cdot T_{sw}$, around $\langle i_L \rangle$, is given in Equation (42). In that expression, Δi_L is the magnitude of the peak current ripple reported in Equation (43). Therefore, the maximum value of $\delta i_L(t)$ is Δi_L and the minimum value of $\delta i_L(t)$ is $-\Delta i_L$:

$$\delta i_L(t) = \frac{v_b}{L} \cdot t - \Delta i_L, \tag{42}$$

$$\Delta i_L = \frac{v_b \cdot d \cdot T_{sw}}{2 \cdot L} = \frac{v_b \cdot v_{dc}}{2 \cdot L \cdot F_{sw} \cdot (v_b + v_{dc})}. \tag{43}$$

It is noted that $\delta i_L(t)$ increases for $u = 1$ in any operation condition. However, the voltage ripple waveform in the DC-bus $\delta v_{dc}(t)$ decreases in *discharge mode* ($i_{dc} > 0$), increases in *charge mode* ($i_{dc} < 0$) and it is equal to zero in *stand-by mode* ($i_{dc} = 0$) as reported in Expression (41). The definition of $\delta v_{dc}(t)$ is given by Expression (44), where Δv_{dc} is the magnitude of the peak voltage ripple reported in Equation (45):

$$\delta v_{dc}(t) = \begin{cases} -\frac{i_{dc}}{C} \cdot t + \Delta v_{dc}, & \text{if} \quad i_{dc} > 0, \\ 0, & \text{if} \quad i_{dc} = 0, \\ -\frac{i_{dc}}{C} \cdot t - \Delta v_{dc} & \text{if} \quad i_{dc} < 0, \end{cases} \tag{44}$$

$$\Delta v_{dc} = \frac{|i_{dc}| \cdot d \cdot T_{sw}}{2 \cdot C} = \frac{|i_{dc}| \cdot v_{dc}}{2 \cdot C \cdot F_{sw} \cdot (v_b + v_{dc})}. \tag{45}$$

From the previous expressions, it is concluded that the maximum value of $\delta v_{dc}(t)$ is Δv_{dc} and the minimum value of $\delta v_{dc}(t)$ is $-\Delta v_{dc}$.

Finally, Expressions (43) and (45) enable the calculation of the peak ripples of the inductor current and DC-bus voltage depending on the steady-state values of the duty cycle d, switching period T_{sw}, ESD voltage v_b, DC-bus current i_{dc}, L and C parameters. Moreover, those expressions are also used to design L and C in agreement with the desired current and voltage ripples for the charger–discharger.

4.3. Switching Frequency

Implementing an SMC with an hysteresis band imposes a variable switching frequency [44], whose maximum value must be supported by the MOSFETs used to construct the charger–discharger. Therefore, predicting the switching frequency is essential to select the appropriate semiconductor devices.

Assuming a correct operation of the SMC, which is ensured by the transversality and reachability conditions analyzed in Section 3, the averaged DC-bus voltage is equal to the reference voltage: $\langle v_{dc} \rangle = V_R$. Moreover, since $k_i = 1 - d$, the averaged value of the term $\{i_L \cdot k_i - i_{dc}\}$ in Ψ (8) is $\{\langle i_L \rangle \cdot (1 - d) - i_{dc}\}$, which is equal to the averaged value of the capacitor current $\langle i_C \rangle$ given in Equation (7). Taking into account that the charge balance principle [43] ensures that $\langle i_C \rangle = 0$ in steady-state, the relations between the ripples and averaged values given in Equations (39) and (40) lead to the following steady-state waveform of the switching function $\delta\Psi(t)$ around 0:

$$\delta\Psi(t) = k_v \cdot \delta v_{dc}(t) + (1 - d) \cdot \delta i_L(t). \tag{46}$$

To fulfill the hysteresis band, the minimum and maximum values of $\delta\Psi(t)$ are $\left\{\min\left(\delta\Psi(t)\right) = -\frac{H}{2}\right\}$ and $\left\{\max\left(\delta\Psi(t)\right) = \frac{H}{2}\right\}$, respectively. Moreover, the peak values of $\delta\Psi(t)$ occur at the peak values of $\delta v_{dc}(t)$ and $\delta i_L(t)$ because those waveforms are synchronized by u as reported in Equations (1) and (2).

Then, the peak value of Equation (46) must be analyzed in the three operation modes of the charger–discharger:

- *Discharge mode* ($i_{dc} > 0$): $\delta v_{dc}(t)$ and $\delta i_L(t)$ have opposite derivatives as reported in Expression (41), hence the maximum value of $\delta v_{dc}(t)$ occurs when $\delta i_L(t)$ is minimum. This condition leads to the following expression for the peak value of $\delta\Psi(t)$:

$$k_v \cdot \Delta v_{dc} - (1 - d) \cdot \Delta i_L = \frac{H}{2}, \tag{47}$$

- *Stand-by mode* ($i_{dc} = 0$): $\delta v_{dc}(t) = 0$ as reported in Expression (44), hence the peak value of $\delta\Psi(t)$ occurs at the peak value of $\delta i_L(t)$:

$$(1 - d) \cdot \Delta i_L = \frac{H}{2}, \tag{48}$$

- *Charge mode* ($i_{dc} < 0$): $\delta v_{dc}(t)$ and $\delta i_L(t)$ have derivatives with the same sign as reported in Equation (41), hence the maximum value of $\delta v_{dc}(t)$ occurs when $\delta i_L(t)$ is maximum. This condition leads to the following expression for the peak value of $\delta\Psi(t)$:

$$k_v \cdot \Delta v_{dc} + (1-d) \cdot \Delta i_L = \frac{H}{2}. \tag{49}$$

Replacing the values of k_v (25), Δi_L (43) and Δv_{dc} (45) into Equations (47)–(49) produce the following expressions for the switching frequency:

- *Discharge mode*:

$$F_{sw} = \frac{1}{H} \cdot \left(\frac{v_{dc}}{v_b + v_{dc}}\right) \cdot \left| -\frac{v_b^2}{L \cdot (v_b + v_{dc})} + \frac{4 \cdot |i_{dc}|}{t_s} \right| \quad \text{if} \quad i_{dc} > 0, \tag{50}$$

- *Stand-by mode*:

$$F_{sw} = \frac{1}{H} \cdot \left(\frac{v_{dc}}{v_b + v_{dc}}\right) \cdot \left[\frac{v_b^2}{L \cdot (v_b + v_{dc})} \right] \quad \text{if} \quad i_{dc} = 0, \tag{51}$$

- *Charge mode*:

$$F_{sw} = \frac{1}{H} \cdot \left(\frac{v_{dc}}{v_b + v_{dc}}\right) \cdot \left[\frac{v_b^2}{L \cdot (v_b + v_{dc})} + \frac{4 \cdot |i_{dc}|}{t_s} \right] \quad \text{if} \quad i_{dc} < 0. \tag{52}$$

From the previous expressions, it is concluded that *charge mode* produces higher switching frequencies. Therefore, the hysteresis band H must be calculated as given in Equation (53) to ensure a maximum switching frequency $\max(F_{sw})$. In that expression, $\max(i_{dc})_{charge}$ corresponds to the maximum magnitude of the DC-bus current expected in *charge mode*:

$$H = \frac{1}{\max(F_{sw})} \cdot \left(\frac{v_{dc}}{v_b + v_{dc}}\right) \cdot \left[\frac{v_b^2}{L \cdot (v_b + v_{dc})} + \frac{4 \cdot \max(i_{dc})_{charge}}{t_s} \right]. \tag{53}$$

Finally, Equation (53) ensures a switching frequency below $\max(F_{sw})$ for the three operating modes, hence any commercial MOSFET supporting switching frequencies higher than $\max(F_{sw})$ will operate correctly under the action of the proposed SMC.

5. Design of the Charger/Discharger and DC-Bus

This paper proposes a design procedure for both the charger–discharger and DC-bus based on the following criteria: maximum DC-bus current $\{\max(i_{dc})\}$, maximum DC-bus current derivative $\left\{\max\left(\frac{i_{dc}}{dt}\right)\right\}$, maximum deviation of the DC-bus voltage γ_{dc} to avoid overvoltages, and maximum settling time t_s acceptable after transients. These criteria must be extracted from the operation requirements of both the loads and energy resources connected to the microgrid.

The charger–discharger and DC-bus circuit was implemented in the power electronics simulator PSIM to illustrate the inductance and capacitance design. The simulation circuit, presented in Figure 4, also considers both the synthesis of the switching function Ψ and the switching circuit previously designed.

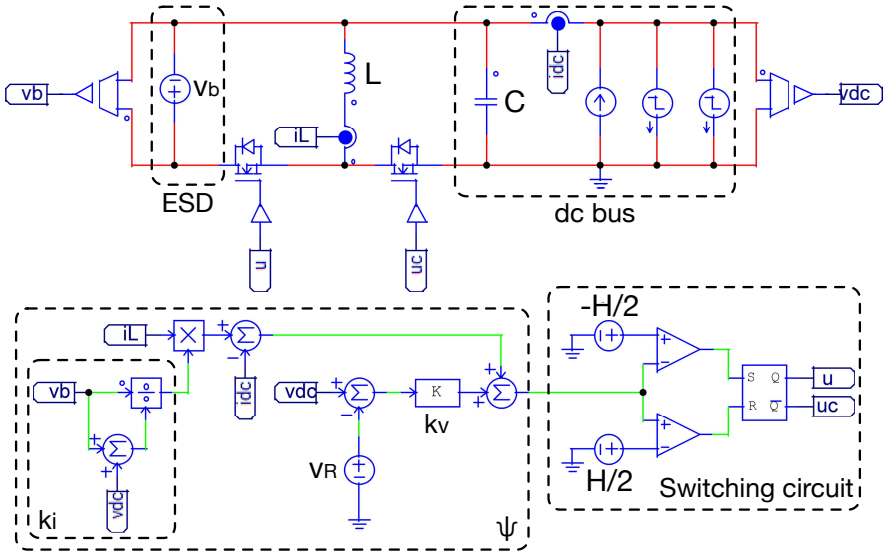


Figure 4. Simulation scheme implemented in PSIM software.

5.1. Inductance Value

The design of the inductance L must be performed to ensure two conditions: first, the required settling time is achievable; and second, the SMC operates into the sliding surface (9) even under transients in the DC-bus current. The best way to perform that design is to plot the stability limits imposed by the required settling time t_s and maximum DC-bus current.

The following parameters are considered to illustrate the inductor design: an ESD voltage (v_b) equal to 12 V, a desired DC-bus voltage (V_R) equal to 24 V, and a DC-bus current up to 1 A in both charge and discharge situations. Figure 5 presents the stability limits defined by Expressions (32) and (34) to achieve, for example, settling times equal to 0.2 ms and 2 ms. The plot shows that an inductor value higher than 200 µH makes it impossible to ensure a settling time equal to 0.2 ms. Such a maximum inductor value $\left\{\max(L) = \frac{t_s \cdot v_b^2}{4 \cdot \max(i_{dc}) \cdot (v_b + v_{dc})}\right\}$ is calculated by evaluating Expressions (32) or (34) equal to zero. However, $\max(L)$ is not practically usable because the system will be stable in steady-state conditions only $\left(\frac{di_{dc}}{dt} = 0\right)$.

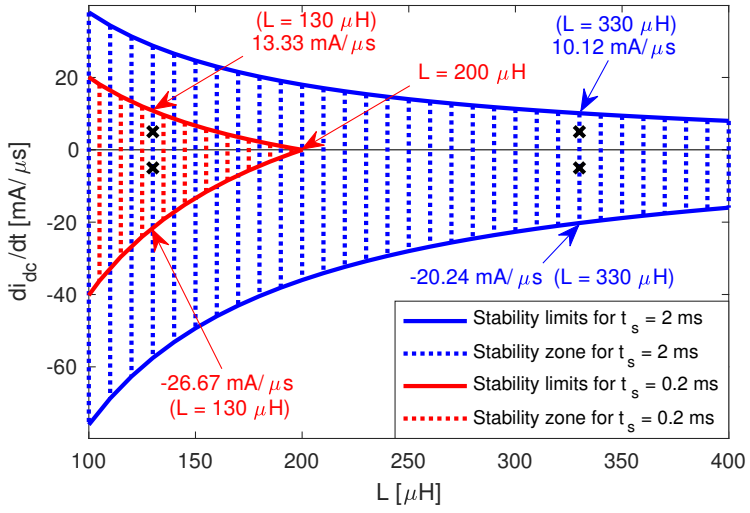


Figure 5. Plot for inductor design.

Assuming the DC-bus must support current transients with derivatives up to 5 mA/ µs (5000 A/s), selecting an inductor L = 130 µH provides the required t_s = 0.2 ms with stable sliding-mode regime for current transients up to 13.33 mA/µs (even up to 26.67 mA/µs for negative transients in i_{dc}); hence, the DC-bus will be correctly regulated. This behavior is expected because smaller values of L provide higher inductor current derivatives, as reported in Expression (41), thus the charger–discharger is able to respond to faster current transients. However, smaller inductors also provide higher current ripples, as reported in Equation (43), which introduce undesired (and detrimental) current harmonics to the ESD.

For the other example considering a settling time equal to 2 ms, the plot in Figure 5 shows that much larger inductor values could be adopted, which makes it possible to reduce the current ripples affecting the ESD. In fact, an inductor L = 330 µH enables the SMC to support similar current derivatives (10.12 mA/µs in this case) but with much smaller pollution of current harmonics.

Finally, constructing the plot for inductor design (Figure 5), using Expressions (32) and (34), makes it possible to easily select a commercially available inductor. This design method is validated by simulating in PSIM the charger–discharger using the circuit in Figure 4. The simulations, presented in Figure 6, evaluate the correct design of L to ensure a stable sliding-mode regime. For this example, the charger–discharger considers an inductor L = 330 µH and an hysteresis band H = 0.2 A to limit the switching frequency at 55 kHz.

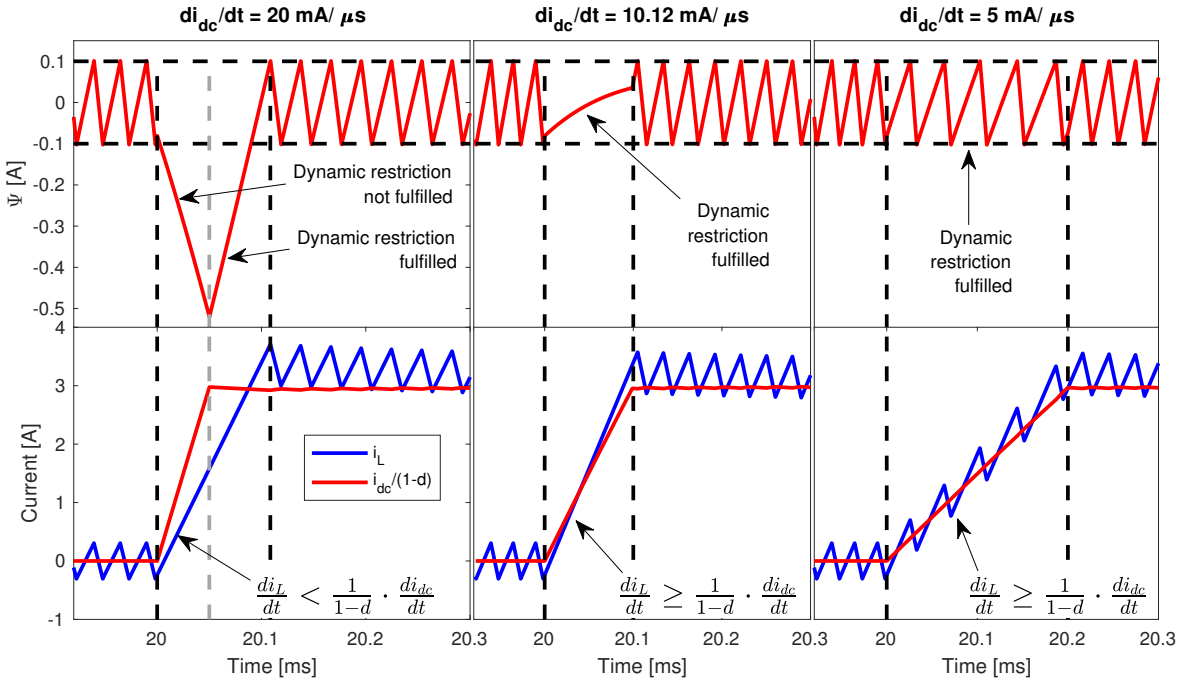


Figure 6. Validation of the inductor design process.

From the plot for inductor design (Figure 5), it is observed that L = 330 µH ensures a stable sliding-mode regime for current transients with derivatives $\frac{di_{dc}}{dt} \leq 10.12$ mA/µs. The simulation at the left in Figure 6 considers a current transient (at 20 ms) with $\frac{di_{dc}}{dt} = 20$ mA/µs > 10.12 mA/µs, hence the switching function Ψ is not trapped into the surface $-\frac{H}{2} < \Psi < \frac{H}{2}$ and the system is not stable during the transient. However, when the transient in the DC-bus current ends (at 20.04 ms), the new current derivative is $\frac{di_{dc}}{dt} \approx 0$ mA/µs < 10.12 mA/µs and the system becomes stable again, which drives Ψ into the surface. In steady-state conditions, e.g., $t < 20$ ms, the DC-bus voltage is regulated by the SMC at V_R, thus the theoretical sliding surface is $\Psi \approx (1-d) \cdot i_L - i_{dc} = 0$ because $k_i = (1-d)$. Therefore, to be in steady-state with a regulated DC-bus voltage, $i_L = \frac{i_{dc}}{1-d}$ is required,

which is confirmed in Figure 6 before $t < 20$ ms (bottom figure). However, the high derivative of the DC-bus current i_{dc} makes it impossible that i_L compensates the term $\frac{i_{dc}}{1-d}$, i.e., $\frac{di_L}{dt} < \frac{1}{1-d} \cdot \frac{di_{dc}}{dt}$, which forces Ψ to leave the sliding-surface.

The simulation at the center in Figure 6 considers a current transient in the DC-bus (at 20 ms) with $\frac{di_{dc}}{dt} = 10.12$ mA/µs, which is the stability limit reported in Figure 5, hence the system is stable even during the transient. In fact, the current waveforms for this case fulfills $\frac{di_L}{dt} \geq \frac{1}{1-d} \cdot \frac{di_{dc}}{dt}$ and Ψ is always trapped into the sliding-surface. The same stable behavior is observed in the simulation at the right of Figure 6, which considers a current transient in the DC-bus with $\frac{di_{dc}}{dt} = 5$ mA/µs, i.e., within the stability zone reported in Figure 5.

In conclusion, the proposed design method for the inductor ensures a stable operation under steady-state and transitory conditions.

5.2. Capacitance Value

The design of the capacitance C must be performed to limit the overvoltage conditions depending on the requirements of both the loads and energy resources connected to the DC-bus.

Despite the sliding-mode controller ensuring a correct regulation of the DC-bus voltage, the operation of the Buck–Boost converter introduces an unavoidable voltage deviation caused by fast current transients. Therefore, to limit the DC-bus voltage into secure limits, the design procedure for C proposed in this paper is based on the worst-case scenario: an instantaneous 100% step-down transient in the DC-bus current during discharge mode. This design condition ensures that voltage increments caused by any current transient with a lower (practical) current derivative will not damage the microgrid components.

In discharge mode, the voltage is regulated by the SMC at V_R, hence the switching function is $\Psi \approx k_i \cdot i_L - i_{dc}$. Then, after a 100% step-down transient in the DC-bus current occurs (instant t_0 in Figure 7), the DC-bus current becomes $i_{dc} = 0$ A and $\Psi \approx k_i \cdot i_L > 0$. Under those conditions, the SMC imposes $u = 0$ ($\overline{u} = 1$) until $\Psi = -\frac{H}{2}$ due to the switching circuit design (37) and (38).

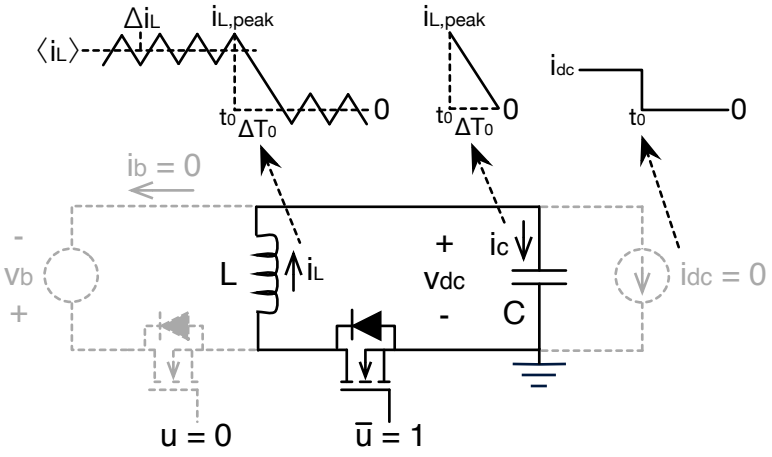


Figure 7. Current waveforms due to a 100% step-down DC-bus current transient.

Figure 7 presents the active devices and current waveforms in the circuit just after the step-down current transient occurs, i.e., $t \geq t_0$. Since $i_{dc} = 0$, all of the inductor current is absorbed by the capacitor ($i_C = i_L$), which increases the DC-bus voltage. This is caused by the structure of the Buck–Boost converter and not by the SMC design or speed: since the averaged capacitor current is zero due to the charge-balance principle [43], the averaged inductor current $\langle i_L \rangle$ must be zero when the DC-bus current is zero. Therefore, the SMC imposes a fixed $u = 0$ to reach the $\langle i_L \rangle = 0$ condition in the shortest time possible. However, reaching that condition $\langle i_L \rangle = 0$ takes a time-interval ΔT_0 as

depicted in Figure 7. During such ΔT_0 time interval, the inductor current is integrated by the capacitor producing an unavoidable overvoltage condition.

Since the SMC ensures reaching $\langle i_L \rangle = 0$ in the shortest time possible, it also ensures the smallest overvoltage condition. The magnitude of that minimum voltage deviation is defined by the DC-bus capacitance value C.

The current waveforms described in Figure 7 account for the worst case scenario: the transient in the DC-bus current occurs when the inductor current is maximum, therefore, at the peak current $i_{L,peak} = \langle i_L \rangle + \Delta i_L$. It is also possible that the current transient occurs when the inductor current is lower than $i_{L,peak}$, which will produce a smaller voltage deviation. Moreover, in discharge mode, the positive peak of i_L coincides with the negative peak of v_{dc}, as reported in Expression (41), hence the maximum voltage deviation γ_{dc} over V_R is calculated as:

$$\gamma_{dc} = \frac{1}{C} \int_{t_0}^{t_0+\Delta T_0} i_L \, dt - \Delta v_{dc}. \tag{54}$$

The integral term of the previous expression corresponds to the area of a triangle with base equal to ΔT_0 and height equal to $i_{L,peak}$ (see Figure 7). The term $i_{L,peak} = \langle i_L \rangle + \Delta i_L$ is calculated from Equations (6), (7) and (43) as follows:

$$i_{L,peak} = \frac{\max(i_{dc}) \cdot (v_b + v_{dc})}{v_b} + \frac{v_b \cdot v_{dc}}{2 \cdot L \cdot F_{sw} \cdot (v_b + v_{dc})}. \tag{55}$$

Using the previous value of $i_{L,peak}$ and the inductor current derivative given in Equation (1), the time interval ΔT_0 needed to reach $i_L = 0$ with $u = 0$ is:

$$\Delta T_0 = \frac{v_b}{2 \cdot F_{sw} \cdot (v_b + v_{dc})} + \frac{\max(i_{dc}) \cdot L \cdot (v_b + v_{dc})}{v_b \cdot v_{dc}}. \tag{56}$$

Finally, using the expressions for d and Δv_{dc} given in Equations (6) and (45), respectively, the maximum voltage deviation γ_{dc} over V_R is calculated as:

$$\gamma_{dc} = \frac{1}{2 \cdot C} \cdot \left\{ \sqrt{\frac{v_{dc}}{L}} \cdot \left[\frac{v_b}{2 \cdot F_{sw} \cdot (v_b + v_{dc})} \right] + \sqrt{\frac{L}{v_{dc}}} \cdot \left[\frac{\max(i_{dc}) \cdot (v_b + v_{dc})}{v_b} \right] \right\}^2 - \frac{\max(i_{dc}) \cdot v_{dc}}{2 \cdot C \cdot F_{sw} \cdot (v_b + v_{dc})}. \tag{57}$$

To illustrate the previous design equation, the same parameters adopted in the previous subsection are considered: an ESD voltage (v_b) equal to 12 V, a desired DC-bus voltage (V_R) equal to 24 V, and a DC-bus current up to 1 A in both charge and discharge situations. Moreover, the same settling time conditions have been addressed. For the first one (t_s = 0.2 ms), an inductor $L = 130$ µH is adopted to ensure an stable sliding-mode regime with current transients derivatives up to 5 mA/µs (see Figure 5). The hysteresis band is calculated from Equation (53) as H = 0.719 A to ensure a switching frequency lower than 55 kHz. The second settling time condition (t_s = 2 ms) enables the use of a higher inductor L = 330 µH, which ensures the same stable sliding-mode regime (see Figure 5) but with a reduced current harmonics pollution injected into the ESD. In this second case, the hysteresis band is H = 0.2 A to provide the same switching frequency. Figure 8 shows the maximum overvoltage γ_{dc} in both cases for different DC-bus capacitances. The figure shows that the same maximum overvoltage condition can be ensured with different values of C; for example, $\gamma_{dc} = 1$ V is ensured with C = 66 µF for $t_s = 2$ ms and with C = 29 µF for $t_s = 0.2$ ms. However, higher values of C produce smaller voltage ripples in the DC-bus as reported in Equation (45), thus providing higher voltage quality to both the loads and energy resources of the microgrid. Furthermore, the reduction of the voltage deviation caused by higher capacitances also reduces the energy stored or requested to the DC-bus during a

current transient, i.e., $E_{bus} = \frac{1}{2}C \cdot v_{dc}^2$. Therefore, the energy exchanged between the DC-bus and the ESD during the bus voltage regulation also decrease. This characteristic enables the increment of the DC-bus capacitor without an increment of the ESD size.

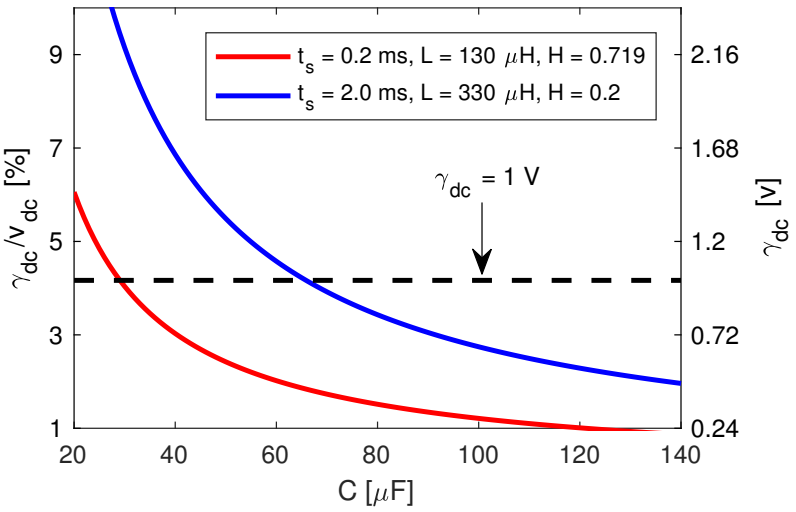


Figure 8. Example of capacitor design.

The previous method is validated by simulating in PSIM the charger–discharger circuit depicted in Figure 4. The simulations, presented in Figure 9, evaluate the correct design of C to ensure a safe maximum voltage in the DC-bus. For this example, the SMC considers a settling-time $t_s = 2$ ms and the charger–discharger considers an inductor L = 330 µH and an hysteresis band H = 0.2 A to limit the switching frequency at 55 kHz.

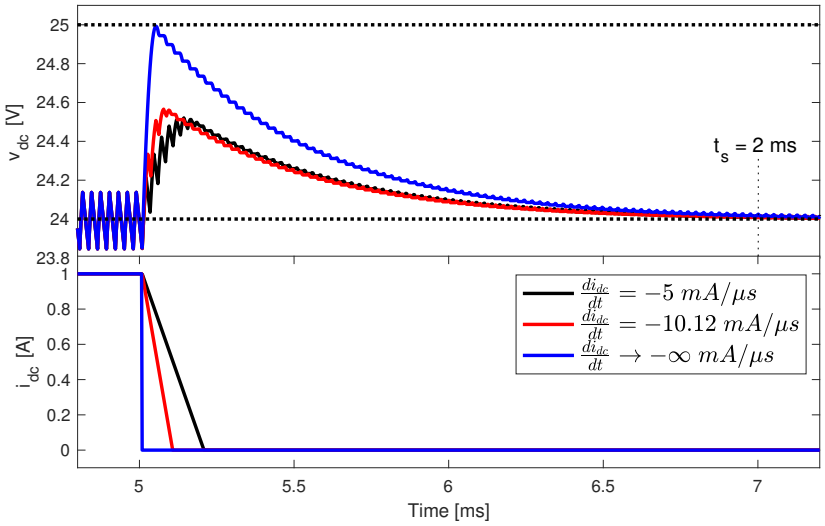


Figure 9. Validation of the capacitor design process.

Assuming a maximum safe voltage for the DC-bus equal to 25 V, the capacitor must be designed for $\gamma_{dc} = 1$ V. From the plot for capacitor design (Figure 8), it is observed that C = 66 µF ensures $\gamma_{dc} = 1$ V for t_s = 2 ms. The simulations in Figure 9 consider such a capacitance for three current transients in the DC-bus (at 5 ms) with the following current derivatives: $\frac{di_{dc}}{dt} \to -\infty$ mA/µs (ideal step), $\frac{di_{dc}}{dt} = -10.12$ mA/µs and $\frac{di_{dc}}{dt} = -5$ mA/µs. In the first case, which is the one used for design a safe value of C, the 100% step-down current transient in the DC-bus causes the predicted maximum

overvoltage condition $\gamma_{dc} = 1$ V. Instead, the other two current transients produce overvoltage conditions under 1 V, which confirm the analyses developed in this subsection.

In conclusion, the proposed design method ensures a safe maximum voltage in the DC-bus for any transitory condition. It must be pointed out that simulations in Figure 9 also validate the design of k_i and k_v because, in the three cases, the settling-time of the DC-bus voltage is the designed one $t_s = 2$ ms and the steady-state error in v_{dc} is zero.

6. Design Example

The following parameters are adopted to illustrate the performance of the proposed solution: an ESD voltage (v_b) equal to 12 V, a desired DC-bus voltage (V_R) equal to 24 V, a DC-bus current up to 1 A with maximum derivatives $\frac{di_{dc}}{dt} = \pm 5000$ A/s (5 mA/µs). This speed in the current transients is common in automotive battery test systems, which are used to create the current profiles for life cycle evaluations of batteries, as reported in [46,47]. Moreover, to avoid damage in the loads and energy resources, the maximum DC-bus voltage must be limited to 1 V over the nominal value (up to 25 V). Finally, DC-bus voltage must be restored after 2 ms and the switching frequency must be limited to 55 kHz, which enables the use of inexpensive MOSFETs.

This example illustrates the simplicity of the circuit design process by means of four steps: design the inductor of the charger–discharger, design the capacitance of the DC-bus, design the controller parameters and design the hysteresis band of the switching circuit.

The first step is to construct the inductor design plot presented in Figure 5 using Expressions (32) and (34) for $t_s = 2$ ms. From that plot, it is noted that $L \leq 400$ µH ensures the dynamic stability for the expected current transient derivative $\frac{di_{dc}}{dt} = 5$ mA/µs. However, two additional conditions must be considered: the tolerance of commercially available inductors and the current ripple injected into the ESD. To account for the tolerance, this example considers a factor of two for the current derivative, so that the inductor is selected from Figure 5 for $\frac{di_L}{dt} \leq 10$ mA/µs, which requires $L \leq 333.5$ µH. A near commercially available inductor value is $L = 330$ µH, e.g., the inductor 2218-H-RC from Bourns Inc. Figure 6 makes evident that $L = 330$ µH provides a stable operation of the circuit for $\frac{di_L}{dt} \leq 10$ mA/µs.

Then, the inductor current ripple is calculated from Equation (43) for the desired switching frequency; Figure 10 shows the current ripple produced by different inductor values. It is observed that the commercially available $L = 330$ µH produces a current ripple of 220.4 mA, which corresponds to the 7.35% of the maximum inductor current $\max(i_L) = \max(i_{dc}) / (1 - d)$. This current ripple is acceptable in terms of the small-ripple approximation [43]; hence, the inductor value $L = 330$ µH is selected for this example. Nevertheless, smaller current ripples are achievable by increasing the inductor but without exceeding the limit imposed by $\frac{di_L}{dt} = 5$ mA/µs.

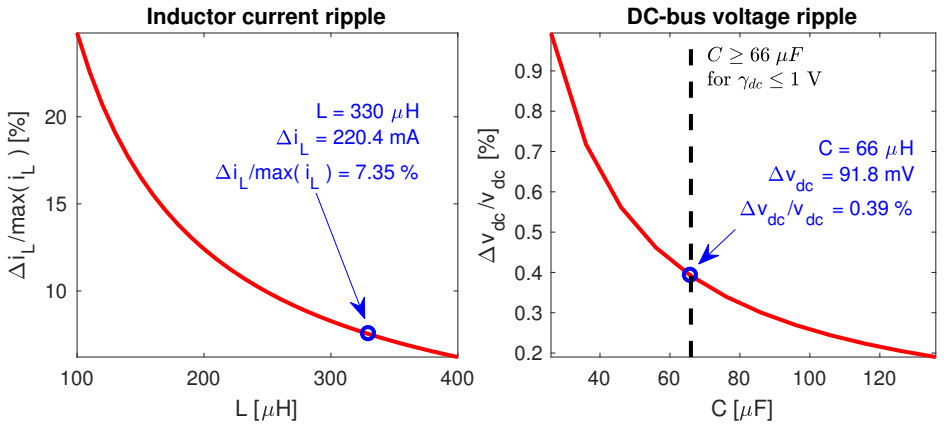


Figure 10. Inductor current ripple for different inductance values (**left**) and DC-bus voltage ripple for different capacitance values (**right**).

The second step is to design the DC-bus capacitance to fulfill the maximum overvoltage value $\gamma_{dc} = 1$ V. The minimum value of the capacitance $C = 66$ µF ensuring $\gamma_{dc} = 1$ V is calculated from Equation (57). This is confirmed in Figure 8, which shows that any capacitor higher than 66 µF will ensure $\gamma_{dc} < 1$ V. Another characteristic to be evaluated is the voltage ripple in the DC-bus, which depends on C as reported in Equation (45). Figure 10 reports the voltage ripples in the DC-bus for multiple values of C, where the minimum capacitance $C = 66$ µF produces a voltage ripple of 91.8 mV (0.39% of the nominal DC-bus voltage). This small voltage ripple is acceptable in terms of the small-ripple approximation [43].

The capacitance tolerance is not mandatory to be considered because the DC-bus design is performed in the worst case. Nevertheless, the capacitor could be increased to introduce a safe margin or to reduce the voltage ripple. For this example, the limit capacitance value $C = 66$ µF is adopted, whose usefulness was already validated in Figure 9: it ensures a DC-bus voltage lower than 25 V for current transients with $\frac{di_{dc}}{dt} \leq -10$ mA/µs. In fact, $C = 66$ µF limits the DC-bus voltage to 25 V even under the occurrence of an unexpected step-like current transient ($\frac{di_{dc}}{dt} \to -\infty$), which could be triggered by the simultaneous disconnection of all the loads from the DC-bus. A commercially available solution is the parallel-connection of two capacitors of 33 µF, e.g., two MKT1820633065 capacitors from Vishay BC Components.

The third step is to calculate the SMC parameters. The design of k_i is given in Equation (23), which provides an automatic adjustment of the SMC to the ESD and DC-bus voltage conditions, as depicted in the implementation of Figure 2. The calculation of k_v is given in Equation (25), which depends on the bus capacitance $C = 66$ µF and desired settling-time $t_s = 2$ ms, resulting in $k_v = 0.132$ A/V for this example.

The final step is to design the hysteresis band H of the switching circuit in Figure 3 to limit the switching frequency. The value of H to ensure a maximum switching frequency of 55 kHz is calculated using Expression (53) obtaining $H = 0.1956$ A. This example adopts $H = 0.2$ A to introduce a small safe margin, which imposes a maximum switching frequency of 53.737 kHz. Finally, the circuital scheme implemented in PSIM, i.e., Figure 4, is configured using those parameters. Figure 11 presents the simulation of the PSIM circuit considering current transients in the DC-bus with amplitudes of 1 A and derivatives equal to $\frac{di_{dc}}{dt} = \pm 5$ mA/µs.

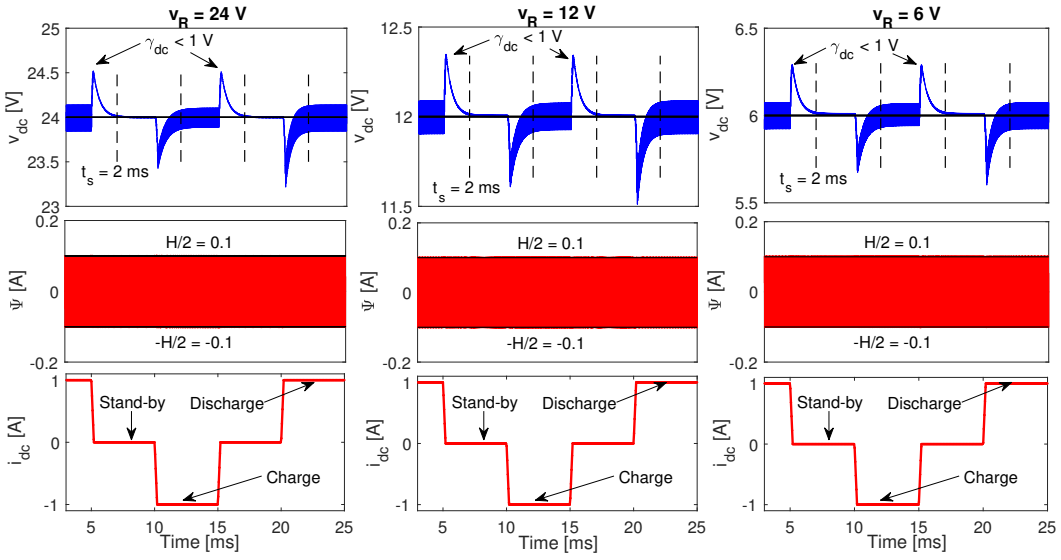


Figure 11. PSIM simulation of the electrical circuit given in Figure 4.

The simulations at the left in Figure 11 consider the DC-bus operating at $V_R = 24$ V, which validates the circuit and SMC design: the DC-bus voltage is correctly regulated to 24 V in all of

the operating modes (charge, discharge and stand-by); moreover, the DC-bus voltage is constrained to ± 1 V around V_R, i.e., the safety restriction $v_{dc} < 25$ V is always fulfilled. This correct behavior is possible because the SMC is always stable. Such a condition is confirmed by the constrained operation of Ψ into the hysteresis band, which also limits the switching frequency. Finally, the DC-bus voltage is restored to V_R after the designed settling time $t_s = 2$ ms in all of the operation conditions.

It must be noted that the design of k_v is independent from the nominal value of the DC-bus voltage. Moreover, k_i is continuously adapted by measuring both the DC-bus and ESD voltages. This robustness of the SMC is also validated in the simulations of Figure 11 by setting $V_R = 24$ V (boost operation), $V_R = 12$ V (Buck–Boost operation) and $V_R = 6$ V (buck operation). The simulations show the same settling time for the bus voltage conditions, which is achieved due to the global stability of the SMC. Furthermore, the overvoltage conditions are always under 1 V because decreasing the DC-bus voltage also decrease γ_{dc}, as reported in Expression (57). Therefore, C must be designed for the higher DC-bus voltage.

In conclusion, the proposed SMC and charger–discharger provide a general solution for interfacing an ESD with the DC-bus of a microgrid. This is achieved by the correct regulation of the DC-bus voltage in Boost, Buck and Buck–Boost conditions.

7. Experimental Implementation and Proof-of-Concept

This section presents the experimental validation of the proposed charger–discharger and SMC. A proof-of-concept prototype was developed as reported in Figure 12.

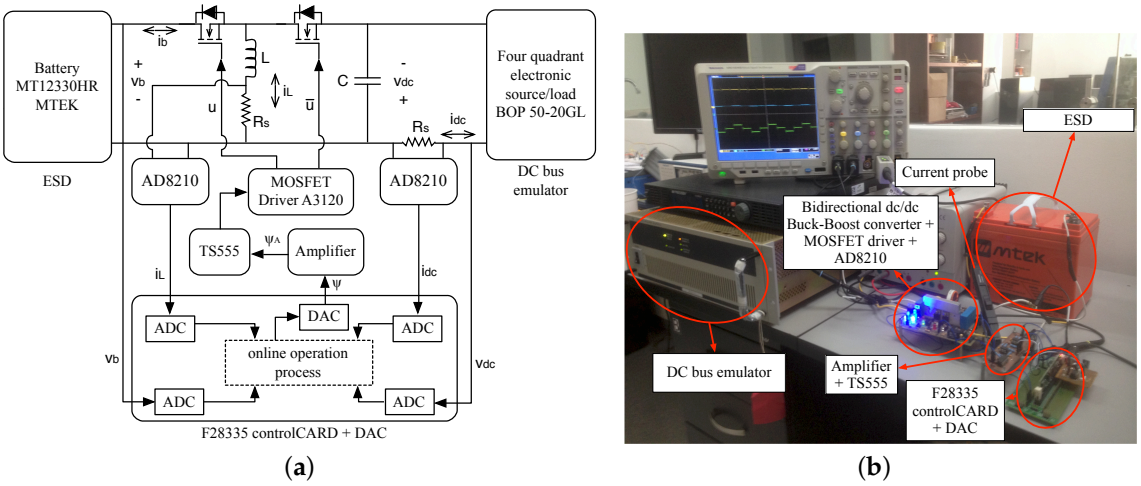


Figure 12. Experimental platform. (**a**) electrical scheme; (**b**) physical setup.

Figure 12a describes the prototype setup. The selected ESD is a 12V battery from MTEK-SA (Medellín, Colombia), while the DC bus is emulated using a four quadrant electronic source/load BOP 50-20GL from Kepco Inc (Flushing, NY, USA). The proposed surface Ψ is calculated using a F28335 controlCARD from Texas Instruments (Dallas, TX, USA) and converted to an analog voltage with a digital-to-analog converter (DAC) MCP4822. Moreover, the switching circuit of Figure 3 is implemented with an amplifier, a TS555 integrated circuit, and an A3120 MOSFET driver.

The bidirectional Buck–Boost DC/DC converter is implemented using an 2218-H-RC inductor from Bourns Inc (Altadena, CA, USA) with $L = 330$ µH, a MKT1813622016 capacitor from Vishay BC (Selb, Germany) with $C = 22$ µF, and two IRF540N MOSFETs from International Rectifier (El Segundo, CA, USA). Furthermore, the inductor and the DC-bus currents are measured using shunt-resistors $R_s = 5$ mΩ and AD8210 amplifiers. These current and voltage measurements are acquired by the controlCARD using the onboard analog-to-digital converters (ADCs). Finally, the physical setup of the experimental platform is shown in Figure 12b.

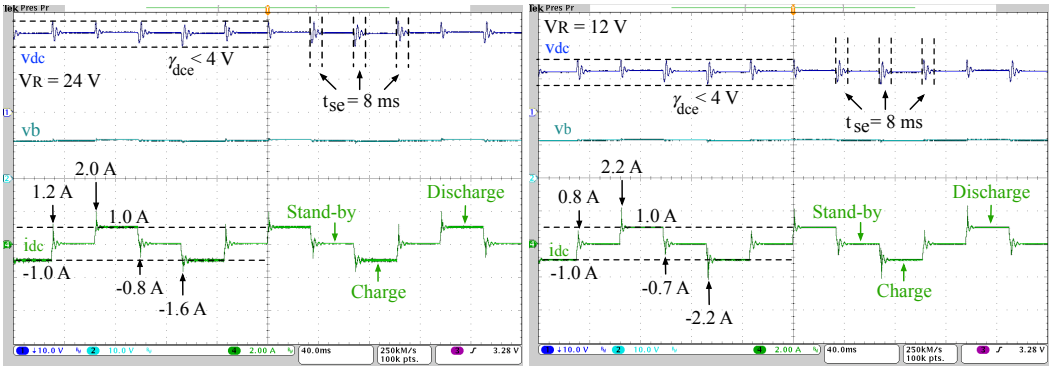
The values of L and C are obtained by following the procedure presented in Section 5 considering the limitations of the experimental setup: $\gamma_{dc} < 2.96$ V, $t_s = 8$ ms, $|\max(i_{dc})| = 1$ A, and $\max(\frac{di_{dc}}{dt}) = \pm 11621$ A/s (± 11.621 mA/µs). Moreover, $H = 0.16$ V is obtained from Equation (53) by defining $\max(F_{sw}) = 52.59$ kHz.

The performance of the proposed solution is evaluated with two experiments, the first one is similar to the simulations presented in Figure 11, and the second one shows the dynamic response of the system for a large change in the operating point.

In the first experiment, the electronic source/load is programmed to reproduce the i_{dc} profiles shown in Figure 11. Three experiments where performed considering the same values of the DC-bus voltage used in Section 6: $V_R = 24$ V, $V_R = 12$ V, and $V_R = 6$ V, with $v_b = 12$ V. However, the electronic source/load is not able to produce i_{dc} steps, as shown in Figure 13, due to its internal dynamic and controllers. The experimental i_{dc} transients exhibit a second-order behavior, whose maximum overshoots are shown in Figure 13a,b, and Figure 13a for $V_R = 24$ V, $V_R = 12$ V, and $V_R = 6$ V, respectively.

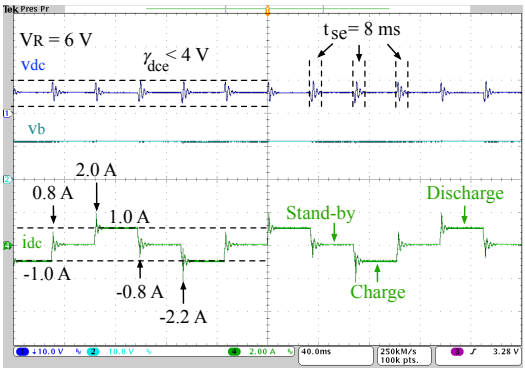
In these experiments, the settling-time (t_{se}) fulfills the design condition $t_s = 8$ ms for the three values of V_R, as shown in Figure 13. However, the experimental maximum deviation of v_{dc} (γ_{dce}) is under 4 V for the three DC-bus voltage values; hence, γ_{dce} is almost 35% higher than the design condition $\gamma_{dc} < 2.96$ V. Such a difference between γ_{dce} and γ_{dc} is produced by the i_{dc} overshoots in the transients, which are between 60% and 120% higher than the i_{dc} value used for the design ($|\max(i_{dc})| = 1$ A): the fourth transient in Figure 13a exhibits a peak value of $i_{dc} = -1.6$ A (60% higher); while the second and fourth transients in Figure 13b and the fourth transient in Figure 13c exhibit peak values of $i_{dc} = \pm 2.2$ A (120% higher). Therefore, experimenting a 35% higher γ_{dce} condition for a 120% higher perturbation in i_{dc} is satisfactory. In conclusion, the results of this first experiment puts into evidence the satisfactory performance of the prototype operating in Boost, Buck–Boost and Buck modes.

The second experiment shows the dynamic response of the prototype during the startup for a 24 V DC-bus in stand-by mode, i.e., the steady-state value of i_{dc} is 0 A. The ESD voltage (v_b) and DC-bus voltage (v_{dc}) waveforms are presented in Figure 14, which shows a correct regulation of v_{dc} at 24 V with a settling-time equal to 8 ms. Once again, the experimental settling-time matches the design value ($t_s = 8$ ms). In this experiment, the overshoot is close to 5 V, which is caused by the large transient in the capacitor current required to charge the capacitor from 0 V to 24 V. This suggests that, in a commercial application, it is required to include a slow-speed bus charge strategy for the startup process. In conclusion, this second experiment shows the accurate settling time imposed by the proposed solution, even for large changes in the operating point, which makes evident the robustness of the solution.



(**a**) (**b**)

Figure 13. *Cont.*



(**c**)

Figure 13. Voltage regulation of the DC-bus for 1 A current steps. (**a**) Boost operation mode with $V_R = 24$ V; (**b**) Buck–Boost operation mode with $V_R = 12$ V; (**c**) Buck operation mode with $V_R = 6$ V.

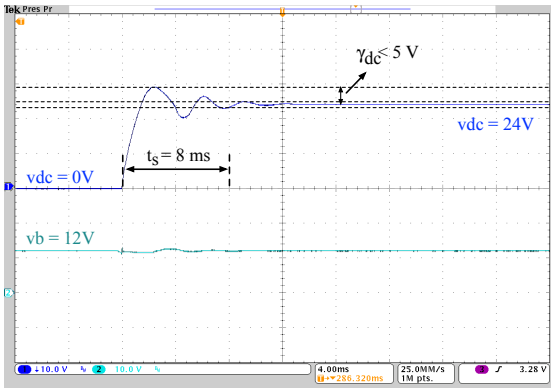


Figure 14. Experimental performance of the proposed SMC.

Finally, those experimental results demonstrate the correctness and usefulness of the proposed SMC and charger–discharger design for DC-bus regulation in microgrids.

8. Conclusions

A system formed by an ESD, a charger–discharger Buck–Boost converter and a DC-bus capacitor has been designed and analyzed. The system includes a sliding-mode controller designed to regulate the DC-bus voltage in both DC and hybrid MGs. On one hand, the use of a Buck–Boost converter allows the connection of an ESD with voltage lower, equal to or higher than the DC-bus voltage, which simplifies the use of commercial ESD systems in MG applications. On the other hand, the SMC provides a robust solution to regulate the DC-bus voltage, which ensures the system stability in the entire operation range of the charger–discharger. Moreover, detailed design and implementation methods for both the SMC and the charger–discharger parameters have been presented.

The SMC and the charger–discharger were designed to fulfill a desired settling time (t_s), a maximum DC-bus voltage (v_{dc}) deviation from the reference (V_R), and a maximum switching frequency (F_{sw}). Such design requirements are fulfilled considering a maximum DC-bus current magnitude ($\max(i_{dc})$) and derivative ($\frac{i_{dc}}{dt}$) for a particular MG application. Simulation and experimental results verify the fulfillment of the design requirements for different perturbations in the DC-bus current, which demonstrates the correct operation of the system in the three operation modes: charging, discharging and stand-by.

Therefore, this single device allows for connecting commercial ESDs to DC-buses with a wide range of voltages. Such a characteristic is ideal for developing commercial ESD management systems.

Moreover, the robust nonlinear control strategy can be easily implemented in inexpensive control cards, e.g., the F28335 controlCARD from Texas Instruments used in this paper.

The main disadvantage of the proposed solution is the unavoidable voltage deviation caused by the Buck–Boost topology after a current transient occurs, even if the correct design of the capacitance constrains the overvoltage condition to safe limits. This overvoltage can be further reduced by adopting a step-up/down DC/DC converter with a second-order filter at the output, e.g., Cuk, Sepic or Zeta converters. However, the complexity of those fourth-order converters require new sliding-surfaces, which is an interesting topic for improving the step-up/down charger–discharger proposed in this paper. Moreover, in the start-up process, the DC-bus must be charged to the nominal voltage without decreasing the state-of-charge of the ESD. Therefore, a start-up routine must be designed to the charge of the DC-bus from the main power sources of the microgrid. Another interesting topic to explore is the use of three-port converters to regulate the DC-bus voltage of an MG. These converters have the possibility to connect an ESD and a DC power source (like a PV generator) with a single converter, which could help to reduce the number and depth of the ESD charging/discharging cycles.

Finally, the proposed design process assumes the current transients' derivatives occurring in the DC-bus are known; however, such information is not commonly reported for the commercial devices that can be connected to a DC-bus (e.g., refrigerators, fans, TVs, computers, light bulbs, etc.), and thus a previous load analysis is required.

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Author Contributions: Carlos Andrés Ramos-Paja conceived and developed the theory of the proposed solution; Daniel González conceived and designed the experiments; Daniel González, Santiago Acevedo and Julián Peláez-Restrepo designed the experimental platform and performed the experiments; Juan David Bastidas-Rodríguez analyzed the data; Carlos Andrés Ramos-Paja, Juan David Bastidas-Rodríguez and Daniel González wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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