JSS Focus Issue on Atomic Layer Etching and Cleaning

Cyclic Etch/Passivation-Deposition as an All-Spatial Concept toward High-Rate Room Temperature Atomic Layer Etching

F. Roozeboom,[a,b,*,z] F. van den Bruele,[b] Y. Creyghton,[b] P. Poodt,[b] and W. M. M. Kessels[a,]**

[a]*Department of Applied Physics, Eindhoven University of Technology, 5600 MB Eindhoven, Netherlands*
[b]*TNO, High Tech Campus 21, 5600 AE Eindhoven, Netherlands*

Conventional (3D) etching in silicon is often based on the 'Bosch' plasma etch with alternating half-cycles of a directional Si-etch and a fluorocarbon polymer passivation. Also shallow feature etching is often based on cycled processing. Likewise, ALD is time-multiplexed, with the extra benefit of half-reactions being self-limiting, thus enabling layer-by-layer growth in a cyclic process. To speed up growth rate, spatial ALD has been successfully commercialized for large-scale and high-rate deposition at atmospheric pressure. We conceived a similar spatially-divided etch concept for (high-rate) Atomic Layer Etching (ALEt). The process is converted from time-divided into spatially-divided by inserting inert gas-bearing 'curtains' that confine the reactive gases to individual injection slots in a gas injector head. By reciprocating substrates back and forth under such head one can realize the alternate etching/passivation-deposition cycles at optimized local pressures, without idle times needed for switching pressure or purging. Another improvement toward an all-spatial approach is the use of ALD-based oxide (Al_2O_3, SiO_2, etc.) as passivation during, or gap-fill after etching. This approach, called spatial ALD-enabled RIE, has industrial potential in cost-effective back-end-of-line and front-end-of-line processing, especially in patterning structures requiring minimum interface, line edge and fin sidewall roughness (i.e., atomic-scale fidelity with selective removal of atoms and retention of sharp corners).
 [DOI: 10.1149/2.0111506jss] All rights reserved.

Manuscript submitted February 2, 2015; revised manuscript received March 13, 2015. Published April 7, 2015. *This paper is part of the JSS Focus Issue on Atomic Layer Etching and Cleaning*.

Today, the continuous doubling of the transistor count on planar microprocessor and memory chips in a two-year cadence has reached the point where Moore's Law (essentially an economic law) and Dennard's scaling (transistor and pitch dimensions) have approached their limits in 2D-scaling. The end of the planar device era was marked with the introduction in 2011 of the 22-nm Tri-Gate device.[1,2] Figure 1 shows its design with gates surrounding the channel on three sides of vertical fins to improve gate delay.

Today, at the emergence of the 10-nm technology node and the 50th anniversary of Moore's Law, 3D device and integration solutions are being rapidly introduced both intra-chip, e.g., Gate-All-Around,[3] vertical NAND,[4] and inter-chip, e.g., 3D Through-Silicon Vias (TSVs).[5]

History of 3D etching.— Whereas the transistor design has been planar for most of its history, its periphery has been subjected to 3D design early on. One of the earliest 3D concepts has been the basic invention of 3D TSVs, already filed in 1958 by the famous W. Shockley,[6] cf. Fig. 2. Yet, in reality 3D Through-Silicon Via (TSV) technology took decades to accelerate the now rapidly growing stacked-chips and micro-electromechanical systems (MEMS) markets by enabling their interconnection in a 3D-integrated System-in-Package (i.e. the so-called '*More than Moore*' domain). Today, the mainstream industrial technology for etching of both TSV and MEMS structures is ion-assisted etching or (Deep) Reactive Ion Etching. This method has become so favorite since it encounters hardly any temperature dependence.[7]

The first 3D architectures in functional transistor design were launched in the 1980s, starting with the introduction of stacked and trench capacitors in NMOS-based memories. Until then the capacitors were designed on the real estate available between the transistor cells. Only in the last decade with the onset of the third era of scaling, i.e. the '*More Moore*' domain,[8] 3D integration has become pivotal in advanced semiconductor manufacturing. Next to cost reduction the other drivers are the reduced form factor and increased performance, such as reduced RC delay and low power consumption, all together enabling new applications in connectivity, mobility and the Internet of Things.

Plasma etching as key enabling technology.— The major challenges in plasma etching of 3D semiconductor devices and of MEMS devices have been reviewed in two recent reviews.[7,9] For the former devices these challenges were reformulated in this journal by Intel into opportunities for ALD and ALEt.[10] Today, atomic-scale deposition and etching of new functional materials are already being implemented in the most advanced transistor, interconnect and patterning technologies. The latest state-of-the-art examples here are in spacer-defined patterning,[11] 3D FinFET and vertical NAND technology with their extremely narrow fins, lines and gaps to create and to fill with ultrahigh fidelity and at acceptable cost.

The obvious distinction of conventional CVD and plasma etching from their *layer-by-layer* counterparts ALD and ALEt is illustrated in Fig. 3. In conventional etch and deposition the process is non-interrupted, and the main reactants are supplied simultaneously, then chemisorbed at the surface where they react and, likewise, the by-products are purged or pumped simultaneously. Also if plasma deposition or etching is done in pulsed mode the reactants are usually still fed simultaneously and in synchronous pulsed mode. The invention of ALD by Aleskovskii,[12] and Suntola and Antson[13] in the 1970s is based on the alternating *time-separated* supply of reactant precursors and their co-reactants, and their respective purging in between. The fact that ALEt was invented a decade later[14] indicates that its realization as the cyclic etching counterpart of ALD is not straightforward.

For a full description of the similarities and differences between ALD and ALEt we refer to the extensive comparison elsewhere in this journal's focus issue.[15] We suffice by resuming the main distinction of ALEt from conventional plasma etching: ideally, ALEt removes only one atomic (sub)layer from the parent material per basic adsorption-purge-activation-purge cycle. In conventional etching, even with fast (i.e. sub-second) plasma pulsing and synchronous gas dosing the depth of the reactive boundary region is less controlled, and the material damage and removal still extends over several monolayer distances.[16]

A major challenge in (cycled) plasma etching is the long cycle time (order: 1–10 sec up to ~1 minute) and the resulting slow etch rate (in DRIE typically 3–5 μm/min) due to the relatively low gas

*Electrochemical Society Fellow.
**Electrochemical Society Active Member.
[z]E-mail: f.roozeboom@tue.nl; fred.roozeboom@tno.nl

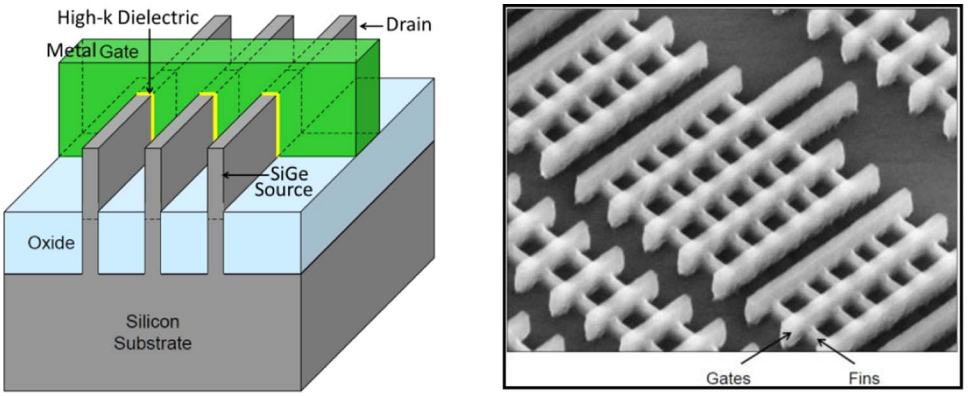

Figure 1. Schematic and SEM image of Intel's 22-nm logic thin gate transistor. After Ref. 2.

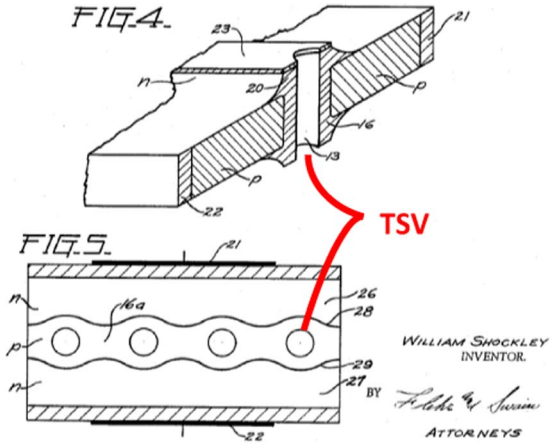

Figure 2. TSV structures proposed in Shockley's original patent. After Ref. 6.

pressures used in the half-cycles.[17,18] This work lays down the concept of cyclic etch /passivation-deposition processing in an all-spatial regime that could lead to high rate (D)RIE and ALEt processing. A part of this work has been filed and published earlier.[19,20] The principle was conceived from an inspiring mix of facts, old and new:

1. The similarity of ion or neutral beam-assisted etching[21] and deposition,[15] and the benefits of plasma-enhanced ALD.[22]
2. Other remarkable similarities between ALD and ALEt both in full and selective area processing.[15]
3. The similarity between time-multiplexed etch/sidewall passivation sequencing in (D)RIE and the sequencing of precursor(s) and co-reactant(s) in ALD and ALEt, and also the duration of these cycle times (∼a few seconds).[20]
4. The concept of spatial Atomic Layer Deposition (ALD) has been commercialized for large-scale and, notably, high-rate film deposition at atmospheric pressure.[23,24] See Fig. 4 for the principle. Atmospheric plasma deposition and related processing becomes more and more popular as it has potential for very high processing rates that are suitable for industrial applications.[25]
5. The use of SiO_2 and SiO_xF_y as more effective self-terminating sidewall protection layers, replacing hydro-fluorocarbons in high-speed oxygen-pulsed deep silicon etching.[26] Similarly, in Si-fin etching the need for a 'tougher' material with stronger sidewall adsorption and passivation than CHF_3 was expressed in order to obtain better retention of sidewall shape (i.e. less striations) and smoother line edges.[27]

   In this context one has recently considered the use of an ALD oxide passivation step in DRIE of high aspect ratio nano-size features, although no experimental data have been shown.[28]
6. In both shallow and through-wafer etching ALD-grown Al_2O_3 hard masks have been reported to show extremely high

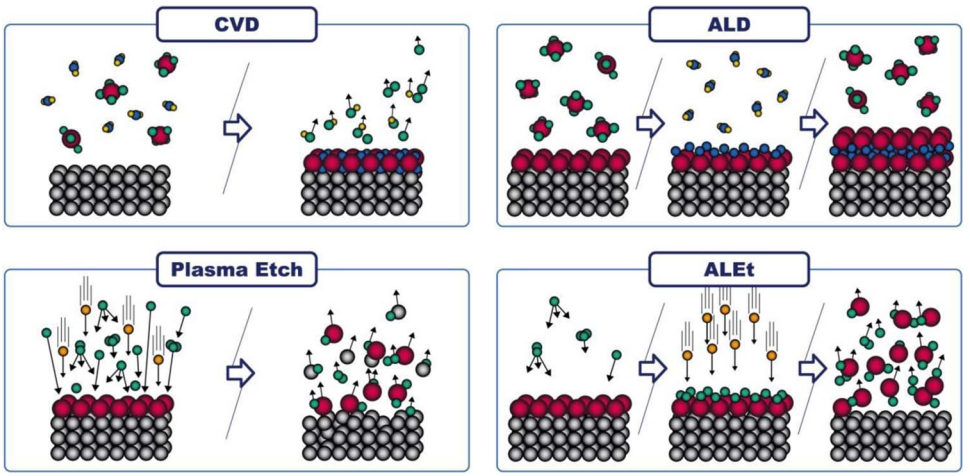

Figure 3. Schematic of conventional CVD and plasma etching and their *layer-by-layer* counterparts, ALD and ALEt. ALEt is cycled between modification by chemisorption of a reactant at the surface and, subsequent volatilization of, ideally, one (sub)monolayer by irradiation with an energetic beam or reaction with a co-reactant. For simplicity reasons the etch processes (bottom pictures) are cartooned in plasma-assisted mode, and the deposition processes (top pictures) in thermal mode. The latter two could be plasma-assisted as well. In the conventional processes (CVD and Plasma etch) the chemical reactants are supplied simultaneously and non-interrupted, and in the layer-by-layer processes (ALD and ALEt) they are alternated.

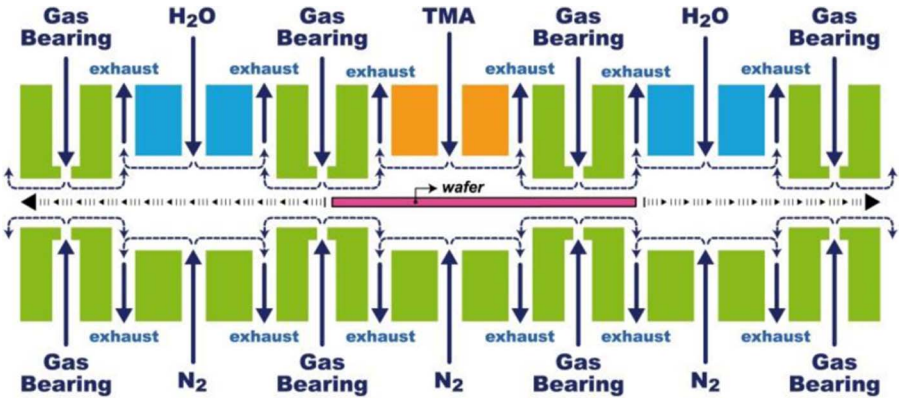

Figure 4. Schematic representation of spatial ALD: a wafer moves horizontally back and forth under spatially divided and confined reaction zones. Arrows pointing upwards indicate exhaust lines. Notice the difference in height of the gas bearing compartments (typically ∼20 to 100 μm) and the deposition compartments (typical height a few mm, and lengths and widths of order ∼1-10 mm).

selectivity (up to 66,000 w.r.t. Si), combined with good surface quality.[29,30] This applies to both deep etch applications in back-end-of-line processing (BEOL) and in shallower etching in front-end-of-line processing (FEOL).

7. Characteristics inherent to reactive ion etching are the initial mask undercut, aspect ratio dependent etching (ARDE) rate, and notching at dielectric interfaces.[31] This is because any etching with SF_6 remains in fact semi-isotropic and proceeds mainly by the non-directional neutral species (radicals), with less than 0.1% of the plasma species being ions causing the directional etching. In addition, pulsed etching with its alternation of etch and passivation pulses suffers from more imperfections.[32] Most prominent for Bosch-type etching is the corrugation ('*scalloping*') of the sidewall, especially for longer etch pulses; see Fig. 5a.

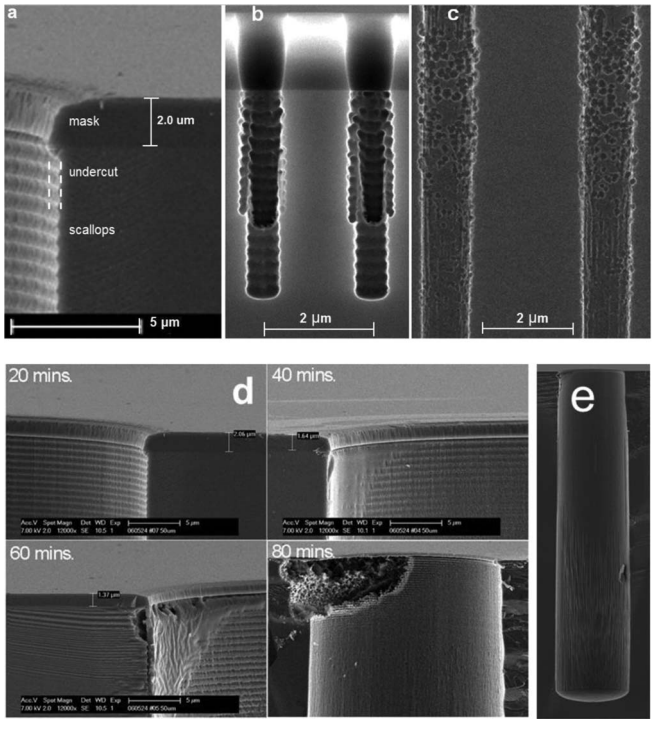

Figure 5. Non-ideal characteristics of the Bosch process: a) mask undercut and scallops, b) striations due to partial hard mask retraction, c) mouse bites due to poor passivation control, d) different stages in time during the creation of a mouse-bitten collar at a via top caused by different stress properties at the intersection of a top SiO_2 hard mask and a fluorocarbon sidewall passivation, and e) vertical striations in the sidewall due to improper passivation. Reprinted with permission from Ref. 33. Copyright, 2008, Wiley-VCH Verlag.

Yet, more defects are encountered, and this is due to the fact that the passivation by plasma C_4F_8 is also an isotropic radical-driven process, leading to non-uniform sidewall passivation and, consequently, sidewall roughness (mouse bites and striations).Some of these features are displayed in Fig. 5, and have been explained elsewhere.[33] Methods to suppress these effects have been discussed but from a chemical or mechanical point of view the fluorocarbon mask material remains not an as silicon compatible passivation as for example SiO_2, Al_2O_3, etc. This holds also for continuous etch processes using halogen-type or mixed O_2/halogen-type chemistries.

8. The need for ultrafast gas switching (<200 ms) and smaller single-wafer etch chamber volumes in both pulsed deep etching and precise layer-by-layer etching.[34] These are measures to match the split-second time constants of many basic chemical half-reactions (also present in ALD processing[35,36]) and to minimize the gas residence time and thus the dose of reactants that are used in one cycle, but are undesired in the next cycle.[17]
9. Methods that have been described for filling high-aspect-ratio features, in which compatible deposition and etching steps are alternated using high-density plasma chemical vapor etch-enhanced (deposition-etch-deposition) gap fill processes.[37]
10. The need to tune the directionality (i.e. ion angular distribution) and to narrow down the ion energy distribution function for etching and filling of refined feature shapes with maximum degree of fidelity by pulsed waveform biasing.[38,39] Interestingly, and seemingly controversial, this also includes the need for tunable plasma process parameters to initiate *isotropic* desorption from and volatilization of the surface independent of its local orientation.[10,15]
11. The development of dedicated (micro)plasma sources in general[40] and atmospheric pressure sources in particular to increase throughput, deposition rate and to reduce process temperature and gas consumption.[25,41]

Each of these facts has its own challenges and potential (sub)solutions. Yet, many of them are connected to the spatial concept approach in this paper. We have only evaluated a few aspects, but valuable ones to assess the feasibility of an all-spatial concept of cyclic etch/passivation-deposition toward high-rate room temperature Atomic Layer Etching.

Below we start with depicting the transition from the conventional temporal Bosch process into a spatial process. This is then followed by replacing the conventional fluoro-hydrocarbon passivation by ALD oxide, and some preliminary experiments in spatial atmospheric pressure ALD in challenging 3D features. This is followed by a section with some modeling background in spatial RIE reactor design, a section on timescale analysis for convection, diffusion, deposition and mass supply, and finally a section on microplasma sources, with some details on the Dielectric Barrier Discharge source that we developed. We conclude with a short outlook.

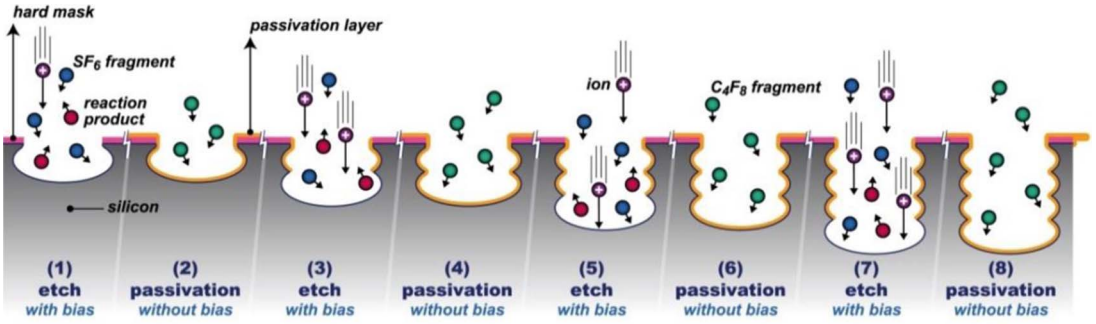

Figure 6. Conventional Bosch etch process scheme for etching silicon with a pre-patterned hard mask atop, using alternating etch and passivation half-cycles.

Spatially-Divided Reactive Ion Etching: A New Concept

The technology mainstay for conventional DRIE is the so-called Bosch process. This room temperature process, illustrated in Fig. 6, consists of two alternating half-cycles[42,43]: 1) etching with SF_6 plasma, and 2) passivation of the sidewalls and bottom of the etched features with a protecting -$(C_2F_4)_n$- fluorocarbon (Teflon-like) polymer liner deposited from plasmas containing etch gases as C_4F_8,[33] C_5HF_7, or alike.

The first half-cycle is an ion-assisted isotropic etch step with SF_6 plasma. If non-interrupted, it would proceed mainly by the non-directional fluorine containing radicals which form volatile SiF_x products that are pumped off. In order to minimize the lateral etching component the etch steps are quickly interrupted by C_4F_8 passivation steps. During each etch step a bias voltage is applied to the substrate holder. This causes a directional physical ion bombardment from the plasma onto the substrate which sputters the polymer off the feature's bottom part and leaves the sidewall passivation intact, thus enabling the anisotropic etching.

The etch and passivation cycle times are each typically 1–10 s with 0.1–1 μm etched per cycle. The process enables plasma etching of deep vertical microstructures (aspect ratios AR ≥ 20:1) in silicon with etch rates of typically 3–5 μm/min, and selectivities up to ∼200:1 against a hard oxide mask (usually SiO_2).[7,18]

An accelerated etch alternative is to convert the above process from its temporal (i.e. *time-separated*) into the *spatially separated* regime.[19,20] The spatial separation can be accomplished by inert (e.g., N_2) gas bearing 'curtains' of heights down to ∼100 μm, or even smaller; see Fig. 7. The gas curtains confine the reactive gases to individual (often linear) injection zones constructed in a gas injector head. The etch and passivation compartments are connected through a gas bearing envelope that is narrow enough (∼1 mm) and pumped differentially to sustain the pressure differences. Thus, pressures can be chosen differently, and can be increased to an optimum in the etch and in the passivation zone. By horizontally moving the substrate back and forth under the multiple injector head one can create the alternate exposures needed to complete the overall cycle. The optimum pressure in each injection slot is obtained by balancing the various gas flows which are injected into and exhausted from the slots, and by a proper design of the distance between the various slots and the gas bearing gap height (a smaller gap causes a larger pressure field gradient between the channels).

The Passivation Step in Spatial RIE: ALD-Based, Low-Pressure or Atmospheric

The selected mask material generally affects etch rate, undercutting, and surface quality of etched features.[44] Oxidic ALD-deposited hard masks like Al_2O_3 are reported to have lower pinhole density and thus higher etch selectivity than conventionally deposited etch hard masks.[29,30] Thus a further improvement in the spatial approach can be expected from the replacement of the CVD-based C_4F_8 passivation cycles by spatial ALD-based deposition cycles of SiO_2, or other oxides (e.g., Al_2O_3). Figure 8 illustrates the schematic configuration of this concept which now consists of a spatial ALD oxide passivation module in an all-spatial etch-passivation cluster concept.

Unlike the C_4F_8 case ALD-based passivation layers are self-limiting and chemisorptive of nature, and less complex in their layer thickness control. This will lead to improved control of the anisotropy and sidewall smoothness in the total DRIE process.

The idea of using temporal ALD passivation in DRIE of high aspect ratio features was conceived recently,[28] yet without any experimental data given. Dingemans et al.[36] published a time-efficient plasma-assisted process for low-temperature (50–400°C) *temporal* ALD of SiO_2 using $H_2Si(N(C_2H_5)_2)_2$ precursor and O_2-plasma. Precursor dosing times as short as ∼50 ms were sufficient to obtain a high conformality (95 ± 5%) in high aspect ratio (30:1) trenches, as shown in Fig. 9a. This indicates that the recombination of O-radicals in such trenches plays no dominant role as was also discussed recently by Knoops et al.[45]

We found that a non-plasma *atmospheric* spatial ALD alternative for oxidic passivation is also possible. Figure 9b shows such an Al_2O_3 layer deposited from trimethyl aluminum and water vapor during 600 repeated cycles of 13.5 ms each in the rotary atmospheric ALD reactor described earlier.[23] The layer has good step conformality (≥ 80%) in trenches with ultrahigh aspect ratios exceeding 130:1. Atmospheric ALD of Al_2O_3 has already successfully been commercialized for the solar cell industry in equipment that deposits films almost two orders of magnitude faster than in conventional (temporal) ALD.[24]

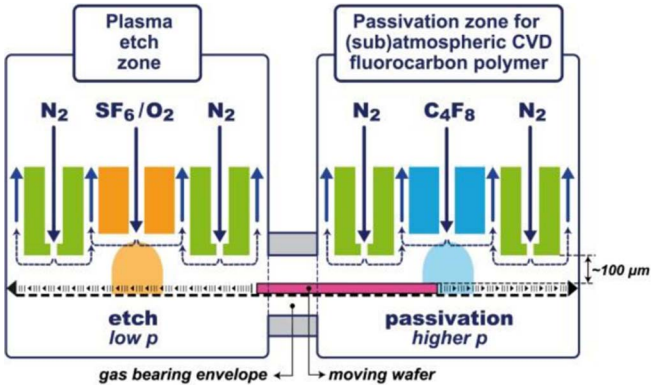

Figure 7. Schematic of spatial RIE process mode with C_4F_8 passivation of a wafer that reciprocates under spatially divided reaction zones. Arrows pointing upwards indicate exhaust lines. Notice the difference in height of the gas bearing compartments (typically ∼20 to 100 μm) and the plasma compartments (typical height ∼10 mm, and length of several 10 mm's and width of order ∼1 mm). The compartments are connected through a gas bearing envelope. Not to scale; wafers will pass the entire zones before shuttling back.

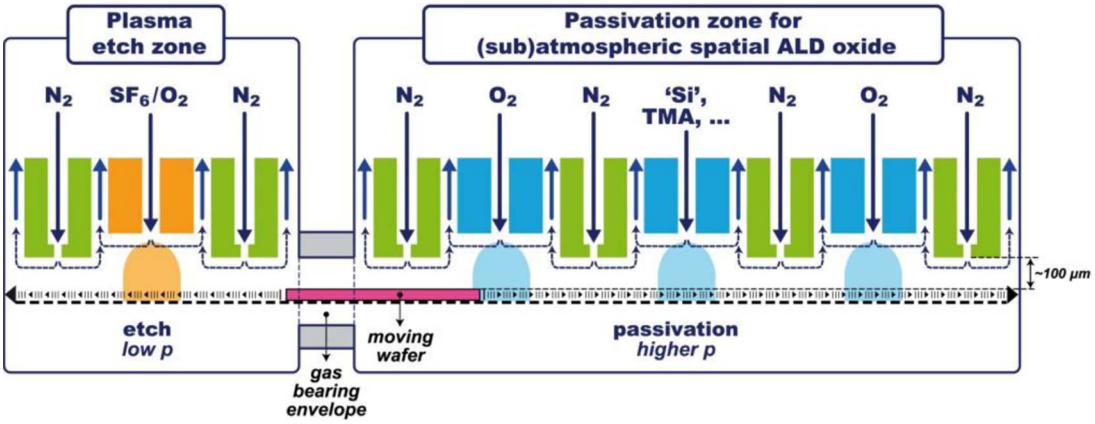

Figure 8. Schematic of alternative all-spatial RIE process mode with spatial ALD oxide passivation (e.g., SiO_2, Al_2O_3, ..). 'Si' denotes a Si-precursor, TMA is trimethyl aluminum. Note, that for deep etching and for shallow ('*layer-by-layer*') etching the wafer exposure times in the respective zones will differ, which will imply different residence times, or different numbers of unit cells in the two main compartments.

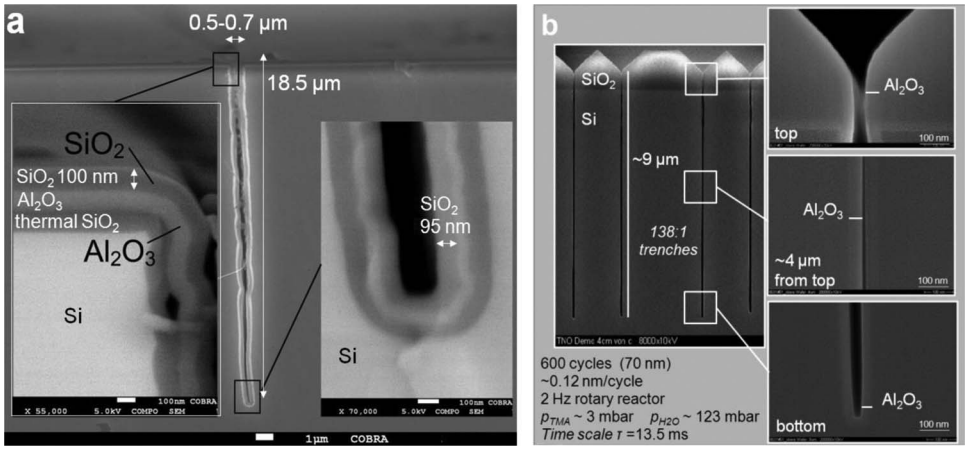

Figure 9. SEM images of deep silicon trenches lined with ALD oxide layers: a) a temporal plasma ALD SiO_2 layer deposited at low-pressure in trenches with aspect ratio ~30:1 during 830 cycles on top of a temporal ALD Al_2O_3 /thermal SiO_2 layer stack inside. Note, that the wavy appearance of the full trench is due to a sample cleaving artefact. After Ref. 36. Copyright, 2012, Electrochemical Society. b) an Al_2O_3 layer deposited at 1 atm. and 200°C in 138:1 aspect ratio trenches during 600 cycles in a rotary spatial ALD reactor. (Trenched wafers kindly provided by Fraunhofer CNT/Namlab, Dresden). Note: in an actual DRIE application as in Fig. 15, the passivation would require only a few ALD cycles (i.e. monolayers of Al_2O_3 or SiO_2).

We also investigated plasma-assisted atmospheric spatial ALD of SiO_2 using the same $H_2Si(N(C_2H_5)_2)_2$ precursor (SAM.24, from Air Liquide) as described above and a plasma source based on a proprietary Surface Dielectric Barrier Discharge (SDBD) concept[46] that was designed in-house and installed in the rotary atmospheric ALD reactor as schematically depicted in Fig. 10. Being operated at high voltage (5 kV) and in the 10–100 kHz frequency range, this type of source provides a highly homogeneous plasma even at atmospheric pressure. The thin plasma region has a thickness of typically 20–50 µm and is principally oriented in parallel with the substrate. The dimensions of this plasma region are 0.5 mm in width and 30 mm in length. The plasma is generated in a reproducible manner in any gas mixture. In this example a gas composition of 10% O_2 in N_2 has been used.

Figure 11 shows a few preliminary micrographs of an array of trenches with aspect ratio 20 : 1 filled with silicon dioxide grown at 50°C during 259 cycles of 65 ms each in the rotary atmospheric pressure spatial ALD reactor. The step conformality of 70% is not

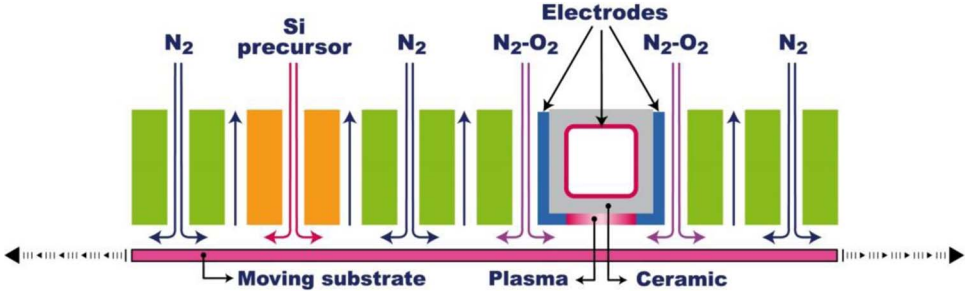

Figure 10. Schematic of atmospheric pressure plasma-assisted spatial ALD reactor with a Surface Dielectric Barrier Discharge plasma source used to deposit SiO_2.

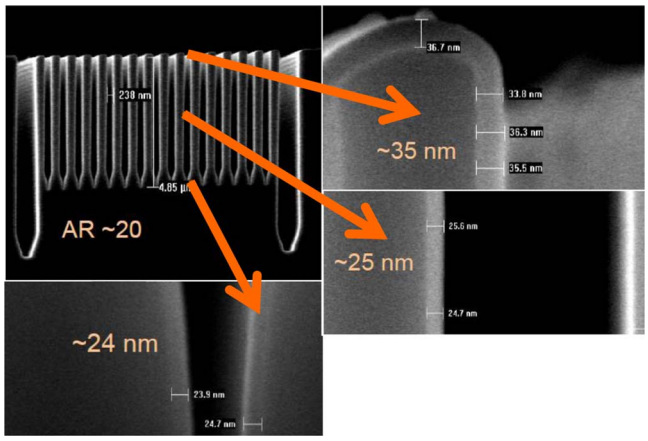

Figure 11. Cross-section SEM images of silicon trenches with aspect ratio ~20:1 lined with an SiO_2 film deposited during 259 repeated cycles of 65 ms each with atmospheric plasma-assisted spatial ALD during cycles at 50°C and 0.4 Hz rotation speed in a rotary ALD reactor provided with an SDBD-plasma source operated at 5 kV and 58 kHz.

optimum, but based on the temporal ALD results shown in Fig. 9a one can expect that this can be further improved.

The deposition results above open up the way to further development of ultrafast atmospheric passivation in RIE. This would not only simplify and accelerate etching, but also reduce costs, for example with sub-second passivation cycles with Al_2O_3, or SiO_2.

Background on Spatial RIE Reactor Design

The basics of an all-spatial RIE process scheme have been illustrated in Fig. 8. Figure 12 gives an impression of the basics in spatial reactor gas inlet design: a wafer is moving under a (plasma) injector head with inlets for etch gas (SF_6/O_2), bearing gas (N_2) and passivation/deposition gas (conventional C_4F_8 or ALD oxide). Typical pressures p_e, p_p and p_{pu} assumed for the etch, passivation/deposition and purge zones, respectively, and the corresponding flow rates Φ_e and Φ_p, lengths L_e and L_p and heights H_e, H_p and H_g of the injection zones are listed in Fig. 12. H is a convenient design parameter to obtain the desired pressures. The pressure drop over each channel is inversely proportional to the cube of its compartment height ($\Delta p \sim H^{-3}$), and linear in L and Φ. Depending on the pressures needed for the spatial RIE process one can calculate the different dimensions of the bearings. An example for low-pressure RIE is shown in Figure 12, indicating these dimensions to be in the mm to sub-mm range. Note, that the pressure for passivation, p_p, is taken to be one order of magnitude higher than the pressure p_e for etching. The relation used is:

$$\Delta p = \lambda \cdot \frac{L}{D_h} \cdot 1/2\rho U^2$$

Here, λ is the friction coefficient, L the length, D_h the hydraulic diameter (which is almost equal to H) and U the flow velocity. The flow velocity is inversely proportional to H which leads to the conclusion that Δp is *inversely* proportional to H^3. Thus the energy of the fluorine ions from the etching plasma will be higher than that for any ions attracted from the passivation plasma (more collisional losses for F-ions in case of C_4F_8 passivation or oxygen ions in case of oxide ALD passivation). Therefore, in an entirely spatial process with non-interrupted voltage biasing of the full substrate, the ion bombardment of the passivation layer will be sustained during the etch half-cycle.

Timescale Analysis for Convection, Diffusion, Deposition and Mass Supply

In order to further optimize the spatial SF_6/O_2 etch and SiO_2 deposition process parameters preliminary gas transport simulations were performed to analyze all relevant timescales involved. The simulation program used is a general purpose CFD model CVD-X developed to predict and optimize deposition processes in the semiconductor industry.[47] In this program specific models for the description of rarefied gas transport inside trenches have been incorporated. Using these models, transient multi-scale simulations have been performed of flow, precursor transport and deposition reactions in ALD-type reactors filled with high aspect ratio trenched wafers.

A short synopsis of the most relevant formulas involved is given in Table I. For more details on the simulation program one is referred to Ref. 47. The simulations were done for the passivation of a wide range of lateral feature scales. The three main categories of features studied are a) microsystem cavities with 50 µm openings and aspect ratio 5:1, b) 1 µm wide 3D-vias (aspect ratio 10:1, areal density 100/mm^2) and c) sub-micron (0.15 µm) trenches (aspect ratio 10:1, areal density 10^4/mm^2); see Table II.

Figure 13 shows some of the main simulations results. For a typical conventional (D)RIE reactor with ~30 liters volume and the process parameter (flow rates, pressure, temperature) settings of Ref. 36, the relevant process time is dominated by the flushing time scale. This is of the order of seconds (6.12 sec for 90% volume flushed;

Assumptions

Pressures:

p_e = 13 Pa (0.1 Torr)
p_p = 133 Pa (1 Torr)
p_{pu} = 12 Pa
$\Delta p_e = p_e - p_{pu}$ = 1 Pa
$\Delta p_p = p_p - p_{pu}$ = 121 Pa

Flow rates:

Φ_e = 120 sccm
Φ_p = 260 sccm

Dimensions:

L_e = 5 mm
L_p = 5 mm

Requirements

Dimensions:

H_e = 4 mm
H_p = 700 µm

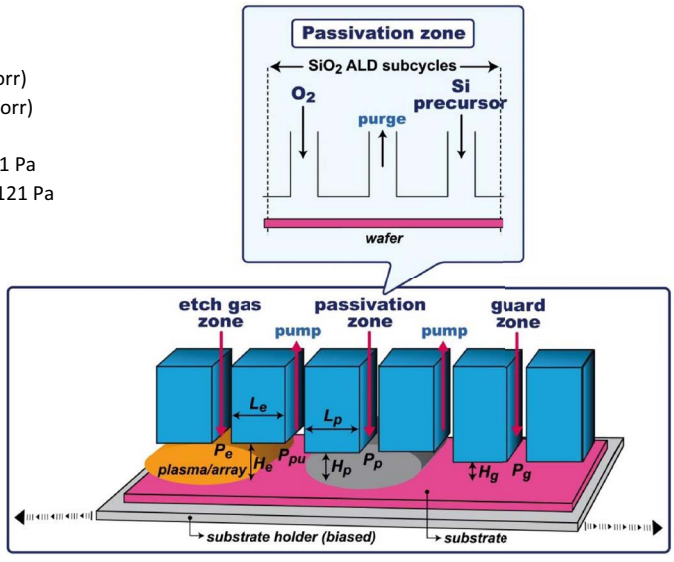

Figure 12. Schematic for modelling the multichannel gas injector head in spatial ALEt, as used for the calculation of the different gas bearing dimensions. The injector contains the etch gas inlet, the passivation gas inlet(s) and an outer guard gas inlet to screen off the ambient atmosphere. All inlets can be separated from each other by purge outlets (drawn) and by bearing gas inlets (not drawn here, but see Fig. 8 for more details). Each gas is injected through an inlet with or without microplasma source. See text for more explanation.

Table I. Formulas used for the timescale analysis of convection, diffusion, deposition and mass supply in the different 3D feature cases, listed in Table II. (a = aspect ratio; A = area). More details in Ref. 47.

Eq. 1. Convection, flushing reactor volume	$\tau_{supply,gas} = \frac{P_{tot} \cdot M_{precursor} \cdot V_{reactor}}{R \cdot \Phi_{tot}}$
Eq. 2. Reactor diffusion	$\tau_{diff,reactor} = \frac{H^2_{reactor}}{D}$
Eq. 3. Trench diffusion	$\tau_{diff,trench} = \frac{L^2_{trench}}{D_{Kn}}$ $\quad D_{Kn} = \frac{4D_{trench}}{3} \cdot C_0$
Eq. 4. Langmuir deposition flat	$\tau_{Langmuir,flat} = \frac{n''_{tot} \cdot R \cdot T}{c_{gs} \cdot f_s \cdot C_0 \cdot P_{precursor}}$ $\quad C_0 = \sqrt{\frac{R \cdot T}{2\pi \cdot M_{precursor}}}$
Eq. 5. Langmuir deposition trenches	$\tau_{Langmuir,trench} = \tau_{Langmuir,flat} \cdot \left(\frac{3}{2}a^2 + \frac{19}{4}a + 1\right)$
Eq. 6. Required mass saturating flat	$\tau_{supply,flat} = \frac{A_{flat} \cdot d_{layer} \cdot \rho_{solid}}{c_{gs} \cdot \left(M_{solid}/M_{precursor}\right) \cdot \Phi_{precursor}}$
Eq. 7. Required mass saturating trenches	$\tau_{supply,trench} = \frac{A_{trench} \cdot d_{layer} \cdot \rho_{solid}}{c_{gs} \cdot \left(M_{solid}/M_{precursor}\right) \cdot \Phi_{precursor}}$

12.25 sec for 99% volume flushed). The calculated optimum saturation time (transition point from the Langmuir-dominated regime to the supply-dominated regime) at 50°C is around 20–50 ms, as shown in Fig. 13a. This corresponds very well with the experimentally determined Si-precursor dosing times for saturation.[36]

The results in miniaturized reaction zones of 2.5 mm height and 5 mm length (in both directions), representative for our spatial reactor dimensions, indicate an optimal pressure range from ∼0.5 Torr for planar structures (Fig. 13a) to ∼5 Torr for TSVs (Fig. 13b) and microsystems (Fig. 13c), at ∼100°C, and 5 - 200 ms timescales depending on the feature's aspect ratio; see Figs. 13b-d.

It is evident that for lower temperatures and higher aspect ratio features the timescales increase (more Langmuir-dominated). Yet, the corresponding timescales for depositing a few passivation monolayers remain typically in the sub-second regime, even at room temperature, i.e. the targeted process temperature for RIE in the spatial regime.

Table II. Dimensions and densities of three characteristic 3D-features used in the timescale analysis of convection, diffusion, deposition and mass supply in spatial DRIE: microsystem cavities with 50 μm openings and aspect ratio 5:1; 1 μm wide 3D-vias (aspect ratio 10:1, areal density 100/mm^2) and sub-micron (0.15 μm, DRAM-like) trenches (aspect ratio 10:1, areal density 10^4/mm^2). Flat wafers are used as a reference.

Feature characteristic	Planar wafer	Microsystems & Sensors/actuators	TSVs	DRAM
Type	-	*MEMS cavities*	*Via hole*	*Trench (pore)*
Diameter/width (μm)	0	50	1	0.15
Depth (μm)	0	250	10	1.5
Aspect ratio	-	5	10	10
Density (number/mm^2)	0	10	100	10^4
Exposed area (%)	0	2	0.008	0.02
Area multiplier	1.0	1.39	1.003	1.007

Considering the mass supply needed in bulk micromachining of silicon (specific density of $5 \cdot 10^{22}$ atoms/cm^3) it will be obvious that the Si-etching half-cycle requires prolonged time intervals. This requirement is the main driving force for the development of high-density plasmas in Si-etching; see the next section.

If, however, the main application is *layer-by-layer* etching of silicon, and dielectric and conductor thin films over moderate silicon topologies, a certain degree of non-directionality is necessary to accomplish isotropic etching of material and desorption of passivation off the sidewalls of the 'shallow' features.[10,15] In this case one may need less directional etch conditions, and higher pressures in combination with dedicated microplasma sources may accomplish this. In the next section we will discuss the general trends in microplasma source design and miniaturization.

Microplasma Sources

Trends in microplasma sources.— The dimensions of the spatial RIE reactor design described above, call for the use of miniaturized plasma sources or arrays. In view of the accelerated etch rate requirements a logical further step is to make the etch cycle proceed at higher pressure, ideally at atmospheric pressure, or at least sub-atmospheric, e.g. 100 mTorr. At higher pressures one can expect higher electron densities (n_e), and correspondingly higher ion and radical formation.[48] Power densities achieved in microdischarges (kW.cm^{-3} to MW.cm^{-3}) are orders of magnitude larger than those in conventional large-scale systems (W.cm^{-3}).[49]

Today, high-density plasma sources are now being designed and explored for utilization as future microplasma sources or arrays. Generally, this research aims at achieving a ∼hundred-fold increase in electron density,[40] beyond the traditional densities of 10^{12} cm^{-3}, or even up to more significant levels,[50] thus enabling high-speed etching at correspondingly higher pressures. The challenge is to avoid increased ion scattering, so that the energy and directionality of the ion bombardment is maintained to combine increased etch rates with good

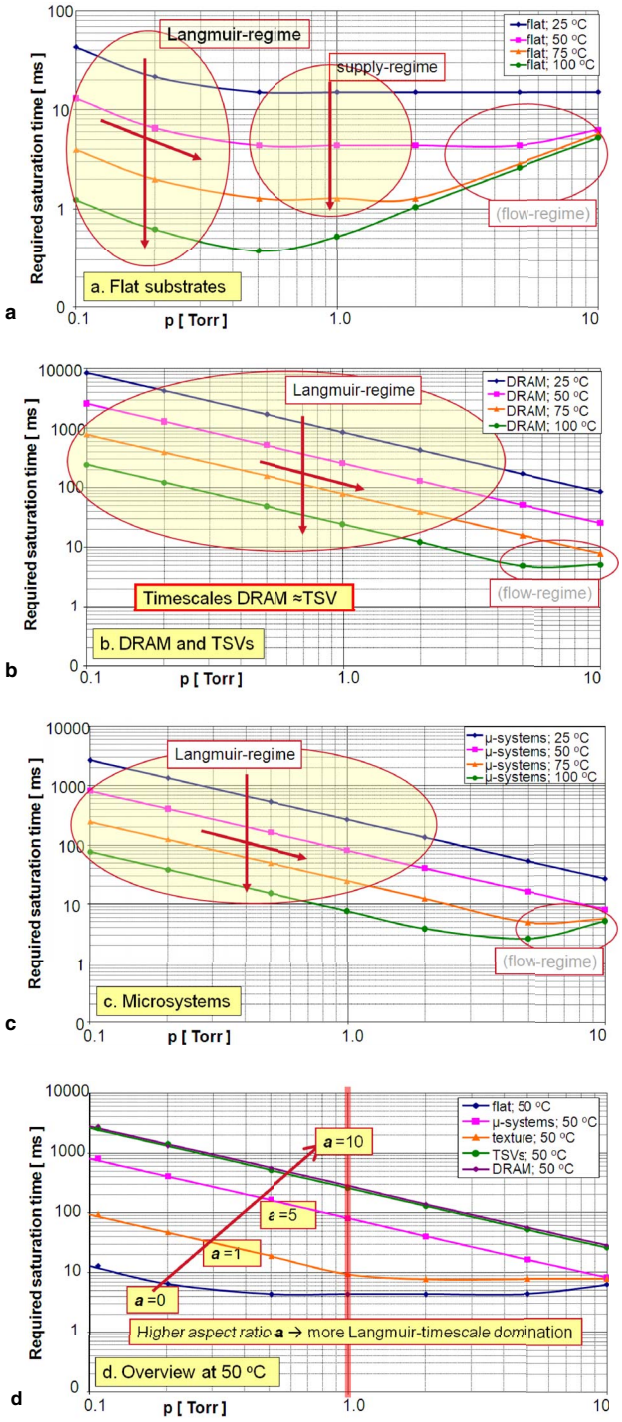

Figure 13. Estimated timescales for optimum saturation on a) planar substrates and on various categories of 3D features with different dimensions and densities (cf. Table II): b) 0.15–1 µm 3D trenches and vias with aspect ratio 10:1, c) microsystems with 50 µm trenches with aspect ratio 5:1, and d) overview at 50°C. Reprinted with permission from Ref. 20. Copyright, 2012, IOP Publishing Ltd.

anisotropy control in 3D Si etching. Figure 14 shows the potential gain in plasma density (n_e) upon miniaturization of ultrahigh-frequency plasma sources in combination with the use of photo-stimulation by UV light sources, or of in-plasma generated photons.

Preliminary SDBD source testing.— The new concept of ALD passivation for RIE in an all-spatial regime can also be combined with microplasma sources replacing the traditional plasma sources. As a

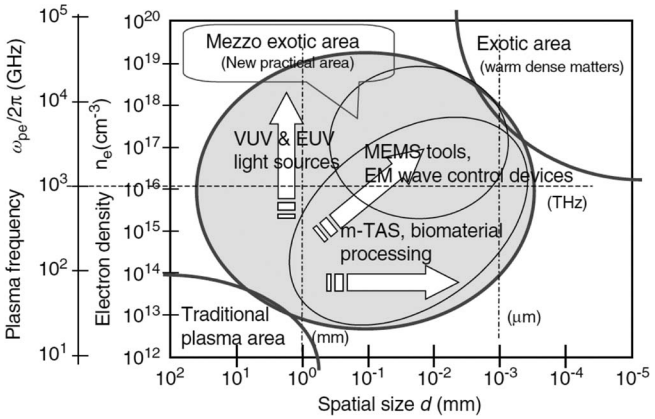

Figure 14. Characteristics of microplasmas in a plane of the spatial size d, the plasma density n_e and plasma frequency. Reprinted with permission from Ref. 40. Copyright, 2006, IEE Japan.

first step we have designed a Surface Dielectric Barrier Discharge microplasma source with a rectangular (0.5 mm wide × 30 mm long) opening for the reactant gas, cf. Fig. 10. It has been tested in a conventional vacuum reactor for its etching behavior at close distances ($\leq$ 20 mm) from an RF-biased Si-substrate with trench patterns pre-etched in a thermal SiO_2 hard mask. The first results obtained are not yet optimized: the maximum Si-etch rate achieved so far was 4 µm/min at only 35 W plasma source power, 10 V substrate bias, 1.2 mbar, 50 sccm SF_6 and 20 mm distance between the microplasma source and the Si-sample.

Next, a preliminary RIE / ALD passivation /RIE cycle was performed on a similar Si-sample in three steps involving two separate non-connected reactor chambers:

1) the vacuum chamber for a 1 min. RIE step using SF_6/O_2 and a surface-DBD source,
2) the rotary spatial atmospheric pressure ALD reactor for the thermal deposition of the Al_2O_3 passivation of only 5 monolayers (5 rotations) under the same non-plasma conditions as described above (Fig. 9b),
3) once more, the vacuum chamber for another 1 min. RIE step.

From the etch profile shown in Fig. 15 one can see two typical scallops on the trench sidewall, and conclude that both directional and lateral etch have been accomplished in a mixed anisotropic/isotropic

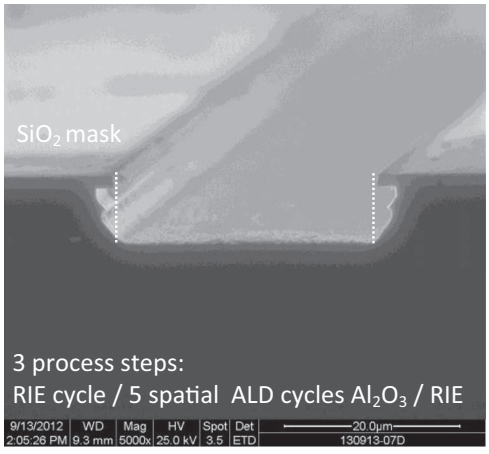

Figure 15. SEM image of trench profile after RIE/ALD passivation/RIE cycle composed of a silicon etch step in a separate vacuum reactor with a surface-DBD microplasma source, followed by 5 cycles of spatial atmospheric ALD of Al_2O_3 in a rotary lab reactor, and finally a second, identical RIE step.

regime where as little as 5 monolayers of Al_2O_3 passivation are sufficient to preserve the shape of the scallop carved out in the first cycle. Another remarkable observation is the flat etch front of the trench bottom. This may be indicative for the robustness ALD-grown Al_2O_3 hard mask, and desired in atomically smooth surface etching in ALEt. In conventional continuous dry etching trench bottoms are often micro-trenched due to ion scattering from the trench sidewalls which results in faster etching of the side corners.[51]

We note that these results have been obtained with non-optimized processing and equipment, so we are confident that further optimization will give further improvements and insights. The process variables are manifold: gas concentration, pressure in the etch and passivation compartments, plasma power, substrate voltage biasing, room temperature processing,[52] plasma source-to-substrate distance, passivation with other spatial ALD oxides like SiO_2.

Concluding Remarks and Outlook

We have described a novel alternative and disruptive concept of Reactive Ion Etching, which converts the conventional time-divided process into the *spatially-divided* regime. The spatial separation is realized by inert gas bearing 'curtains' of heights above the wafers down to ~20 to 100 μm. These curtains confine the reactant gases to individual (e.g., linear) injection slots constructed in a gas injector head. By moving the substrate horizontally back and forth under the head one can expose the wafer to the alternate gases in the overall cycle without the intermittent reactor volume refreshment time delay that occurs upon every cycle.

Spatially-divided Reactive Ion Etching has the potential of yielding higher etch rates in (deep) 3D Si etching and becoming a future high-speed alternative for the conventional Bosch process in cost-effective creation of advanced 3D interconnects (TSVs), MEMS/NEMS manufacturing and related applications.

An additional advantage of the spatial RIE regime is the significant reduction of passivation that settles on (and flakes from) the reactor walls since in this regime no etch or passivation products deposit. Moreover, fluorine-free, thus environmentally friendlier passivation chemicals can be used. When, in addition, the etch process is applied with a uniform ALD-based passivation by SiO_2 or alike rather than with CVD-based C_4F_8-based half-cycles, the anisotropy control and high fidelity pattern transfer can be improved in 2D and in 3D etching. Furthermore, in many FEOL and BEOL flowcharts any future spatial RIE modules can certainly be integrated with or into other spatial ALD-modules or pulsed CVD modules providing cost-effective and low-temperature or gap or via filling with liners,[53] seed/barrier layers,[10] etc.

We note that the concept of spatial RIE etching can be applied in many more demanding application fields such as in the front-end-of-line of the *More Moore* domain. Yet, research will probably first continue with the optimization of current temporal (pulsed) reactor technology, much along the lines described by Cooke[17] and others.[54] Already in today's advanced RIE etching, we witness the steady development of advanced pulsed waveform plasma etching to meet the stringent requirements for further nanoelectronics scaling beyond the 10-nm technology node by better control of the critical plasma parameters such as ion and radical densities, ion energy distribution functions,[38,39] and electron temperature in conventional high-density plasma reactors.[55]

We conclude that today the potential of *ALD-assisted nanomanufacturing* technologies like Atomic Layer Etching (ALEt) concepts derived from etch-purge-passivation/deposition-purge subroutines in (D)RIE and ALD is now clearly being recognized and promoted.[10,54,56,57–59] The ongoing scaling of Moore's Law will soon require the implemention of these complementary technologies to meet the 10-nm challenges in surface and sidewall passivation of resist and feature patterns that is required to minimize interface, line edge and fin wall roughness.[27,60–62] For cost reasons and flexibility in local pressure, i.e. (an)isotropy control, in the spatial etch and purge compartments one can envisage a gradual shift to the adoption of *ALD-enabled RIE* (we abbreviate it as *ALDeRIE*) in the spatial domain as well. Obviously, the spatially divided version is not commercially available yet and not straightforward, but – once realized for dedicated materials and topographies – it will certainly lead to far improved price-performance ratios in Atomic Layer Etching.

Acknowledgment

The authors thank Fraunhofer CNT and Namlab in Dresden for providing the ultradeep trenched wafers that we used for ALD deposition (Fig. 9b). The in-depth discussions with Prof. D.C. Schram (Eindhoven University of Technology) on microplasma source design are gratefully acknowledged.

References

1. C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, *Proc. Symp. VLSI Tech.*, Honolulu, Hawaii, p. 131 (2012).
2. C.-H. Jan, U. Bhattacharya, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai, *Proc. Tech. Dig. Int. Elect. Dev. Meeting*, 2012, paper 3.1.1, p. 44 (2012).
3. K. J. Kuhn, U. Avci, A. Cappellani, M. D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manpatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chau, and I. Young, *Proc. Tech. Dig. Int. Elect. Dev. Meeting*, 2012, paper 8.1.1, p. 171 (2012).
4. A. Goda and K. Parat, *Proc. Tech. Dig. Int. Elect. Dev. Meeting,* 2012, paper 2.1.1, p. 13 (2012).
5. *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, P. Garrou, C. Bower, and P. Ramm, Editors, Wiley-VCH Verlag, Weinheim (2008).
6. W. Shockley, *Semiconductive Wafer and Method of Making the Same*, US Pat. 3,044,909, July 17, 1962.
7. V. M. Donnelly and A. Kornblit, *J. Vac. Sci. Technol. A*, **31**, 050825 (2013), and references therein.
8. International Technology Roadmap for Semiconductors, 2013 edition, Semiconductor Industry Association, 2013 edition; http://public.itrs.net/Links/2013ITRS/Summary2013.htm
9. C. G. N. Lee, K. J. Kanarik, and R. A. Gottscho, *J. Phys. D: Appl. Phys.*, **47**, 273001 (2014).
10. C. T. Carver, J. J. Plombon, P. E. Romero, S. Suri, T. A. Tronic, and R. B. Turkot, Jr., *ECS Journal of Solid State Science and Technology*, **4**, N5005 (2015).
11. Y.-K. Choi, T.-J. King, and C. Hu, *IEEE Trans. Electron Devices*, **49**, 436 (2002).
12. V. B. Aleskovskii, *Zh. Prikl. Khim.*, **47**, 2145 (1974); *ibid*., *J. Appl. Chem. USSR*, **47**, 2207, (1974).
13. T. Suntola and J. Antson, *Method for producing compound thin films*, US Pat. 4,058,430, Nov. 15, 1977.
14. M. N. Yoder, '*Atomic layer etching'*, US Pat. 4,756,794, July 12, 1988.
15. T. Faraz, F. Roozeboom, H. C. M. Knoops, and W. M. M. Kessels, *ECS Journal of Solid State Science and Technology*, **4**(6), N5023 (2015).
16. C. Petit-Etienne, M. Darnon, L. Vallier, E. Pargon, G. Cunge, F. Boulard, O. Joubert, S. Banna, and T. Lill, *J. Vac. Sci. Technol. B*, **28**, 926 (2010).
17. M. Cooke, *ECS Journal of Solid State Science and Technology*, **4**, N5001 (2015).
18. B. Wu, A. Kumar, and S. Pamarthy, *J. Appl. Phys.*, **108**, 051101 (2010).
19. F. Roozeboom, A. M. Lankhorst, P. W. G. Poodt, N. B. Koster, G. J. J. Winands, and A. J. P. M. Vermeer, *Apparatus and method for reactive ion etching*, Pat. application WO 2011/105908, 1 Sept. 2011; US 20130118895 A1, May 16, 2013.
20. F. Roozeboom, B. Kniknie, A. M. Lankhorst, G. Winands, R. Knaapen, M. Smets, P. Poodt, G. Dingemans, W. Keuning, and W. M. M. Kessels, *IOP Conf. Series: Materials Science and Engineering*, **41**, 012001 (2012); F. Roozeboom, B. Kniknie, A. M. Lankhorst, G. Winands, R. Knaapen, M. Smets, P. Poodt, G. Dingemans, W. Keuning, and W. M. M. Kessels, *ECS Transactions*, **50**(32), 73 (2013).
21. J. W. Coburn and H. F. Winters, *J. Appl. Phys.*, **50**, 3189 (1979).
22. H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, and W. M. M. Kessels, *J. Vac. Sc. Technol. A*, **29**, 050801 (2011).
23. P. Poodt, A. Lankhorst, F. Roozeboom, C. Spee, D. Maas, and A. Vermeer, *Adv. Mater.*, **22**, 3564, (2010), and references therein.
24. P. Poodt, D. C. Cameron, E. Dickey, S. M. George, V. Kuznetsov, G. N. Parsons, F. Roozeboom, G. Sundaram, and A. Vermeer, *J. Vac. Sc. Technol. A*, **30**, 010802 (2012).
25. D. Merche, N. Vandencasteele, and F. Reniers, *Thin Solid Films*, **520**, 4219 (2012).
26. H. V. Jansen, M. J. de Boer, K. Ma, M. Gironès, S. Unnikrishnan, M. C. Louwerse, and M. C. Elwenspoek, *J. Micromech. Microeng.*, **20**, 075027 (2010).

27. C. A. Mack, *Proc. of SPIE*, **9189**, 91890D (2014).
28. B. Kobrin and B. '*Method and apparatus for anisotropic etching*', US Pat. application US2010173494 (A1), July 8, 2010.
29. S. Tegen and P. Moll, *J. Electrochem. Soc.*, **152**, G271 (2005).
30. L. Sainiemi and S. Franssila, *J. Vac. Sci. Technol. B*, **25**, 801 (2007).
31. J. Kiihamäki, *Fabrication of SOI micromechanical devices*, PhD thesis, VTT, Finland, 2005. http://www.vtt.fi/inf/pdf/publications/2005/P559.pdf.
32. F. Laermer and A. Urban, *Microelectronic Engineering*, 67, 349 (2003).
33. F. Roozeboom, M. A. Blauw, Y. Lamy, E. van Grunsven, W. Dekkers, J. F. Verhoeven, F. van den Heuvel, E. van der Drift, W. M. M. Kessels, and M. C. M. van de Sanden, in *Handbook of 3-D Integration, Technology and Applications of 3D Integrated Circuits*, P. E. Garrou, C. A. Bower, and P. Ramm, Editors, p. 47, Wiley-VCH Verlag, Weinheim (2008); and references therein.
34. T. Panagopoulos, *Rapid and uniform gas switching for a plasma etch process*, US Pat. 8,133,349, March 13, 2012.
35. P. Poodt, J. van Lieshout, A. Illiberi, R. Knaapen, F. Roozeboom, and A. van Asten, *J. Vac. Sc. Technol. A*, **31**, 01A108-1/7 (2013).
36. G. Dingemans, C. A. A. van Helvoirt, D. Pierreux, W. Keuning, and W. M. M. Kessels, *J. Electrochem. Soc.*, **159**, H277 (2012).
37. B. van Schravendijk and H. te Nijenhuis, '*Atomic layer removal for high aspect ratio gapfill*', US Pat. 7981763, July 19, 2011.
38. S.-B. Wang and A. E. Wendt, *J. Appl. Phys.*, **88**, 643 (2000).
39. M. C. M. van de Sanden, M. A. Blauw, F. Roozeboom, and W. M. M. Kessels, in *Proc. AVS 54th International Symposium*, Seattle, WA (2007).
40. K. Tachibana, *IEEJ Trans*., **1**, 145 (2006).
41. F. Massines, C. Sarra-Bournet, F. Fanelli, N. Naudé, and N. Gherardi, *Plasma Process. Polym.*, **9**, 1041 (2012).
42. F. Laermer and A. Schilp, *Method for anisotropic plasma etching of substrates*, US Pat. 5,498,312, March 12, 1996.
43. F. Laermer, S. Franssila, L. Sainiemi, and K. Kolari, in *Handbook of Silicon Based MEMS Materials and Technologies*, V. Lindroos, M. Tilli, A. Lehto, and T. Motooka, Editors, p. 349, Elsevier, Oxford (2010).
44. M. Boufnichel, P. Lefaucheux, S. Aachboun, R. Dussart, and P. Ranson, *Microelectron. Eng.*, **77**, 327 (2005).
45. H. C. M. Knoops, E. Langereis, M. C. M. van de Sanden, and W. M. M. Kessels, *J. Electrochem. Soc.*, **157**, G241 (2010).
46. Y. Creyghton, P. Poodt, M. Simor, and F. Roozeboom, *Plasma source, surface processing apparatus and surface processing method*, European patent application EP 14173878.1, filed June 25, 2014.
47. A. M. Lankhorst, B. D. Paarhuis, H. J. C. M. Terhorst, P. J. P. M. Simons, and C. R. Kleijn, *Surface and Coatings Technology*, **201**, 8842 (2007).
48. D. C. Schram, *Plasma Sources Sci. Technol.*, **18**, 014003 (2009).
49. F. Iza, G. J. Kim, S. M. Lee, J. K. Lee, J. L. Walsh, Y. T. Zhang, and M. G. Kong, *Plasma Process. Polym.*, **5**, 322 (2008).
50. M. J. Kushner, *A Low Temperature Plasma Science Program: Discovery Science for Societal Benefit*, White Paper to the 2014 FESAC Strategic Planning Panel, August 5, 2014. https://www.burningplasma.org/resources/ref/fspp/whitepapers/LTP_Program_v22_Kushner.pdf
51. S. A. Vitale, H. Chae, and H. H. Sawin, *J. Vac. Sci. Technol. A*, **19**, 2197 (2001).
52. S. E. Potts, H. B. Profijt, R. Roelofs, and W. M. M. Kessels, *Chem. Vap. Deposition*, **19**, 1 (2013).
53. Y. Civale, A. Redolfi, D. Velenis, N. Heylen, J. Beynet, I. S. Jung, J. J. Woo, B. Swinnen, G. Beyer, and E. Beyne, *Proc. 4th Electronics System Integration Technology Conference (ESTC 2012)*, Amsterdam, Sept. 17, 2012, paper 1.1.
54. A. Agarwal and M. J. Kushner, *J. Vac. Sci. Technol. A*, **27**, 37 (2009).
55. S. Banna, A. Agarwal, G. Cunge, M. Darnon, E. Pargon, and O. Joubert, *J. Vac. Sci. Technol. A*, **30**, 040801 (2012).
56. J. B. Park, W. S. Lim, B. J. Park, I. H. Park, Y. W. Kim, and G. Y. Yeom, *J. Phys. D: Appl. Phys.* **42**, 055202 (2009).
57. K. J. Kanarik, T. Lill, E. A. Hudson, S. Sriraman, S. Tan, J. Marks, V. Vahedi, and R. A. Gottscho, *J. Vac. Sci. Technol. A*, **33**, 020802 (2015).
58. D. Metzler, R. L. Bruce, S. Engelmann, E. A. Joseph, and G. S. Oehrlein, *J. Vac. Sci. Technol. A*, **32**, 020603 (2014).
59. S. U. Engelmann, R. L. Bruce, M. Nakamura, D. Metzler, S. G. Walton, and E. A. Joseph, *ECS Journal of Solid State Science and Technology*, **4**, N5054 (2015).
60. E. Altamirano-Sánchez, Y. Yamaguchi, J. Lindain, N. Horiguchi, M. Ercken, M. Demand, and W. Boullart, *ECS Trans*., **34**, 377 (2011).
61. G. S. Oehrlein, R. J. Phaneuf, and D. B. Graves, *J. Vac. Sci. Technol. B*, **29**, 010801 (2011).
62. N. Agrawal, Y. Kimura, R. Arghavani, and S. Datta, *IEEE Trans. Electron Devices*, **60**, 3298, (2013).