# On Polymorphic Circuits and Their Design using Evolutionary Algorithms

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**Abstract.** This paper introduces the concept of polymorphic electronics (polytronics) – referring to electronics with superimposed built-in functionality. A function change does not require switches/reconfiguration as in traditional approaches. Instead, the change comes from modifications in the characteristics of devices involved in the circuit, in response to controls such as temperature, power supply voltage (VDD), control signals, light, etc. The paper illustrates polytronic circuits in which the control is done by temperature, morphing signals, and VDD respectively. Polytronic circuits are obtained by evolutionary design /evolvable hardware techniques. These techniques are ideal for the polytronics design, a new area that lacks design guidelines/know-how,- yet the requirements/objectives are easy to specify and test. The circuits are evolved/synthesized in two different modes. The first mode explores an unstructured space, in which transistors can be interconnected freely in any arrangement (in simulations only). The second mode uses a Field Programmable Transistor Array (FPTA) model, and the circuit topology is sought as a mapping onto a programmable architecture (these experiments are performed both in simulations and on FPTA chips). The experiments demonstrated the synthesis of polytronic circuits by evolution. The capacity of storing/hiding "extra" functions provides for watermark/invisible functionality, thus polytronics may find uses in intelligence/security applications.

## 1. Introduction

The classic approach to multifunctional system design is based on switching/multiplexing the output of single-function modules/subsystems, each with its stand-alone independently implemented circuit. When a condition is triggered, either by a command, or by the signal from a sensor/detector, a switching action takes place routing the output of one module instead of another. If N functions are needed, area for implementation of N modules needs to be physically present.

Reconfigurable devices allow the ensemble to collapse possibly within the size of one module, resources being shared, different functions being achieved following a reconfiguration based on switches. One of the consequences is efficient adaptive computation. Circuits can react to environment or context and change functionality as appropriate. A simple example is that of a power aware Digital to Analog Converter in a portable device, capable of 16 bits resolution if the battery is loaded, and only 8 bits if battery is low (a fine-grained resolution with no resource overhead can be envisioned for graceful degradation). Similarly, a speed/resolution compromise can be imagined; e.g. 16 bits at 100kHz and 8 bits at 1MHZ.

In this paper we introduce another approach to multi-functionality, based on the polymorphic electronics concept first described in [1]. The term *polytronics* is derived from *poly*morphic elec*tronics*, but covers a wider range of polymorphic information processing structures, referring to primitive computational elements with built-in, superimposed multi-functional designs. This contrasts not only with today's digital logic circuits, but, in fact, with all currently used information processing structures (electronic and non-electronic, such as optical), which are based on primitive components designed for single function. The concepts of polytronics can be applied to multi-functional devices (for an example of a multi-functional devices see [2], for evolving devices one can follow a methodology as in [3]), or to multi-functional circuits, which is the focus of this paper. Polytronic circuits have several intrinsically built-in functions, and can have the same output provide different functional response under the control of certain global parameters, such as the supply voltage. In a different embodiment the circuit can provide different desired functional response simultaneously at different probing points. Polytronics could constitute the fabric of a new type of versatile, multi-functional systems.

A simple example of multiple functionality can be considered in the context of a configurable logic block (CLB) that needs to provide, selected as needed, either an OR function or an AND function. A common implementation technique uses a circuit implementing the AND, a circuit implementing the OR, and a selection logic that, based on a control signal, activates the desired circuit and routes its output to the output of the block. In a polytronic implementation a single circuit would be designed. The function of the circuit would change as a result of changes that a control parameter produces in the parametric characteristics of its constituent devices. The control parameter could be voltage, temperature, light, radiation, or any other parameter that changes the characteristic (and operational point) of a device.

This paper demonstrates the concept of polytronics, and in particular the use of evolutionary/evolvable hardware techniques to obtain polytronics. The paper is organized as follows: Section 2 discusses the evolutionary approach to polytronic design and details the two techniques employed in the experiments – free evolution and evolution on the FPTA. Section 3 presents four experiments in which polytronic circuits are evolved. Section 4 presents a discussion on the evolved polytronics as well as plans for follow-on experiments. Section 5 discusses possible applications of polytronics in defense/security/intelligence and space applications. Section 6 presents the conclusions.

## 2. Evolutionary Approach to Polymorphic Design

How to design polytronic circuits? Unlike the case of traditional circuits there are no design guidelines or handbooks. The approach relies largely on changes in the device characteristics, usually subtle effects, commonly ignored in a first order approximation by traditional design (e.g. changes with temperature). Evolution however, can do without design rules, as long as the circuit specifications are straightforward, which is the case, and candidate circuits can be evaluated and ranked - thus, this is a problem well suited for evolutionary approach. An automated synthesis system based on evolutionary algorithms is presented with the multiple requirements that the circuit needs to satisfy. A generative process determines candidate solutions that are evaluated against a fitness function incorporating desired criteria and compete against each other, the best candidates being selected for reproduction and the process repeats; in most cases after a number of generations an acceptable (perhaps sub-optimal) solution can be found. For details on different ways of applying evolutionary techniques to design of electronic circuits see for example [4-6].

The resources used in the experiments are of two different kinds. In one case, unconstrained evolution allows the free exploration of the search space, with no topological restrictions – this can lead to new, (patentable) designs. The second approach uses the FPTA model introduced in [7] and further detailed along with various evolutionary experiments in [8-10]. Different loads were used in experiments to explore their influence on the convergence of the evolutionary algorithm.

### 2.1 Unconstrained evolution

The unconstrained/free evolution was described in [11]. The experiments described in this paper use only NMOS and PMOS transistors, which can be interconnected in arbitrary topologies. The width and length of the transistor channel were also parameters for search. The advantage of this representation is the flexibility to map circuits with arbitrary types of interconnections, by establishing a straightforward mapping between the electronic circuit topology and the chromosome. Each functional block of the chromosome, also called gene, states the nature, value, connecting points, width and length of the MOS (Metal-Oxide-Semiconductor) transistors. However, there is no integrated circuit model that supports the hardware implementation of the evolved solutions.

### 2.2 Evolution on FPTA

The FPTA is a cellular architecture, with transistor-level reconfigurability. Its flexibility in comparison with other devices was discussed in [10]. The elementary cell has a number of "fixed" transistors interconnected by transistors acting as switches. The number of "fixed" transistors per cell varied in different generations of the FPTA. The experiments presented here used the early version of the cell, with 8 transistors interconnected by 24 switches [7]. Each switch is associated with a bit in the chromosome describing the cell. A bit being "1" translates to a closed switch, a "0" to an open switch. One can configure candidate circuits by programming the switches with binary string chromosomes produced by the Genetic Algorithm.

This approach has the advantage that its solution can be implemented after evolution, or evolved directly in hardware on a programmable FPTA chip. Moreover, the chip can be reconfigured to map different polymorphic gates as needed. The disadvantage is that the topology has certain restrictions imposed by architectural constraints. Also, the evolved circuits may in certain cases rely/make use of the non-ideal characteristic of the switches (i.e. the non-zero ON resistance and finite OFF resistance), which means that the transistors acting as switches can not be ignored and may lead to a topology that involves more actual components than may be possible if connections were ideal and the topology unconstrained.

## 3. Evolutionary Experiments

The experiments presented in this paper demonstrate the evolution of polymorphic gates that change logic function under control of a) temperature, b) control signal or c) VDD. The temperature controlled polytronic AND/OR gates are AND for 27°C and become OR at 125°C (in other experiments at 5°C/90°C – one can choose the desired temperature). In a second set of experiments we evolved a AND/OR/XOR polymorphic gate with 10 transistors, which reacts at the change of a control signal Vmorph as follows: the gate is OR if $V_{morph}$ = 0V, XOR if $V_{morph}$ =1.5V, AND if $V_{morph}$ = 3.3V. In a third set of experiments we evolved polytronics gates changing from AND when the power supply was 1.2V to OR when the power supply was 3.3V, etc.

The following indicates the evolutionary parameters used in the experiments. The population size was 50; the number of generations ranged between 100 to 200; the mutation rate was 8% and crossover rate was 30%.

### 3.1 Control by temperature

The experiments were performed through SPICE simulations as well as on the FPTA chip, with the chip immersed in a temperature chamber. (For more extreme temperature experiments and a study on using evolution to expand the operation domain of electronics at high temperatures see [12]). The simulation experiments performed SPICE analysis at two temperatures of interest, circuit response was evaluated against two different criteria (for the lower and for the higher temperature). The fitness function was based on a combination of the quality of solutions at the two temperatures.

#### 3.1.1 Free/unconstraint topology search

In a first experiment, a AND/OR polymorphic gate was evolved. The gate behaves as an AND gate at 27°C and as an OR gate at 125 °C. Figure 1 depicts the circuit and its response. The circuit receives two inputs, In1 and In2, and it uses a 3.3V voltage supply. The output was a 10MOhms resistive load. This figure depicts the circuit inputs, In1 and In2, as well as the circuit output for 27°C (AND gate) and 125°C (OR gate).

#### 3.1.2 Evolution on FPTA

A similar AND/OR gate was evolved using two FPTA cells. The evolved circuit behaves as an AND gate at 5°C, and as an OR gate at 90°C. Figure 2(A) shows the evolved circuit and Figure 2(B) shows the circuit response. Inputs In1 and In2 are applied to the first FPTA cell, while the output is collected from the second FPTA. Each re-configurable cell consists of 8 transistors interconnected through 24 switches.

### 3.2 Control by dedicated input signal $V_{morph}$

More than two functions can be superimposed. Figure 3 depicts a circuit that behaves as an OR for $V_{morph}$ = 0, as an XOR for $V_{morph}$ = 1.5V and as an AND for $V_{morph}$ = 3.3V. The schematic in Figure 3 provides the information on transistors width and length, parameters that have been

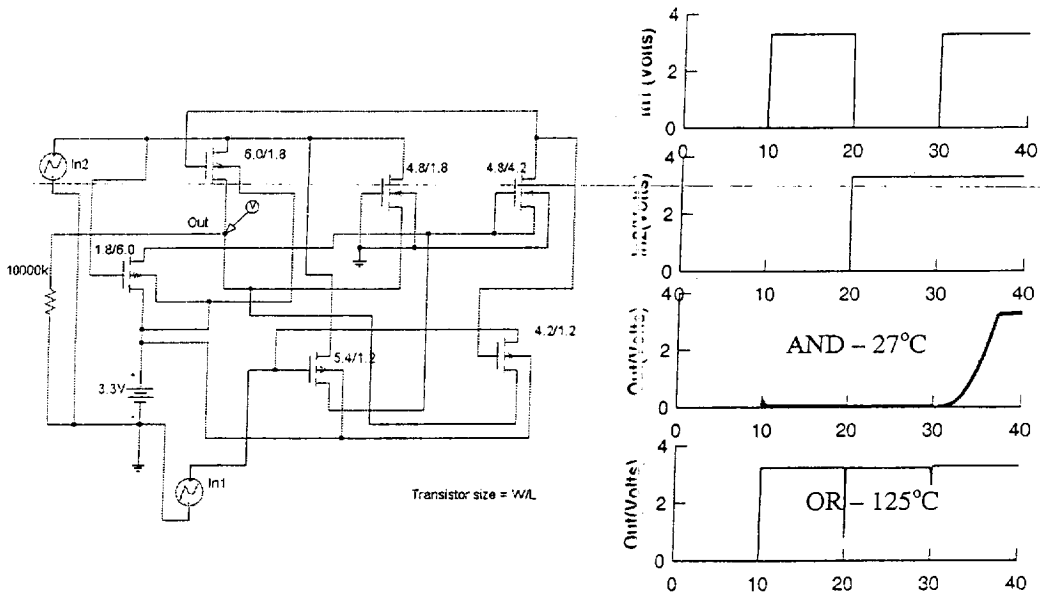


**Figure 1** – Schematic of the Polymorphic circuit evolved for different temperatures (left). Circuit inputs and outputs (at 27 and 125°C) in the left. Axis X shows time in miliseconds.

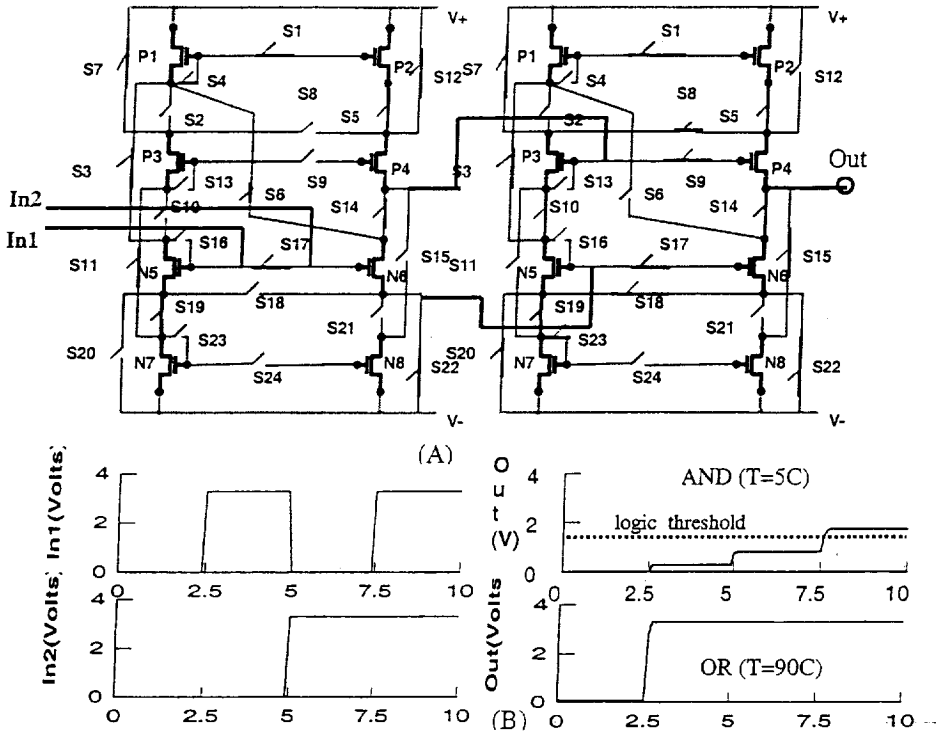


**Figure 2** - Schematic of the evolved circuit on the FPTA(A) and its response at different temperatures(B). Axis X shows time in miliseconds.

evolved together with the circuit topology. Also shown in this figure the response of the evolved polymorphic gate.

### 3.3 Control by supply voltage (VDD)

In this experiment we evolved a circuit that performs different functions depending on the level of the power supply voltage, VDD. When VDD = 3.3V, the gate behaves as an OR gate; when VDD=1.2V it behaves as an AND gate. A possible application would be to endow circuits with built-in different behavior for *active* or *sleeping (power saving)* mode. Figure 4(A) displays the evolved circuit and Figure 4(B) shows the response. Note that the input voltage levels are adjusted with VDD.

## 4. Discussion

The experiments presented in this paper show solutions that satisfied the imposed stopping conditions for evolution. Additional constraints are required to produce circuits closer to practical use. The gate in Figure 1 evolved to a satisfactory solution as far as the logic level, which was the objective of the experiment, yet it is a slow gate, and its response can be definitely improved (perhaps even by a solution with fewer transistors). If we don't ask for it, evolution will not volunteer a solution for what we think (but not specify in clear) should be good. In the second experiment Figure 2 illustrates a compliant response (the level in the last interval, corresponding to the (1, 1) input combination is interpreted as a (1), being above the threshold defined as half-way between VDD and GND. Again, this is to illustrate the concept –more robust circuits further away from the threshold can be obtained, which will become the focus once we find the most useful context (from an application point of view) as far as temperature range and voltage level. Another observation is that the first experiment (without constraints in the possible connections) led to a better solution. The polymorphic gates with voltage control are not the first ever multi-functional gates that change function at the modification of an input control signal. For example U.S. patent 042335245 describes a 4 transistor circuit that performs XOR/OR/NAND and a 6 transistor that performs ADD/NOR/OR/NAND/AND. It is Ok for polymorphic circuits to exploit switch-like functionality of transistors – the main difference compared with the classic switch-based approach to multi-functional circuits would be that these switches are not (only) for multiplexing the outputs from constituent stand-alone functions.

VDD control can be used in having reactive power-down change of functionality. It is also to observe that with VDD one can quasi-instantly change the function of the entire circuit, no matter its size! In fact all global controls including supply voltage, temperature, or control signal, etc. can be used for quasi-instant control of an entire circuitry. To change the function of a classical reconfigurable circuit all configuration bits need to be loaded and the associated time increases with the size. Fractions of second are needed for million gates

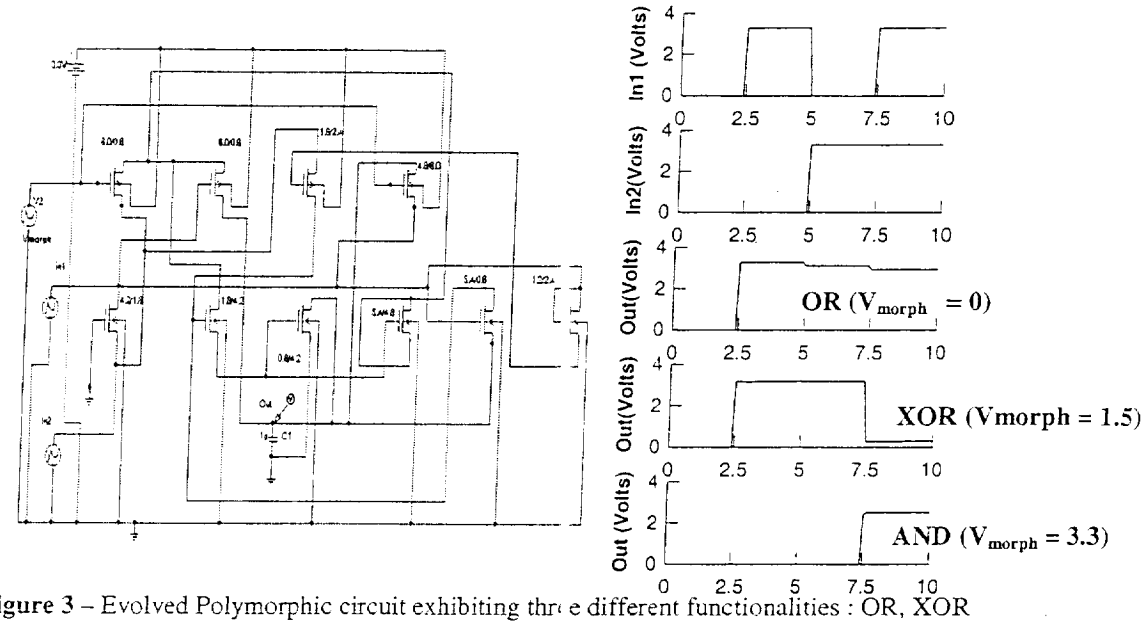


**Figure 3** – Evolved Polymorphic circuit exhibiting thr e different functionalities : OR, XOR and AND. At the right, circuit's inputs and outputs are lotted.

components. Using a flash context-switching scheme is rapid but requires extensive extra resources. Polymorphic circuits are fast – circuits could completely change function on a clock edge.

## 5 Applications

The polytronics concept opens a new domain of commercial and defense applications. For example:

- Polytronics provides a new way to obtain circuits with one or more conceived "extra" functions in addition to the "main" function of the circuit. The "extras" can be activated under certain conditions or can coexist. Possible uses of the "extras": an authentication signature / watermark, extra protection from reverse engineering (the real operational function of the circuit shows up only in special conditions), protection from unauthorized usage by incorporating biometric info part of circuit design, providing an additional communication channel.

- Polytronics allows for a built-in reactive behavior surfacing/taking control in specified conditions: for example, smart fuses in which the increased temperature triggers a new functionality of the guidance electronics. It would also enable systems that rapidly morph between functions, without switching overhead. It would also provide more compact multi-functional designs.

Certain applications may require a hidden/secret function, hard to detect and/or understand if reverse engineered. Polytronics could provide this feature. For example, a circuit may for all purposes look and act as a clock generator. In reality, when a control key – such as temperature level or pattern, EM pattern, VDD control etc is applied, it would exhibit a burst that unlocks/resurrects a special encoding scheme. This "extra" function may be a watermark visible only when certain conditions are cr ated. This can be used for tagging, or other IP /verification need. The control may also be a biometric pa tern. For example, a circuit can be designed to produce its essential function only if its components receive in ividual specific biometric signal. More specific, the ar ay of voltages generated after a preprocessed fin gerprint scan influences different areas of the circuit "b asing" it variably to create the condition in which the sy tem is ok to operate. This offers a unique "p rsonalized" custom chip with biometric info part of its ha dwired design.

## 6. Conclusion

This paper introduced a new paradigm of circuits with sup r-imposed multiple functionality. Polytronics circ its are multi-functional circuits in which the fun tional changes come not from a switch-based routing of outputs of modules designed for individual functions, but more from superimposed functional design and cha ges from modifications of device characteristics and ope ating points. The paper demonstrates the approach for sev ral cases of morphing control – using temperature, VDD and control voltage signals. Evolvable hardware app ars an ideally suited technology for the desi n/determination of polytronics, since this is an area with ut any design know-how, but it is easy to specify requ rements in an objective function. Circuits were evol ed both with a free/unconstrained topology search, and using a FPTA model. The experiments show the succ ssful evolution of polytronic AND/OR and ANI /OR/XOR gates behaving differently at different

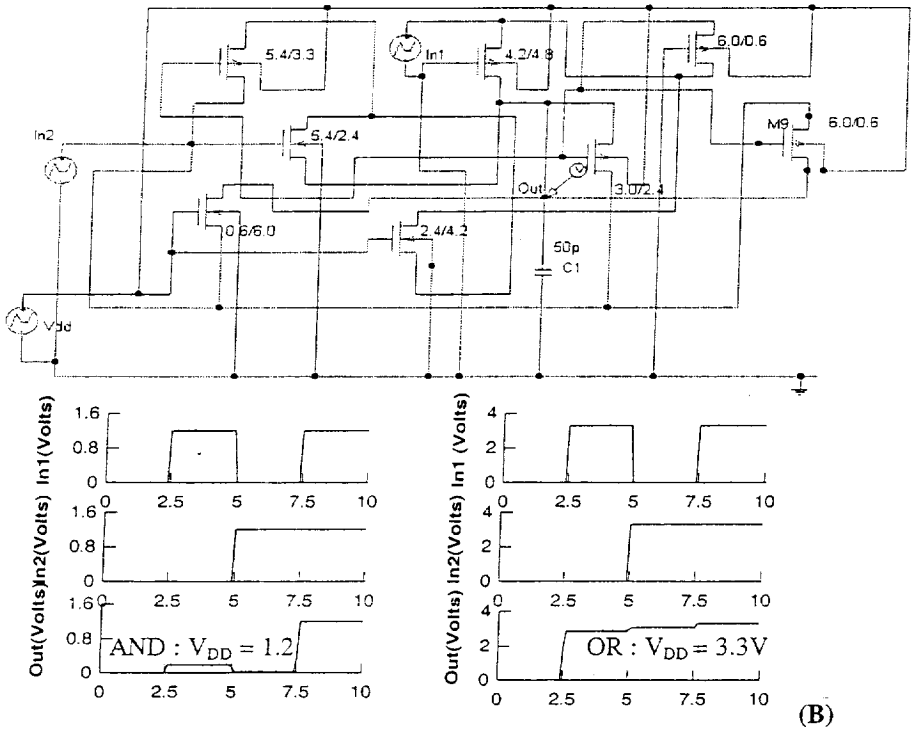


**Figure 4**– Schematic of the polymorphic circuit controlled by supply voltages(A). Circuit inputs and response for two cased, $V_{DD}$=1.2V (left) and $V_{DD}$=3.3V (right). Axis X gives the time in milliseconds.

temperatures, VDDs, or morphing voltage signals. The SPICE code for circuits discussed in this paper can be obtained from the URL provided as reference [13].

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