NBTI-Aware Synthesis of Digital Circuits

Sanjay Kumar

Chris Kim

Sachin Sapatnekar

University of Minnesota

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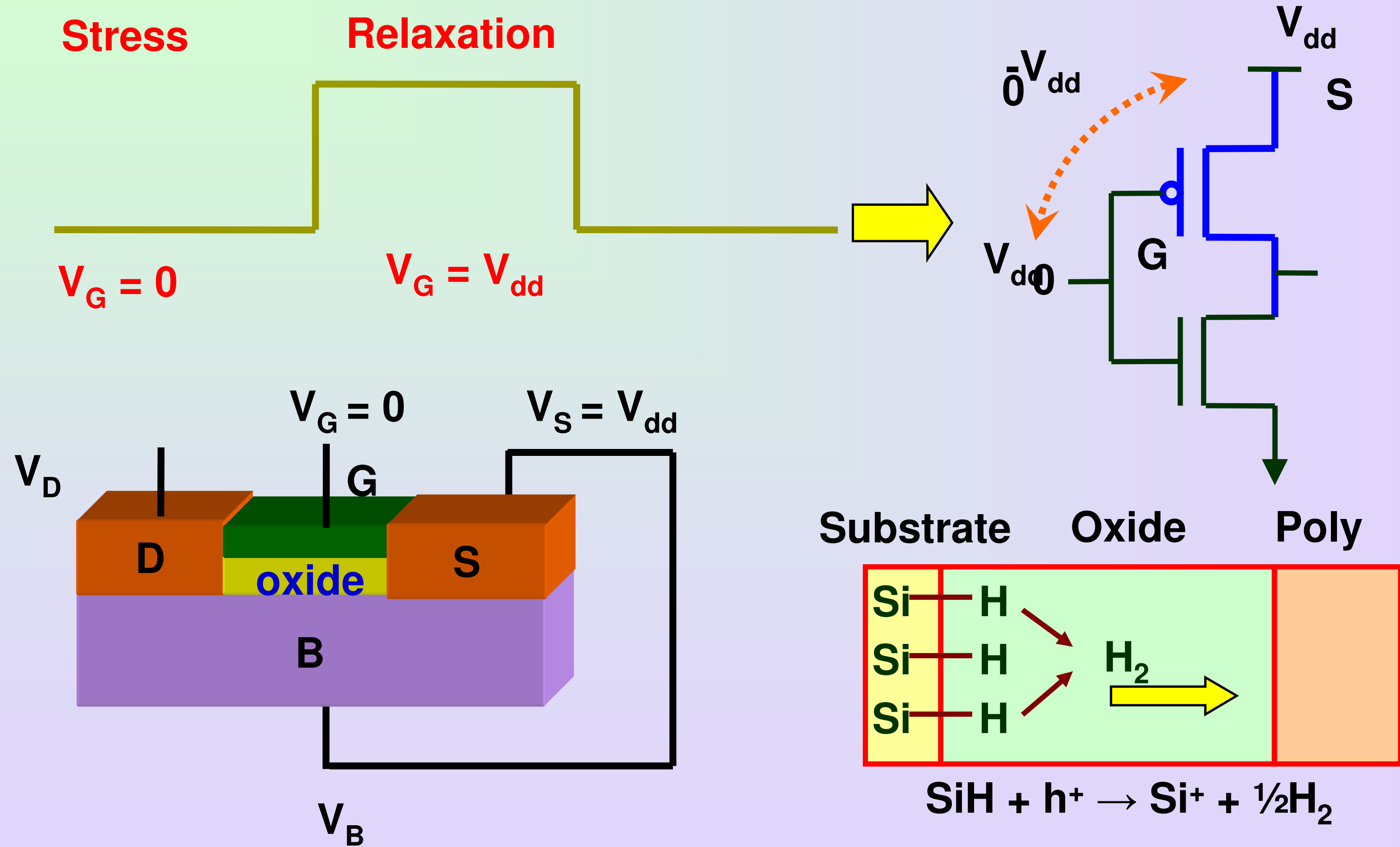
Negative Bias Temperature Instability (NBTI)

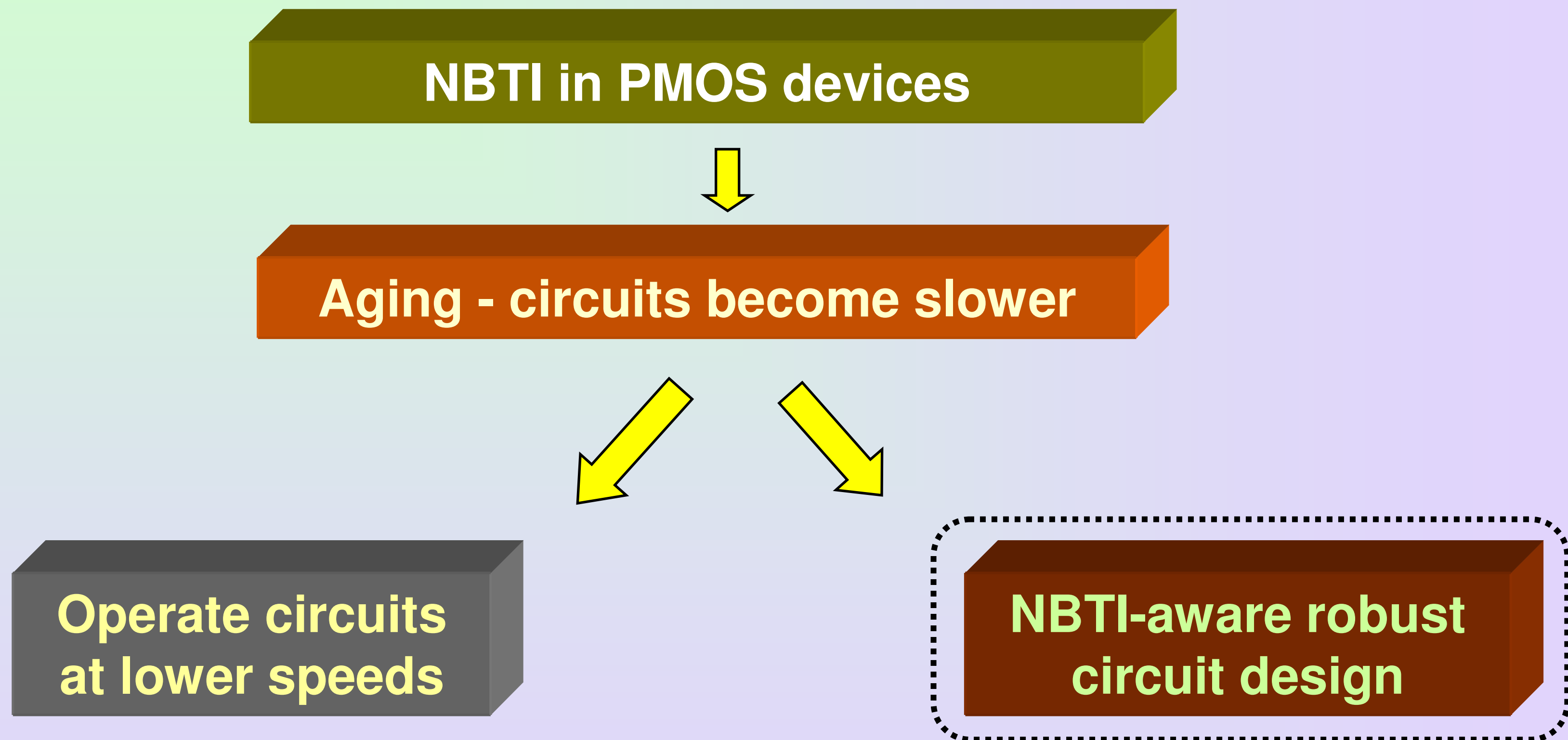


Increase in PMOS V_{th} gradually *over a few years*

Outline of this talk

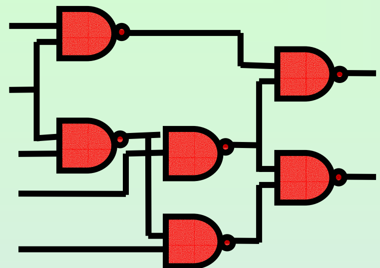
- Problem Description
  - How does NBTI affect circuits?
- Modeling and Estimation
  - What parameters does it depend on?
- Design for Reliability
  - How can we overcome this effect?
- Results and Summary
  - How does our work compare with other solutions?

Problem Statement

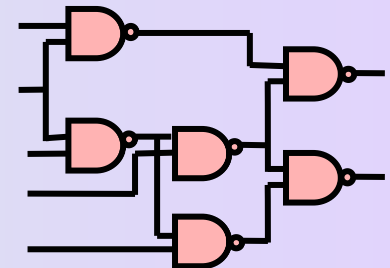


Design NBTI-resilient circuits with the least amount of overhead

Sizing for Reliability [DATE06, ICCD06, ISQED07]

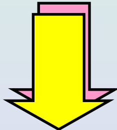


After 10 years



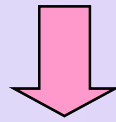
Original design

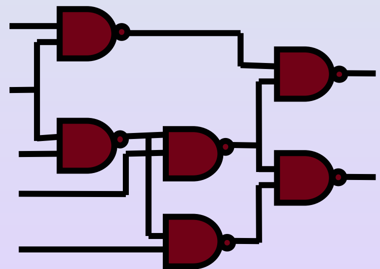
Gates become weak, target freq not met



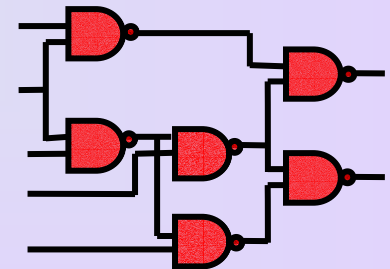
Area overhead

Reliable design





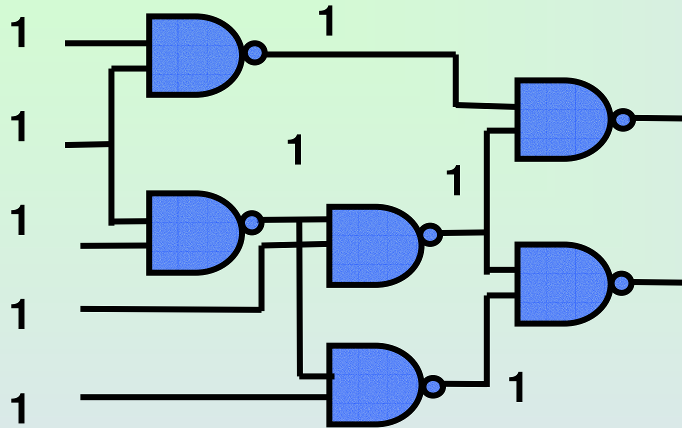
After 10 years

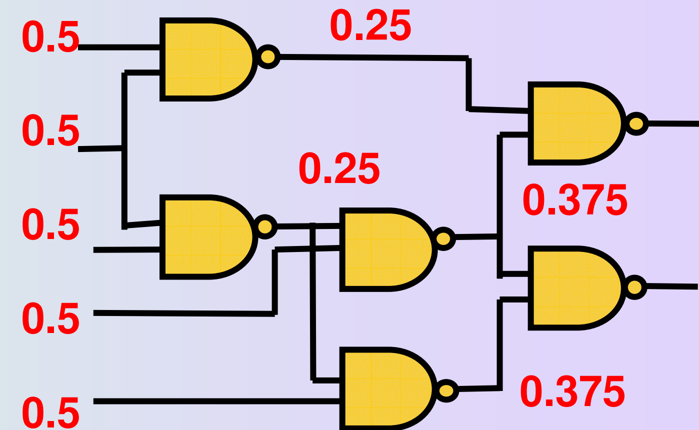


Design sized accounting for aging

Still meets specs

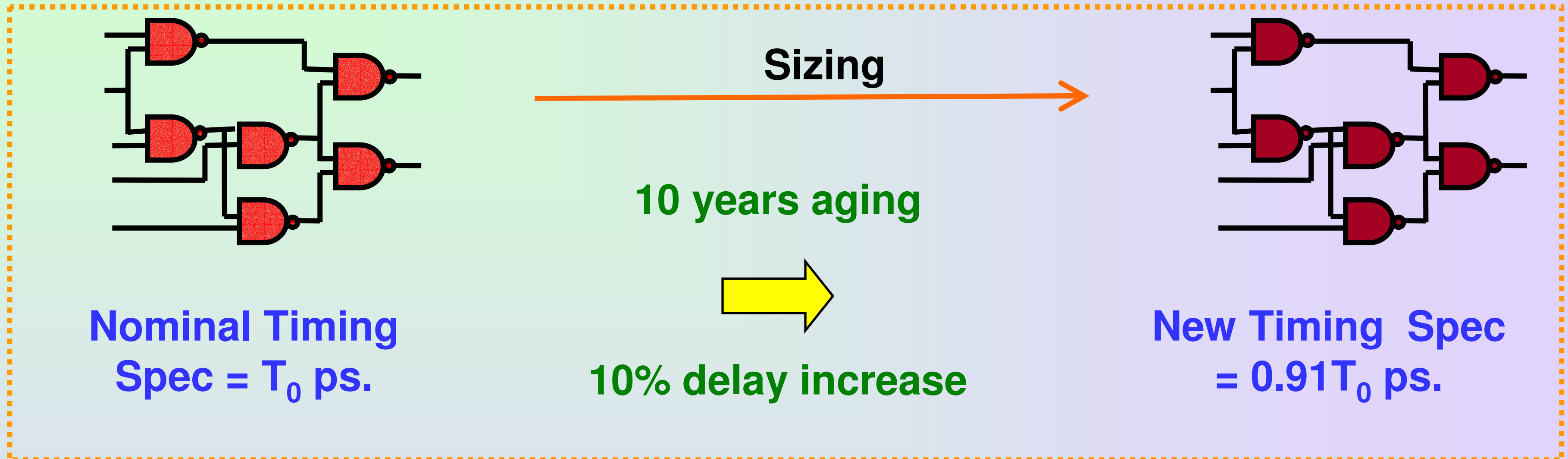
"Worst Case" NBTI Assumption





- Worst case NBTI
  - All PMOS devices degrade maximally
  - Easy to estimate impact
  - Conservative and pessimistic
- Actual Circuit Operation
  - NBTI effect based on ***Signal Probability (SP)***
  - Each node has a certain SP
  - Worst case can never happen

Limitations of Sizing based flow



Allows changes in gate sizes only

Synthesize circuits accounting for NBTI-induced delay degradation.

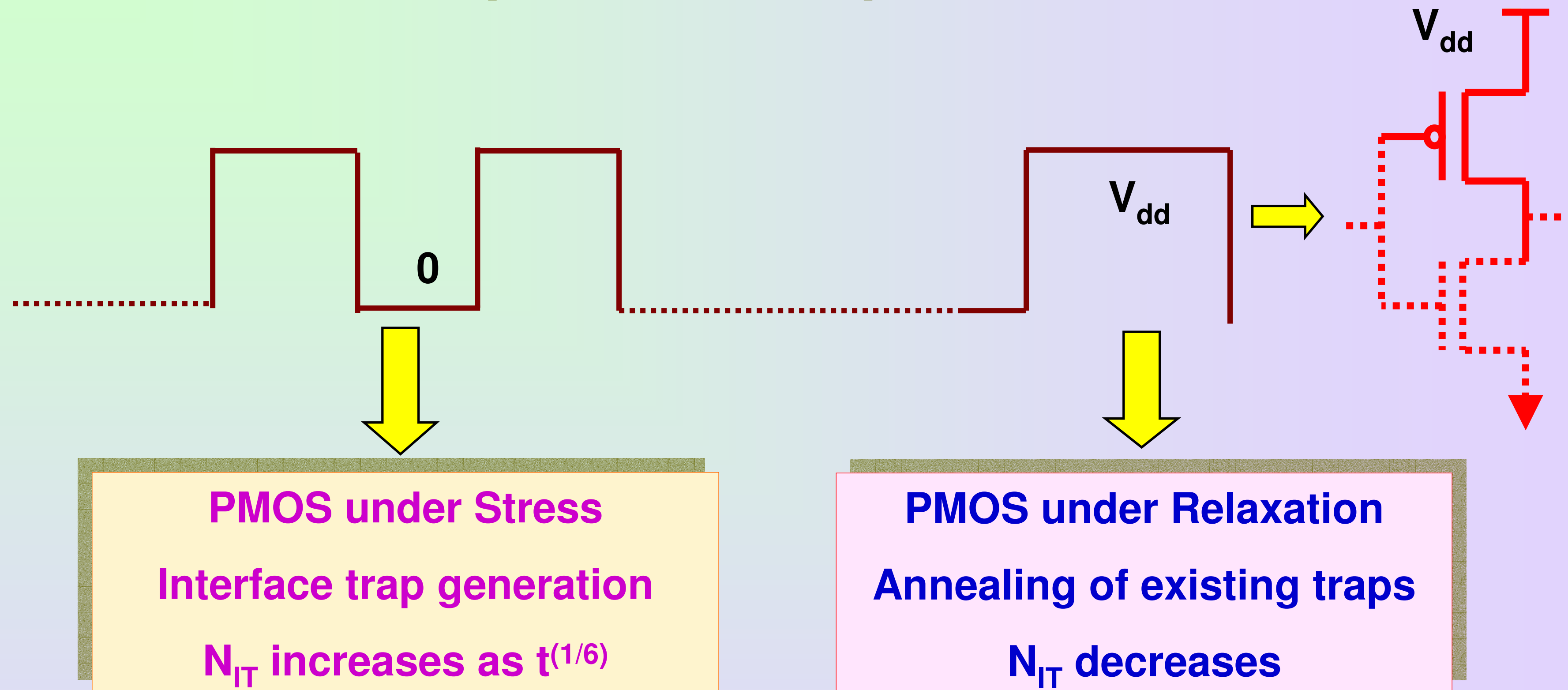
Our Work

- Focus
  - Incorporate NBTI-guard banding into synthesis during tech-mapping
  - Reduce pessimism in estimation of aging effects
  - Design best NBTI tolerant structures
- Requirements
  - NBTI-aware library characterization
  - Signal probability of primary inputs
  - Suitable cost function (delay, area, power, etc) in tech-mapping

NBTI Modeling and Library Characterization

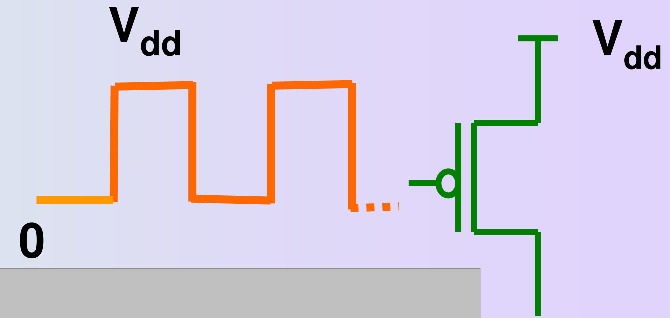
Key Results

NBTI Model (ICCAD06)



- N_{IT} strong function of Signal Probability (SP)
- Electrical parameter: $\Delta V_{th} \propto N_{IT}$

V_{th} Degradation



Vth (V)

0.47
0.45
0.43
0.41
0.39
0.37
0.35

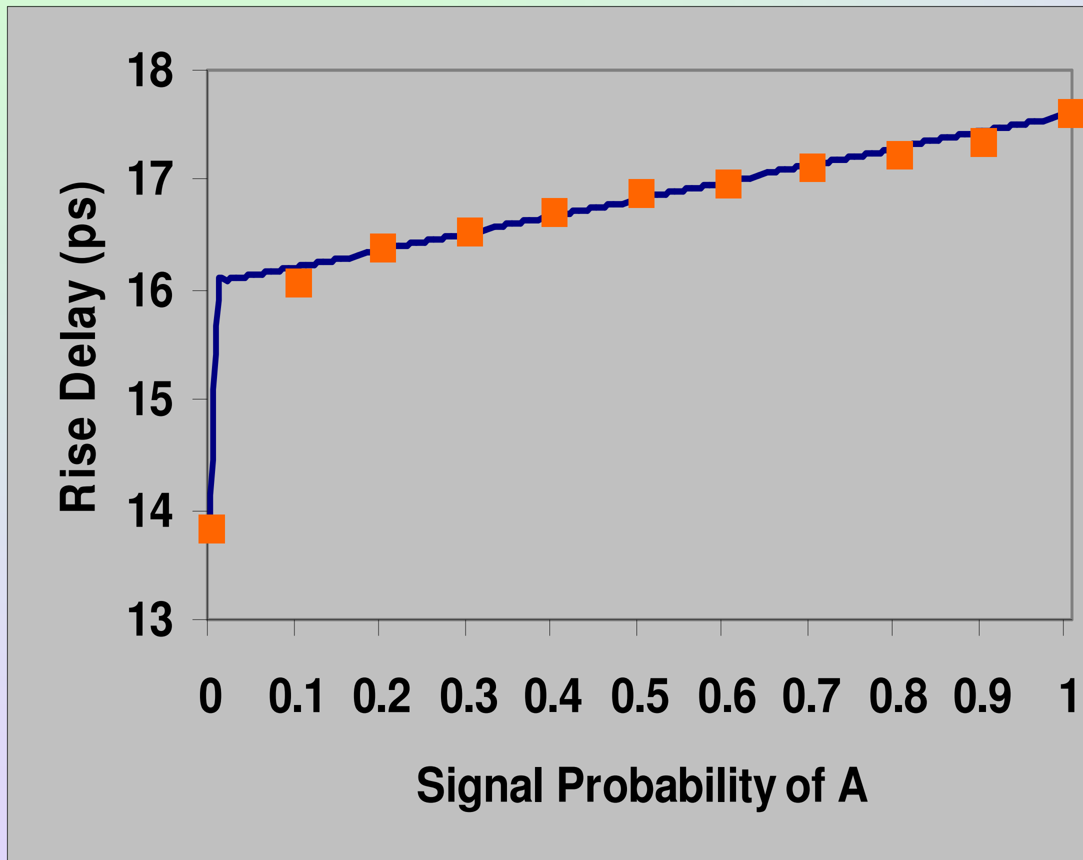
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

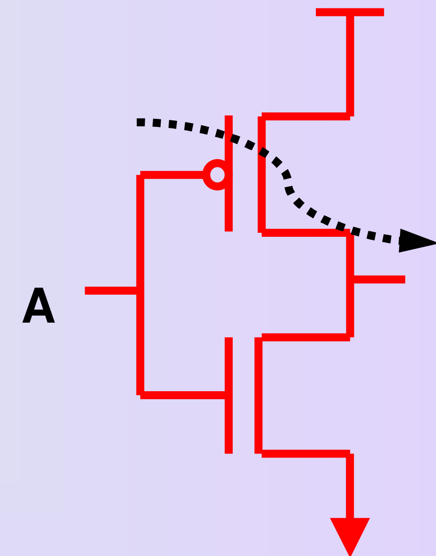
Signal Probability (SP)

V_{thmax}

Signal Probability: Probability that the signal is ***low***

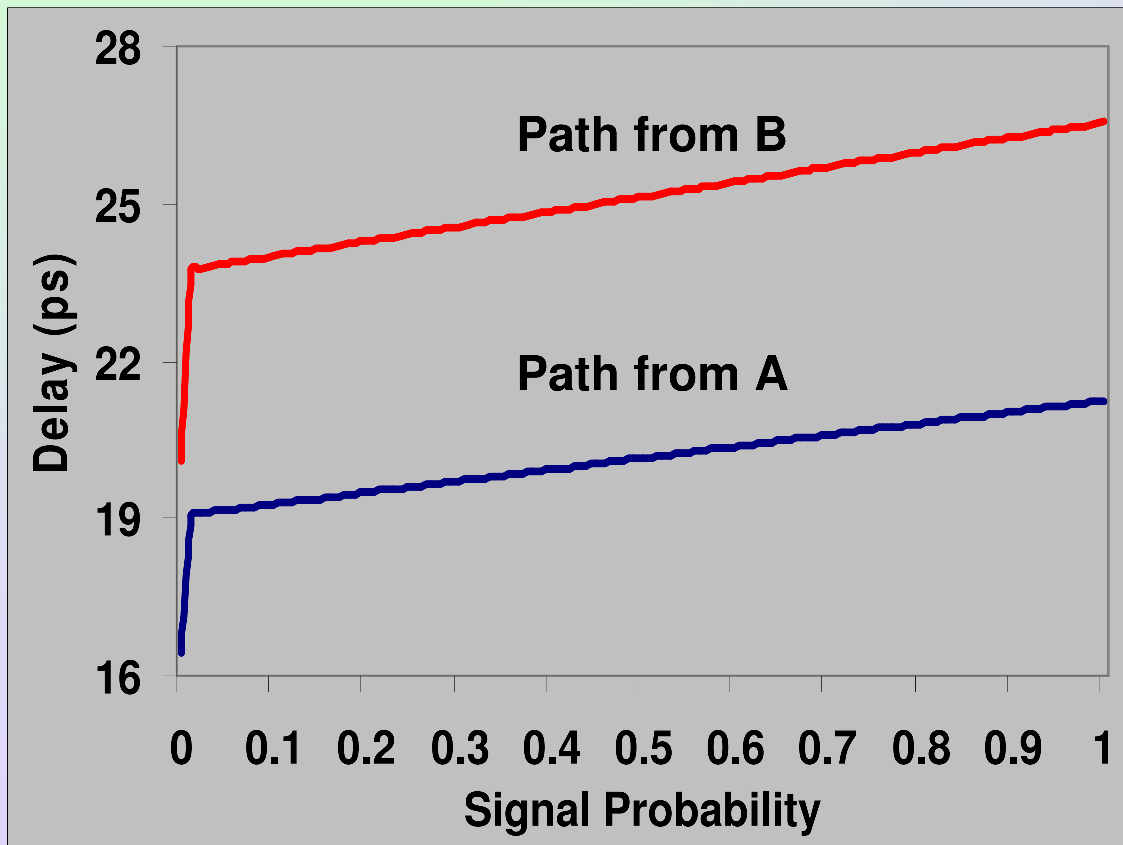
Inverter Characterization

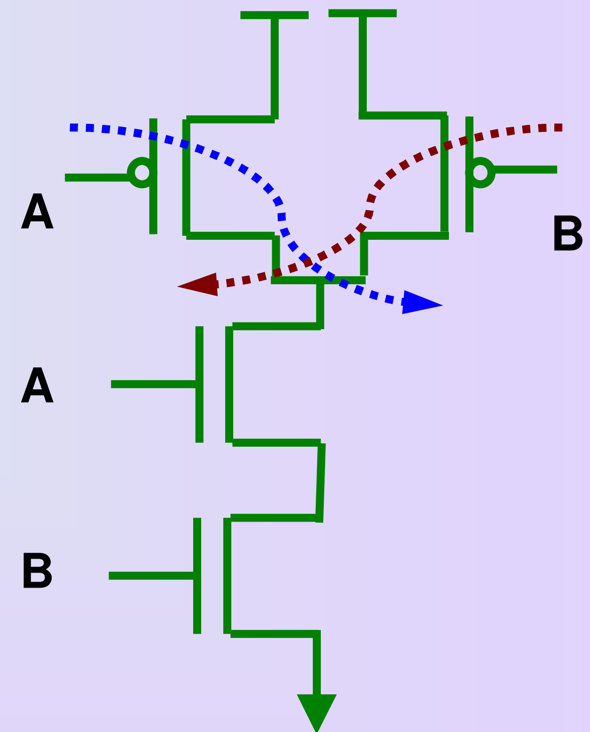




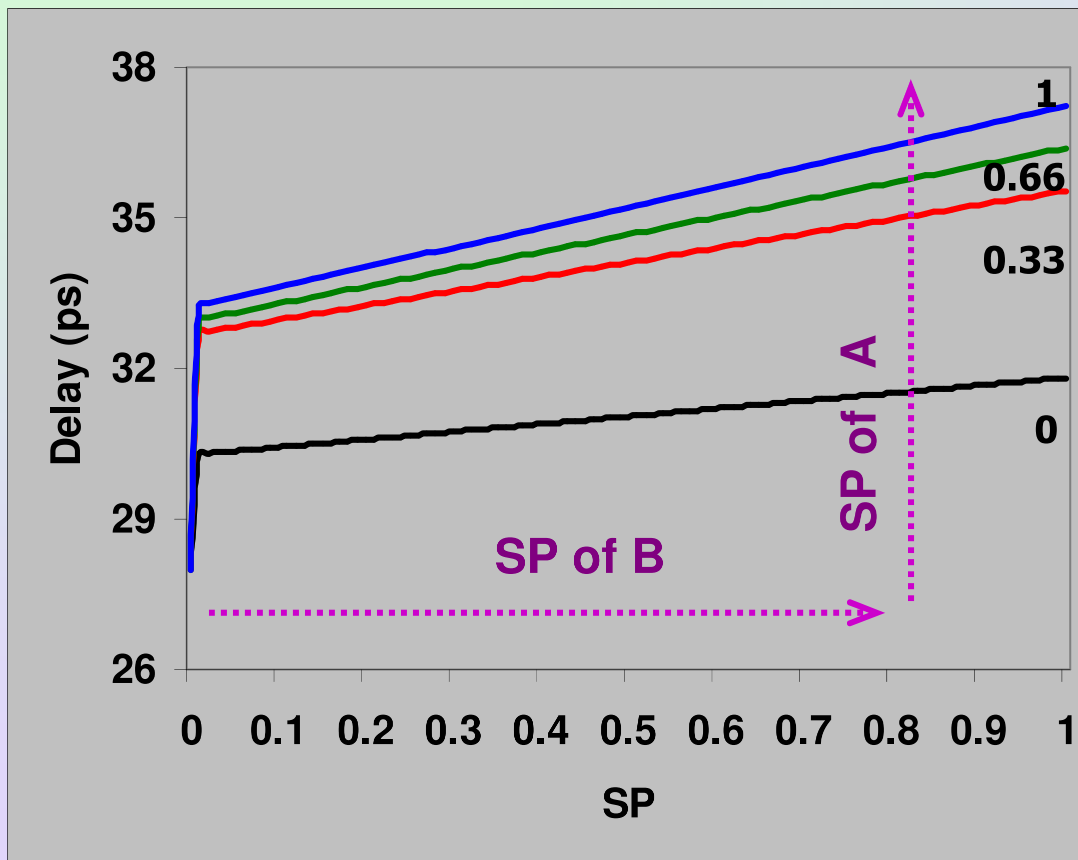
Build a model of delay versus signal probability

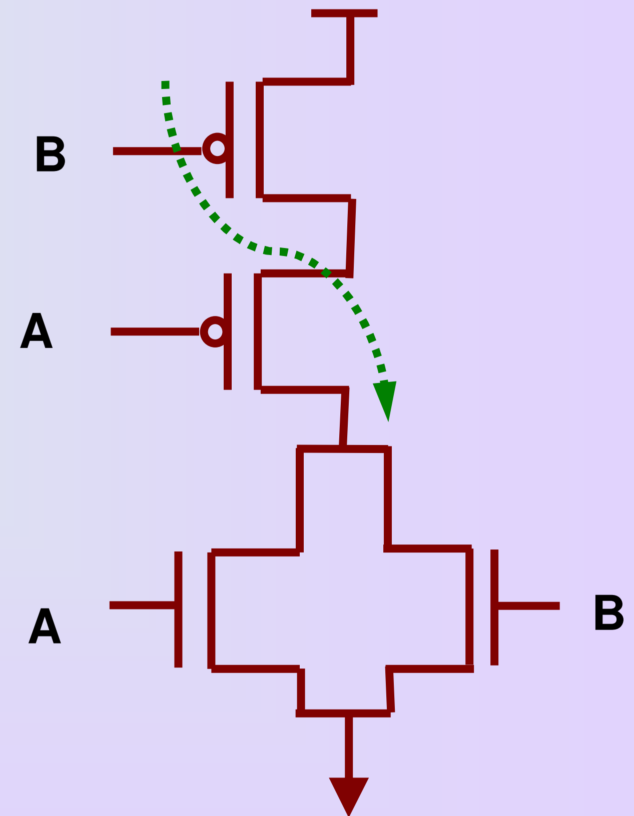
NAND Gates





NOR Gates – PMOS Stacking





Technology Mapping

SiS – synthesis tool

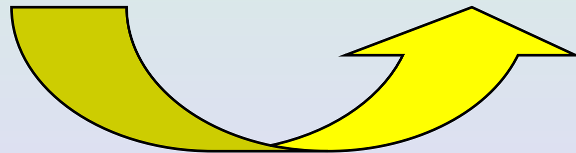
42 gates (NOT, NAND2, NAND3, NOR2, NOR3, AOI12, AOI22, OAI12, OAI22)

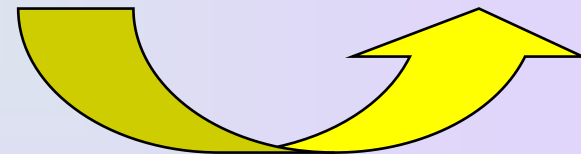
Nominal Synthesis

Library: Delay of gates characterized assuming no NBTI (Nominal PMOS V_{th})

Logic cone: Boolean function realized at each node

Cost function: Minimum area that meets the target delay





Compute delay of different candidate blocks at each node

Choose the structure with the best cost function

NBTI-Aware SP-based Synthesis

Library: Delay of gates characterized assuming no NBTI (Nominal PMOS V_{th})

Logic cone: Boolean function realized at each node

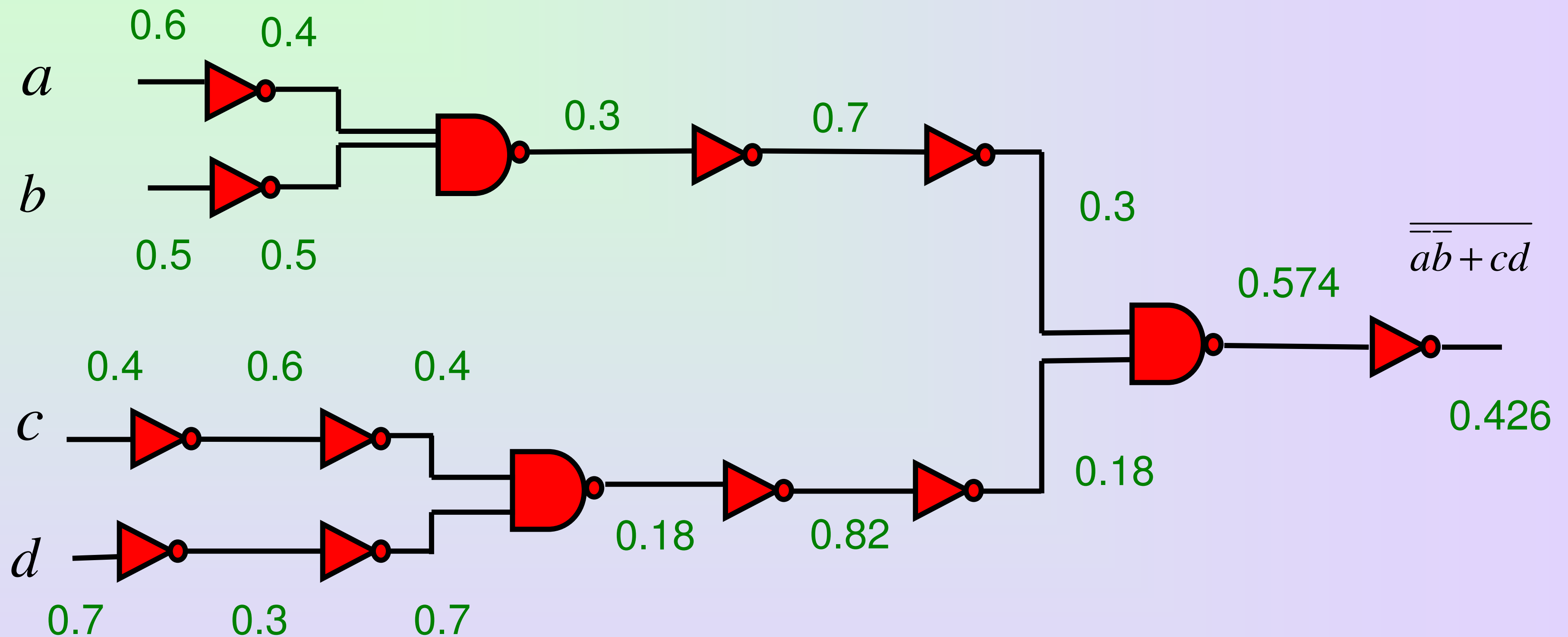
Cost function: Minimum area that meets the target delay

Compute delay of different candidate blocks at each node

Choose the structure with the best cost function

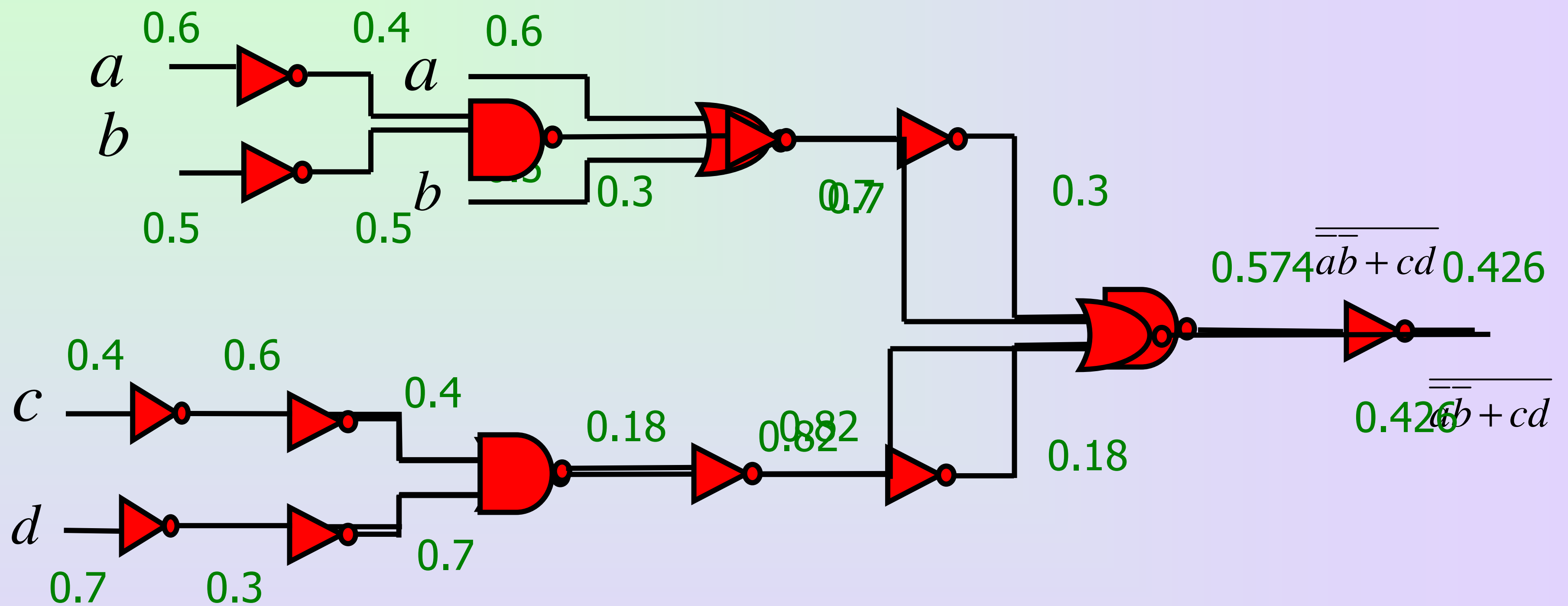
Pick best candidate gate under a new metric for delay

Subject Graph

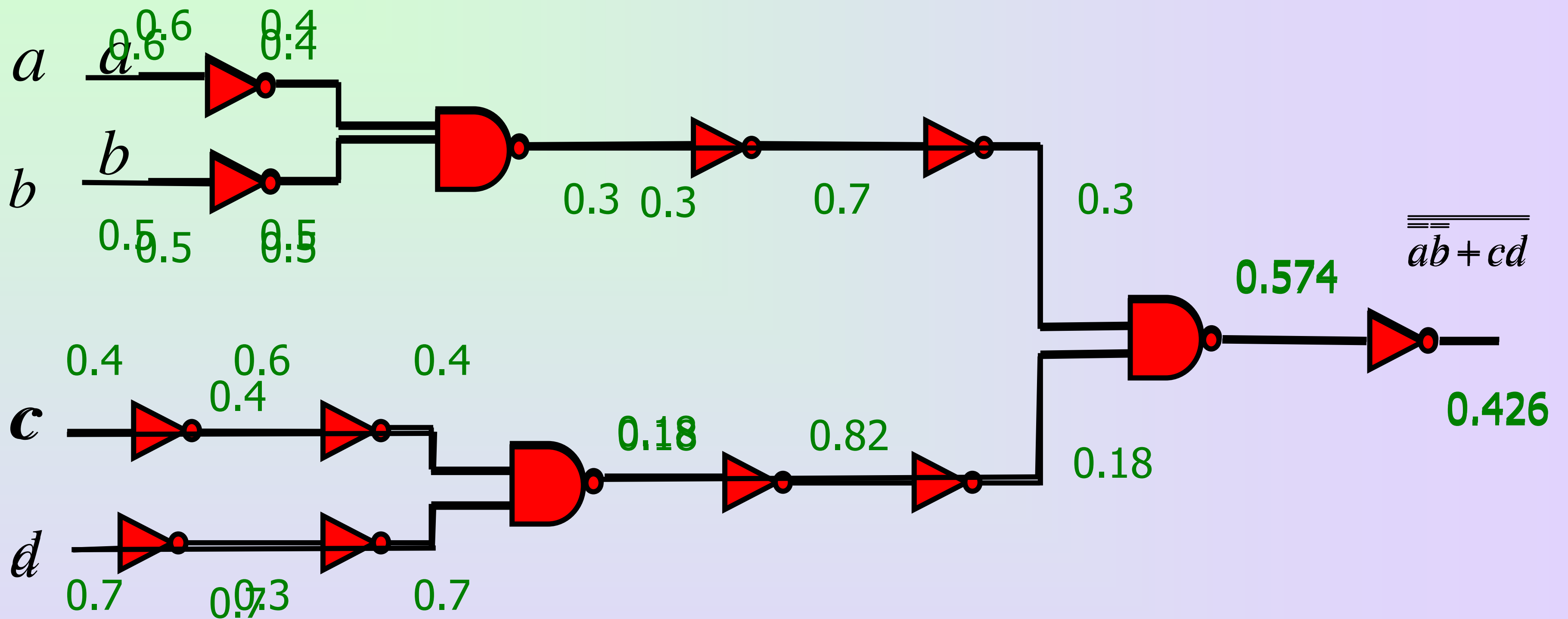


NAND-NOT Dual Representation of the Subject Graph

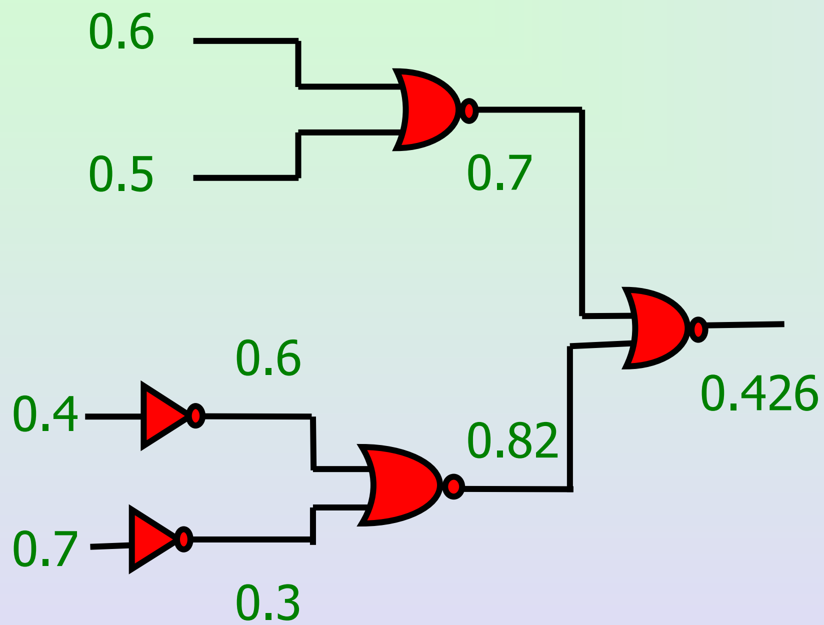
Performing SP-based Synthesis

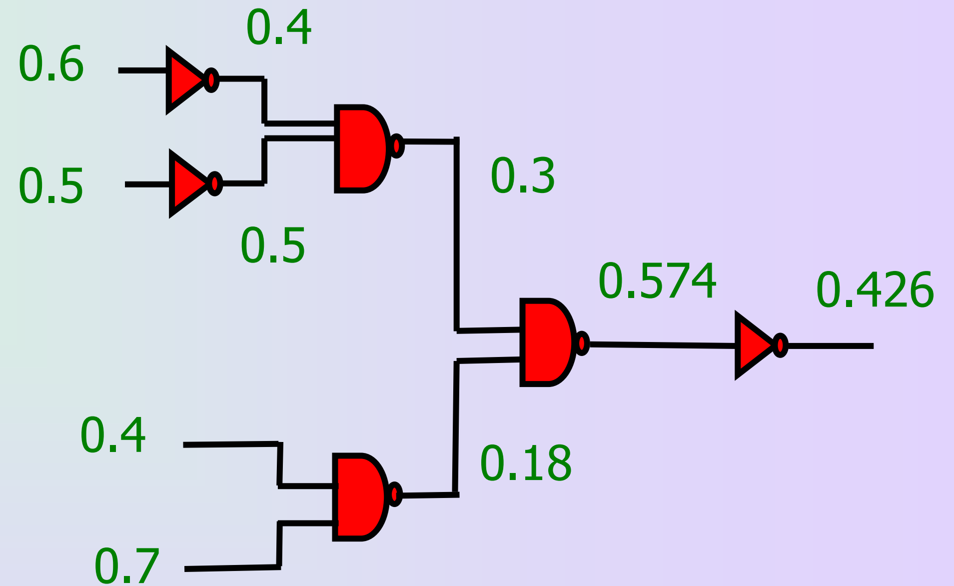


Performing SP-based Synthesis



Performing SP-based Synthesis





Pushing nodes with large SP inside the gates

Worst Case Synthesis

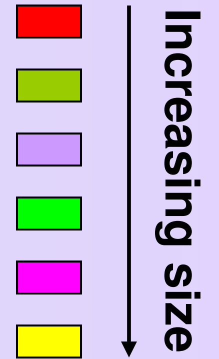
Pick best candidate gate under "worst case" NBTI-induced delay

Library: Delay of gates computed using V_{thmax} for PMOS transistors

Logic cone: SP of each node in subject graph set to 1

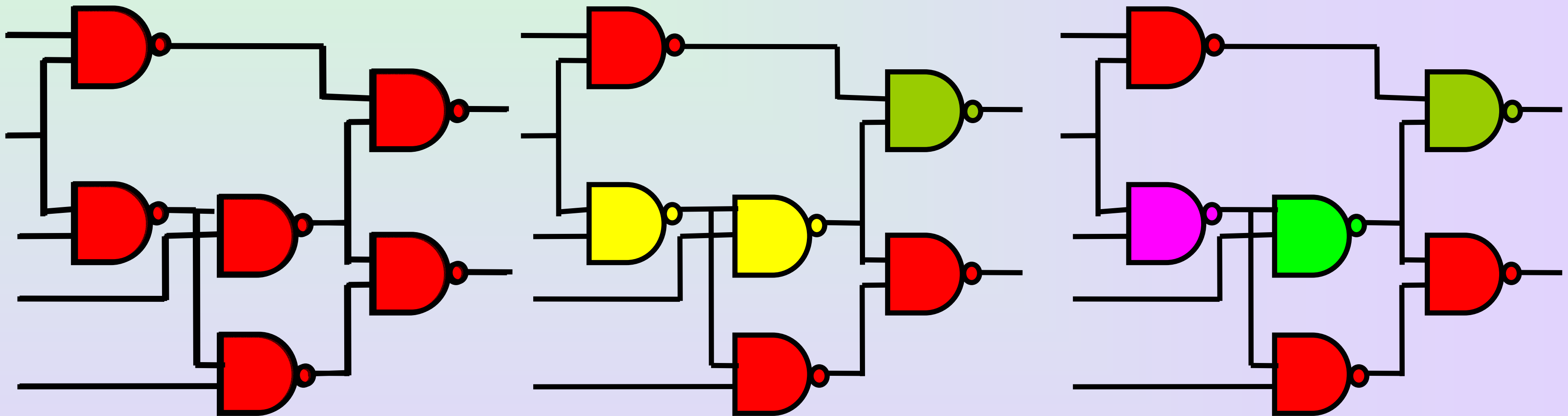
Cost function: Minimum area that meets the target delay

C17 - Synthesis Results



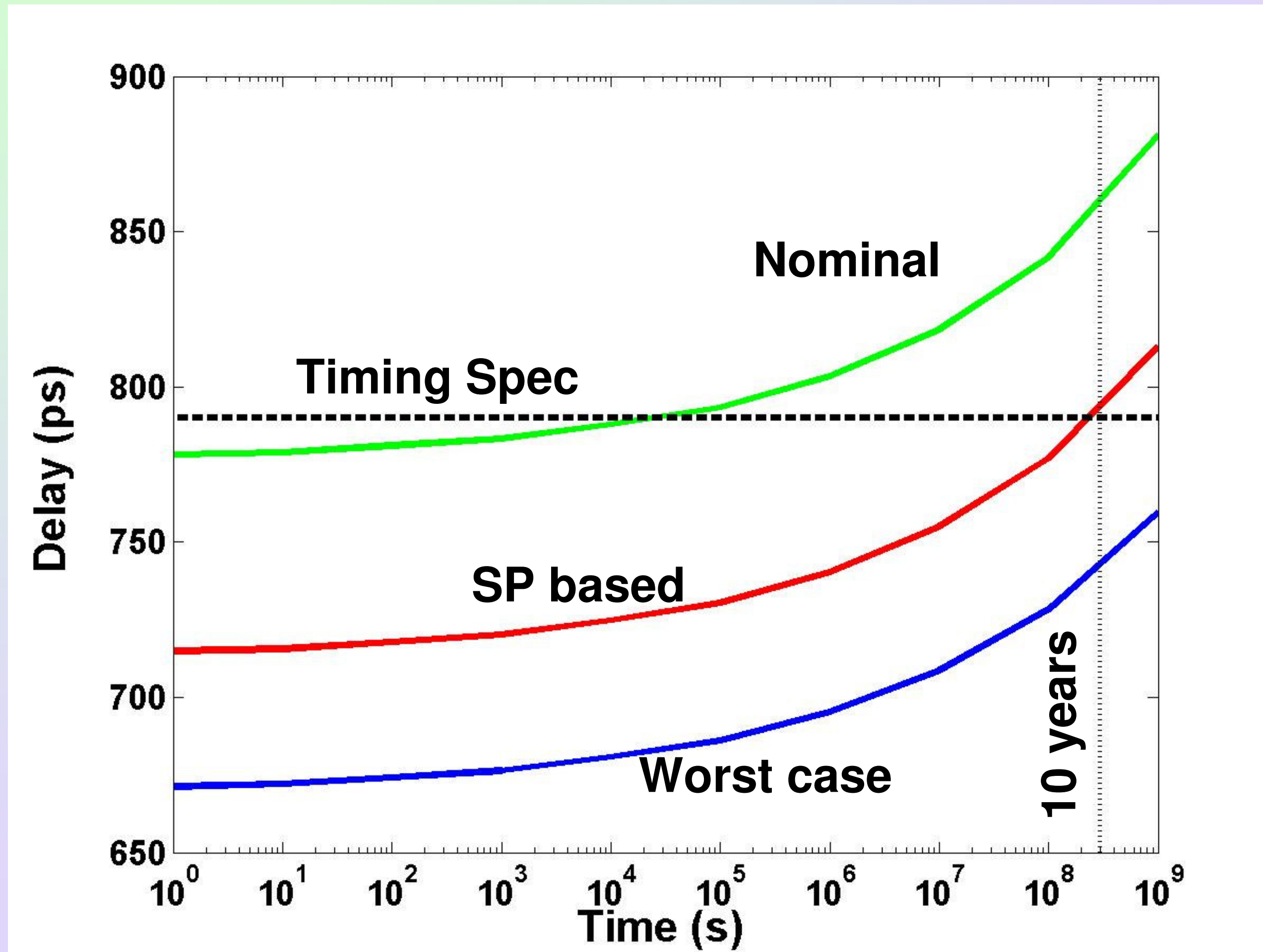
T_{spec} = 70ps

Circuit fails with aging



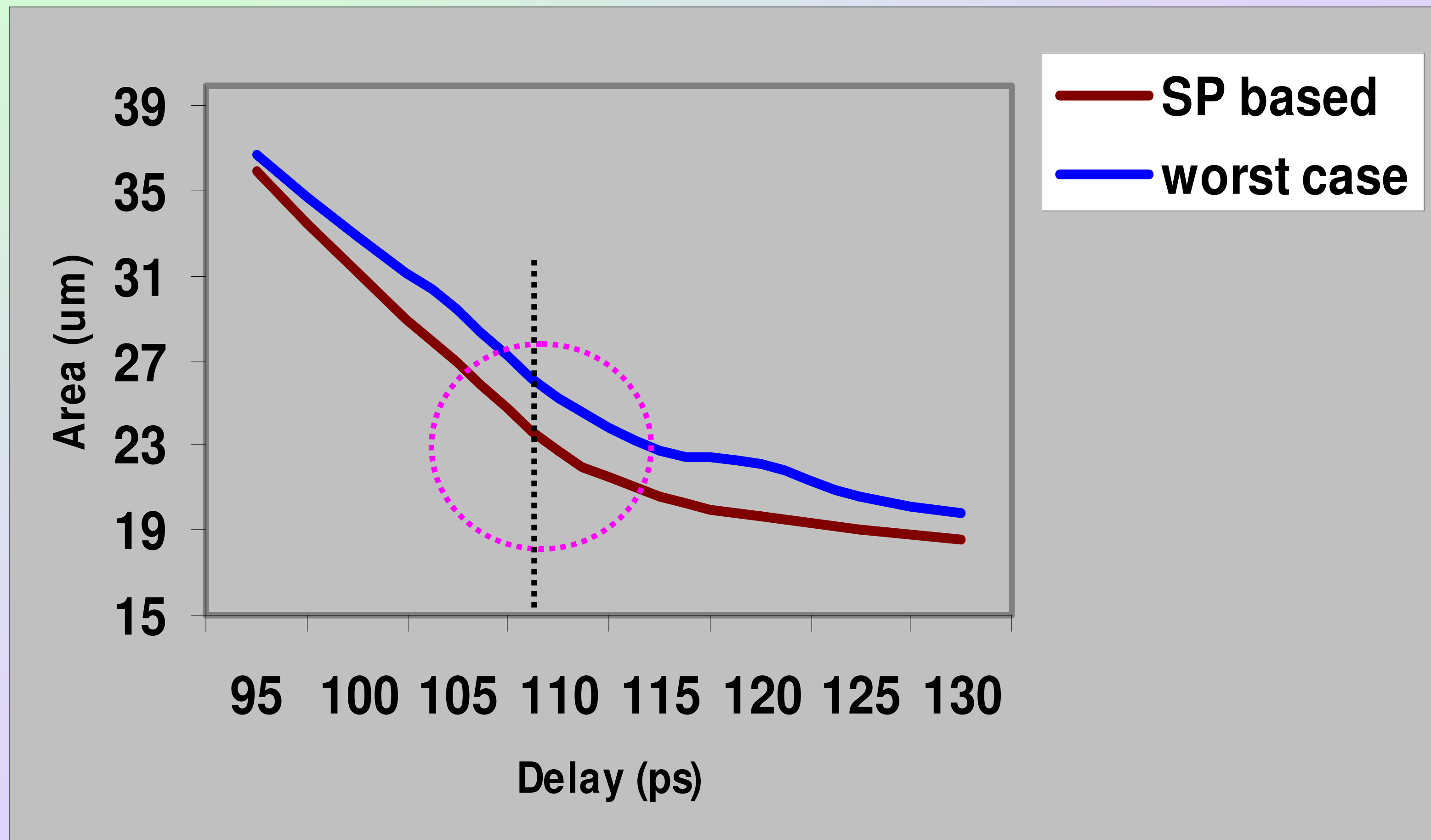
Nominal synthesis	Worst case synthesis	SP-based synthesis
Area = 7.4µm	Area = 11.6µm	Area = 9.8µm

Temporal Degradation of Circuits



Data for Benchmark C432

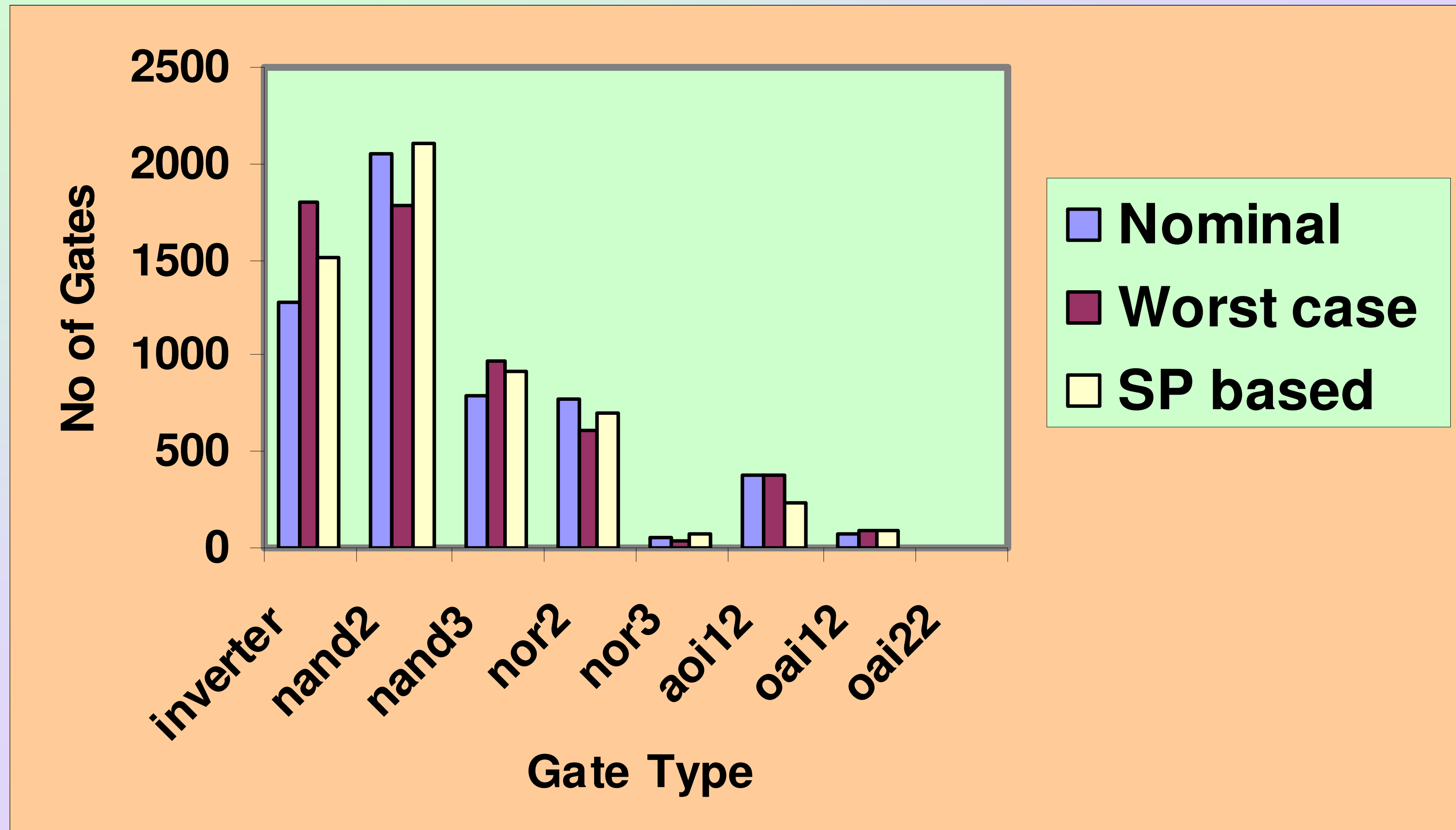
Area Delay Curve – Benchmark b1



Overall Savings

		Worst case		SP based			
Bench mark	Target Delay (ps)	Area (µm)	Power (µW)	Area (µm)	Area Savings (%)	Power (µW)	Power Savings (%)
C1355	735	1282	122	1052	18	99	19
C1908	860	1234	122	1192	3	117	4
C3540	1100	2570	256	2057	20	206	20
C6288	3200	4356	448	3817	28	387	14
alu2	923	760	74	691	9	65	12
des	620	8738	891	8657	1	866	3
alu4	940	1498	149	1302	13	126	15
vda	480	2088	243	1967	6	223	8

Distribution of Gate Types – Benchmark des



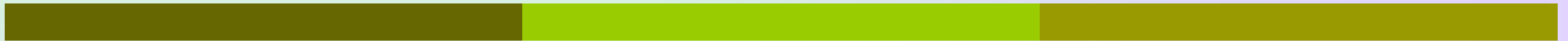
Summary

- NBTI (aging) in circuits causes delay degradation
- Need to relax timing or design NBTI-resilient circuits
- Area increase to counter effect of V_{th} degradation
- NBTI-aware optimal synthesis method presented
- Signal probability based design reduces pessimism, leads to area savings over "worst case" methods

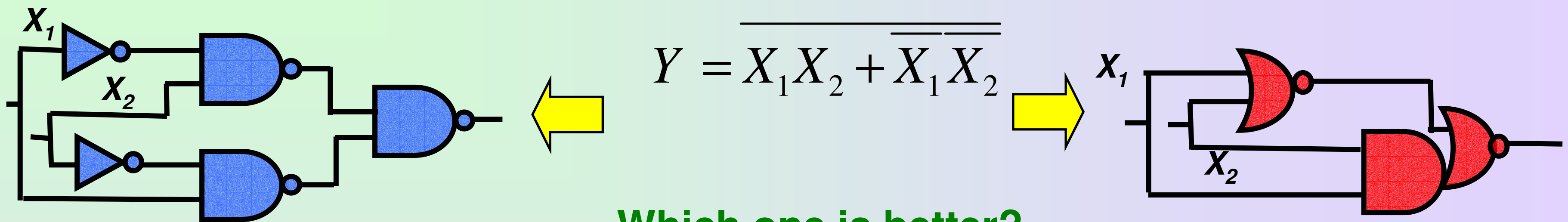
Thank You

Questions and Comments

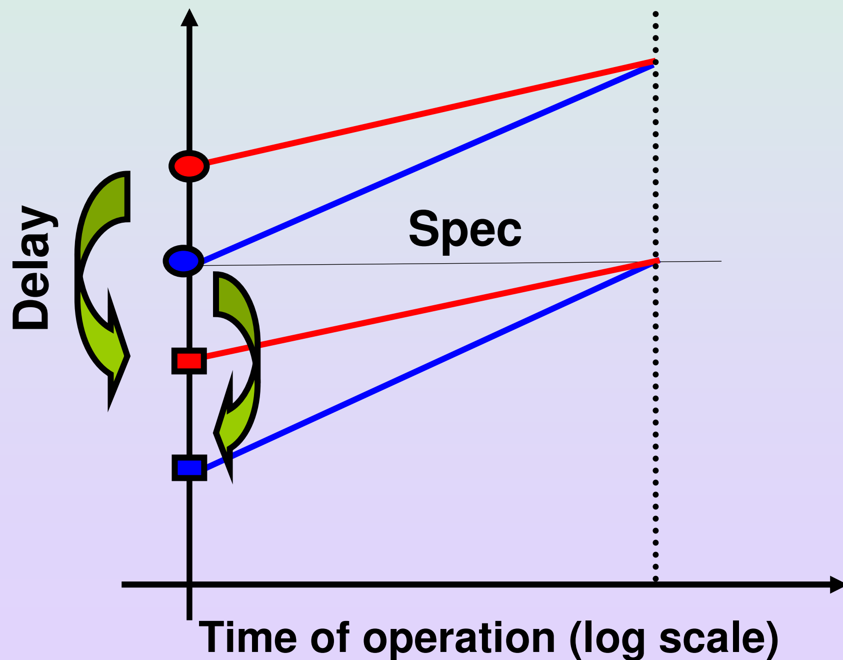
Backup

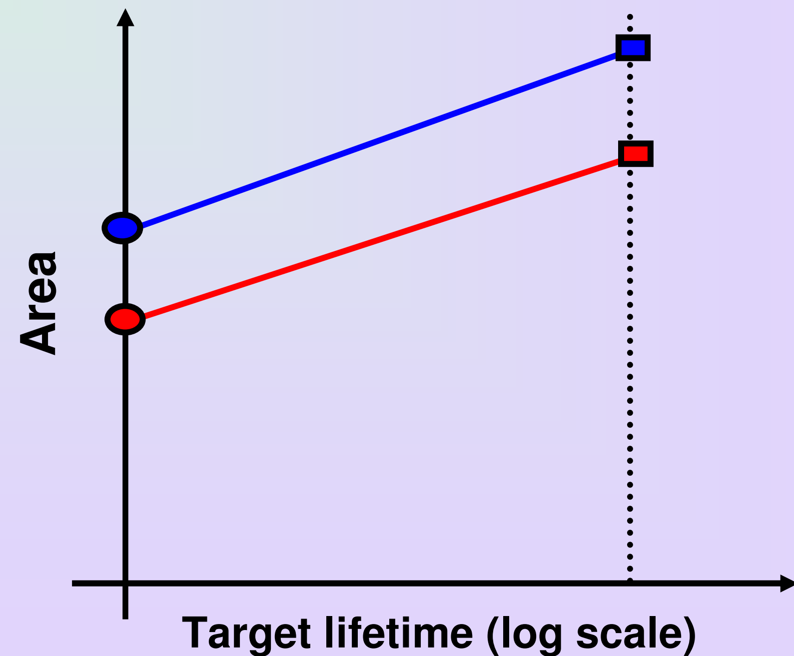


Synthesis versus Sizing



Which one is better?



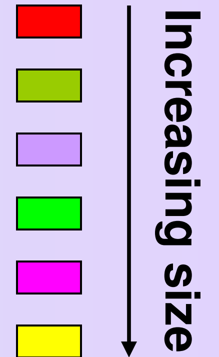


What if……

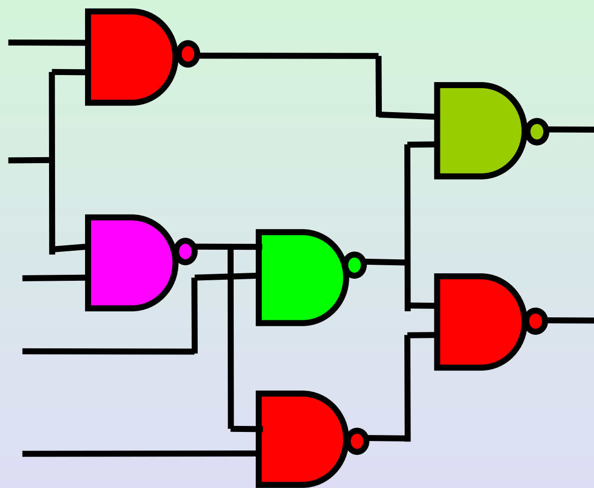
- Signal Probability (SP) of primary inputs not equal to 0.5
- SP values closer to the “worst case”

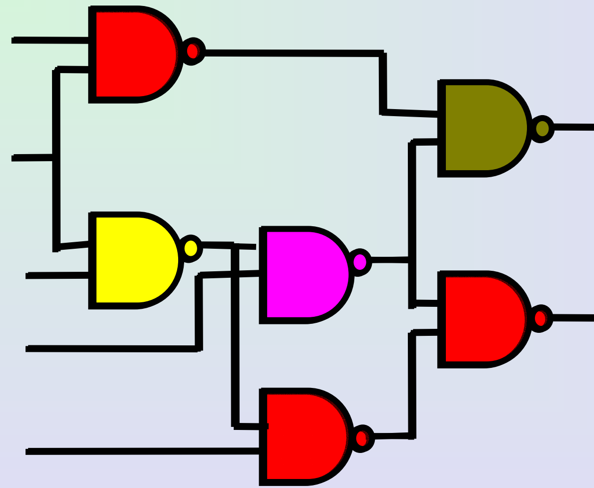
- Gain over “worst case” depends on library gates, sizes and SP distribution
- Still better than sizing approaches
- Can we set SP such that gain is maximized?

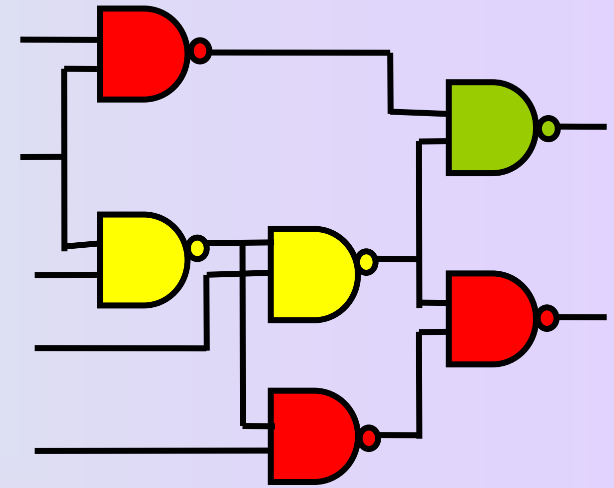
C17 – Synthesis with Different SP



T_{spec} = 70ps







0.5 SP-based synthesis

Area = 9.8µm

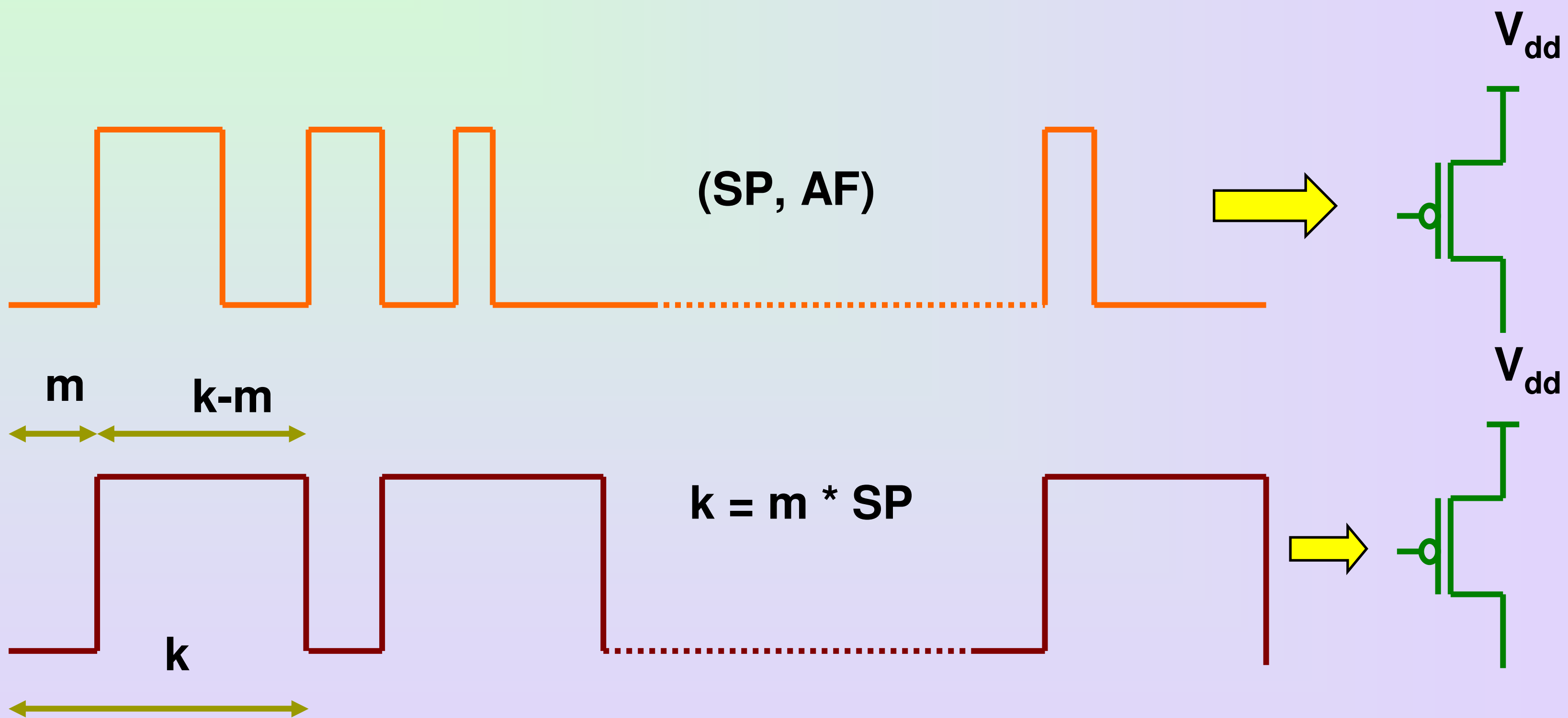
0.8 SP-based synthesis

Area = 10.8µm

Worst case synthesis

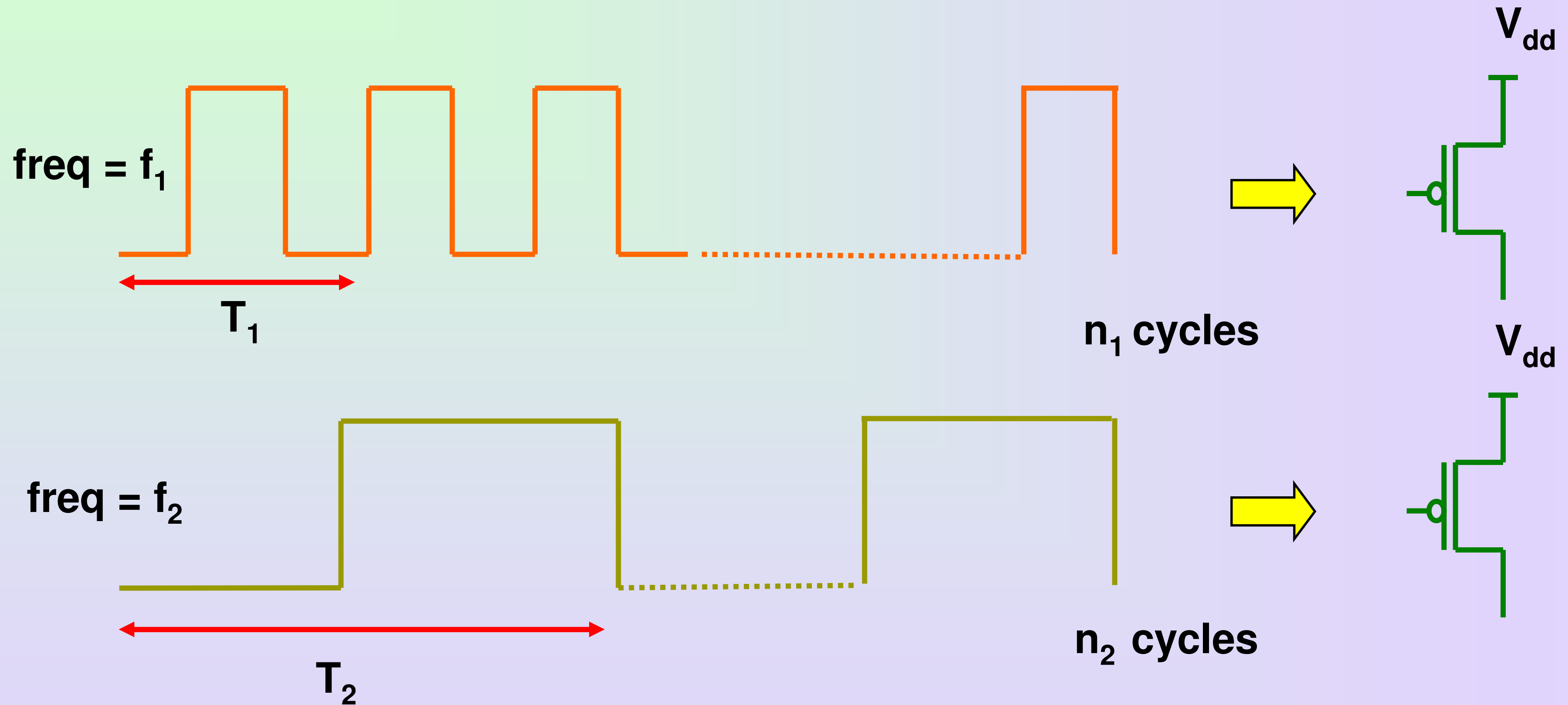
Area = 11.6µm

Converting Random Waveforms to Deterministic Periodic Signals



Interface trap count for both these waveforms are equal “asymptotically”

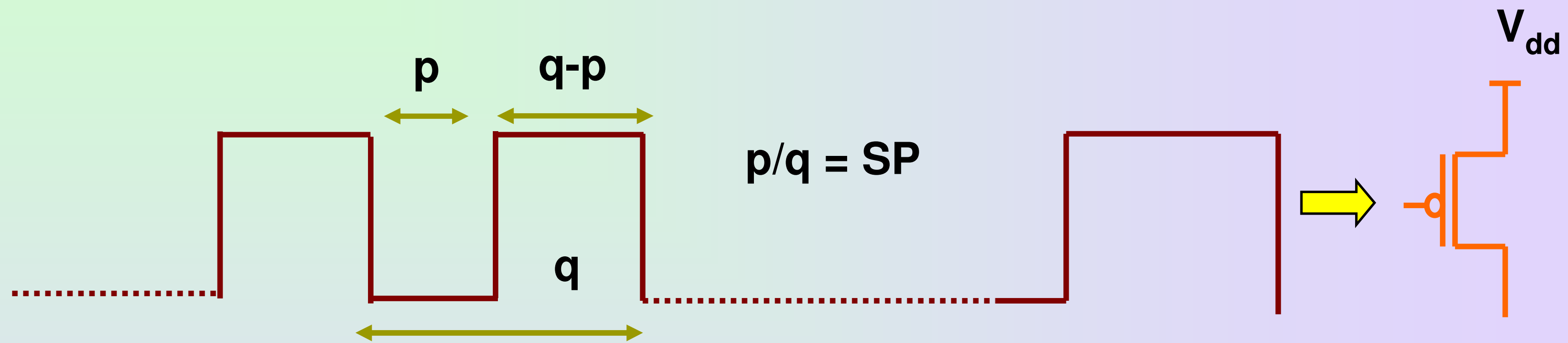
Frequency Independence



Number of interface traps for both cases same

Trap generation independent of frequency

"s_k" Notation – Multi-cycle Model



$$s_{k=nq+i} = \begin{cases} \left(i + s_{qn}{}^{6}\right)^{1/6} & 0 < i \le p \\ \dfrac{s_{nq+p} + s_{nq}\left(\dfrac{i-p}{2i}\right)^{0.5}}{1 + \left(\dfrac{i-p}{2i}\right)^{0.5}} & p < i \le q \end{cases}$$

$N_{IT}(kt_0) = s_k\, N_{IT}(t_0)$