A Switched-Capacitor CMOS Voltage Reference for Ultra Low-Voltage and Ultra Low-Power Operation

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Abstract—An ultra low-voltage and low-power CMOS voltage reference using subthreshold, body effect and switched-capacitor techniques is proposed in this paper. No resistor and BJT is used in this structure. The proposed circuit has been simulated with Chartered 0.18-µm CMOS process. The simulated results show that the voltage reference can operate with sub-0.6V supply and total supply current is 210nA at 0.58V supply. The temperature coefficient of 7.67ppm/℃ for a temperature range of -40℃ to 85℃ is achieved. The layout area is only 0.018 mm².

I. INTRODUCTION

Voltage reference is one of the basic building blocks in many applications of analog and digital circuits. With the expansion of the portable battery-operated environmental products market, small area, low voltage and low power are the key characteristics in mix-signal/RF systems nowadays, such types of characteristics drive a strong demand for the smaller area, lower supply voltage and lower power consumption voltage reference that can be implemented with a standard CMOS process [1]. In CMOS technology, parasitic vertical bipolar junction transistor (BJT) formed in a p- or n-well is widely used to implement a bandgap voltage reference [1], [2]. Unfortunately, for silicon, the reference voltage is around 1.25 V and common-collector structure of the parasitic vertical BJT and the input common-mode voltage of the amplifier are the major limitation to design an ultra low voltage circuit [3]. Such constraint can be overcome by using current mode [4], [5] and resistive subdivision methods [6] that allow us to get sub-1V operation. But these structures still require large-area parasitic BJTs with large turn-on voltage and resistors. A nanopower voltage reference generator [7] has been presented to solve these problems that without any BJT and resistor. But this structure has these defects: (1) the circuit has two high threshold voltage devices that will increase the cost of fabrication, (2) the process stability of this structure is worse than that of a bandgap reference and this structure does not have any trimming procedure, (3) the output reference voltage is unique if temperature compensation has been made. These problems will affect the application of this structure.

To address the above-mentioned design problems, an ultra low-voltage ultra low-power switched-capacitor voltage reference circuit has no BJT or resistor in a standard CMOS process, is presented in this paper. The key feature of it is that no high threshold voltage device is needed. The design techniques are presented in detail in the following sections.

II. PRINCIPLE OF THE PROPOSED VOLTAGE REFERENCE

The complete circuit of the proposed voltage reference is shown in Fig.1. The structure is composed of core circuit and switched-capacitor circuit.

A. Core circuit

The core circuit consists of forward bias circuit, current generator circuit and start-up circuit. Forward bias circuit is
composed of M5 and M6, which is used to forward bias the source-bulk junction to reduce the threshold voltages of the M7 and M9 [6]. Since the threshold voltage of a PMOS transistor is given by [6]

$$V_{thp} = V_{thp0} + \gamma \left( \frac{\sqrt{2}}{\phi_t} \right) \left( V_{SB} - \sqrt{2} \frac{\phi_t}{\phi_f} \right)$$

where $V_{thp0}$ is the threshold voltage with zero biased source-bulk voltage, $\gamma$ is the body bias coefficient, and $\Phi_t$ is the bulk Fermi potential. With this body effect technique, the threshold voltage can be reduced significantly. In order to avoid turning on the p-n junction of the source-bulk junction at the highest temperature, the forward bias voltage $V_{GS12}$ is set to about 0.3V at room temperature. At this time, the threshold voltages of M7, M9 and M11 transistors are about 220mV at room temperature and the temperature-dependent bulk current of these transistors are small enough to neglect.

The current generator circuit is made up of M1–M4, M7–M10, which generates the $I_1$ that is mirrored to $I_c$, such current is then injected into the diode-connected PMOS transistor M12 for temperature compensation. Transistors M1 and M2 compose the current mirror-impose equal current $I_1$ in M8 and M10. At the same time, transistors M3 and M4 compose the current mirror impose equal current $I_1$ in M7 and M9. All the transistors are standard digital MOS transistors with a threshold voltage of 245mV and -345mV for NMOS and PMOS at room temperature, respectively. To bias M8 and M10 in the subthreshold region, and, at the same time, to bias M7 and M9 in the saturation region. This situation is achieved by two different threshold voltages because of body effect technique. Except M8 and M10, all the transistors operate in the saturation region. Assuming the channel length is long enough and $V_{DS}>4V_T$, the I-V characteristics of a PMOS transistor in the saturation and the subthreshold regions can be approximated by (2) and (3) respectively [7], [8], [9].

$$I_D = \frac{\mu_p C_o W}{L} \left( V_{SG} - V_{thp} \right)^2$$

$$I_D = \frac{\mu_p C_o W^2}{L} \exp \left( \frac{V_{SG} - V_{thp}}{nV_T} \right)$$

Where $V_T$ is the thermal voltage, $n$ is the subthreshold slope parameter, $\Phi_B$ is the Bulk Fermi potential, $\epsilon_{si}$ is the permittivity of Si and $N_{CH}$ is the channel doping concentration. The gate-source voltages of M7 and M8 (M9 and M10) are identical, and M10 and M8 in subthreshold with drain current $I_1$ and M9 and M7 in saturation with a drain current $I_1$. Then, we have

$$|V_{gs1}| + nV_T \ln \left( \frac{I_1}{\mu_p C_o W^2 (W/L) / \Phi_2} \right) = V_{gs1}$$

$$|V_{gs10}| + nV_T \ln \left( \frac{I_1}{\mu_p C_o W^2 (W/L) / \Phi_2} \right) = V_{gs10}$$

where $W_X$ and $L_X$ are the width and length of MOSFET X. For the source-bulk junction forward bias voltages of M7 and M9 are same, the $V_{thp1}=V_{thp2}$. Assuming $W_1/L_1=W_9/L_9$, so $I_1=I_c$. Since $I_1=I_c$, $V_{gs1}=V_{gs10}$ and $V_{gs10}=V_{gs1}$, by subtracting (4) from (5), we can get the expression of the current

$$I_c = \frac{\mu_p C_o W/L}{2 \frac{(W/L)}{nV_T} \ln \left( \frac{L_2 / L_1}{W_2 / W_1} \right)}$$

The previous generated current $I_c$, given by (6), is then injected into the diode-connected transistor M12, that can generate a output voltage for temperature compensation. M12 operates in the saturation region and then by using (2) and (6), we can derive the output voltage

$$V_{SG12} = \frac{V_{gs12}}{\sqrt{(W_6/L_6)/(W_1/L_1)}} - 1 \ln \left( \frac{W_6/L_6}{W_2/L_2} \right)$$

According to the temperature variation characteristic of threshold voltage [7], [10], we can assume that the threshold voltage of an NMOS transistor linearly decreases with temperature. Since the second term of (7) is proportional to absolute temperature, if $W_1/L_1$, $W_6/L_6$, $W_2/L_2$, $W_10/L_10$ and $W_12/L_12$ are set in an appropriate value, the temperature compensation can be achieved and $V_{SG12}$ can be a temperature-compensated output reference voltage. Equation (6) can be achieved with temperature ranging from -40°C to 85°C by setting the source-gate voltages of M7, M8 and M9, M10 to 300mV and 260mV at room temperature, respectively.

Since the core circuit has two stable states, one state is the current given by (6), the other is zero current, a start-up circuit [11] composed of MS1, MS2 and MS3 is used to ensure that the first stable state is achieved.

B. Switched-capacitor circuit

The core circuit mentioned above can not be applied as a voltage reference generator because it does not have any trimming procedure and the temperature-compensated output reference voltage is unique. Switched-capacitor technique can solve the aforementioned problems [11], [12]. The switched-capacitor circuit is shown in Fig. 2. Transistor S1–S6 are the switches which are controlled by the non-overlapping clock signals $\Phi_1$, $\Phi_2$, $\Phi_3$. The amplifier is composed of MA1–MA5, it generates an output reference voltage $Vref$, which has been temperature-compensated, based on the source-gate voltage difference $\Delta V_{SG}$.

Transistors MA1, MA2 and MA4 compose a one stage cascode amplifier. MA3 and MA5 are used for boosting the transconductance of MA1 which can boost the gain of the amplifier. For the low voltage operation, all the transistors except MA4 and MA5 operate in the subthreshold region. MA4 and MA5 operate in the saturation region, their threshold voltages are reduced by body effect technique as same as M7, M9 and M11.

Assuming $V_{SG1}$ is the source-gate voltage when the current flowing through transistor M12 is $(M+1) \times I_c$ and $V_{SG2}$ is the source-gate voltage when the current flowing through transistor M12 is $I_c$. When $\Phi_3=0$ and $\Phi_2=1$, current injecting through transistor M12 is $(M+1) \times I_c$, the total charge at node X is $-V_{SG1 \times} V_{OS}(C_1+C_2)+V_{OS \times} C_3$, where $V_{OS}$ is the offset voltage of the amplifier. When $\Phi_1=1$ and $\Phi$
$z=0(\Phi^2\gamma=0)$, current injecting through transistor M12 is $I_c$, since there is no resistive path connect to $X$, the total charge at node node X that is equal to last clock phase. Then, we have

$$- (V_{S1} - V_{G1}) + V_{G1} = - (V_{S2} - V_{G2}) + V_{G2} + (V_{OS} - V_{ref}) + C_3$$

(8)

During this phase, we can derive the output reference voltage

$$V_{ref} = \frac{C_1}{C_3} (V_{S1} - V_{G1}) + \frac{C_2}{C_3} V_{G2} = \frac{C_1}{C_3} \Delta V_{S1} + \frac{C_2}{C_3} V_{G1}$$

(9)

Then, we have:

$$V_{ref} = \frac{C_1}{C_3} (V_{ref0}) + \frac{C_2}{C_3} (\sqrt{M+1} + \sqrt{M+1}) \frac{nV}{\sqrt{a}} \sqrt{\ln(c)}$$

(10)

where we have defined $a=(W_1/L_1)/(W_2/L_2)$, $b=(W/L_2)/(W/L_1)$, $c=(W_2/L_2)/(W/L_1)$. Then, we obtain

$$\frac{\partial V_{ref}}{\partial T} = \frac{C_2}{C_3} K_{VT} \left[ \frac{1}{a} - 1 \right] \frac{nV}{\sqrt{a}} \sqrt{\ln(c)}$$

(11)

where $K_{VT}$ is the temperature coefficient of $|V_{thp12}|$. Therefore, $V_{ref}$ can realize zero temperature voltage by properly choosing parameters $C_1$, $C_2$, $M$ and can be arbitrary value in theory by changing the value of $C_2$. $C_3$. By trimming $C_1$, $C_2$ and $C_3$, we can regulate for process variations to get a very low temperature coefficient and very high initial accuracy. Equation (10) shows that the offset voltage does not influence the output reference voltage $V_{ref}$ because it is stored on $C_3$. Therefore, the amplifier does not need the differential pairs input stage for low offset voltage. Moreover, clock signal $\Phi_1$ must turn switch S5 off earlier then switch S6, or $C_3$ will lose the offset charge.

C. Analysis of the minimum supply voltage

The minimum supply voltage is imposed by the core circuit and amplifier. The supply voltage must ensure every transistor do not operate in the triode region which should operate in the saturation region. Such supply voltage also has to ensure the $V_{OS}$ of transistors which should operate in the subthreshold region higher than $4V_T$. Hence, we have

$$V_{DDmin} = \max \{ |V_{GS9} + V_{DSS2} |, |V_{G59} + V_{DSS3} |, 4V_T + V_{GS1} + 4V_T, 4V_T + V_{GS4} + V_{DSS4} \}$$

(12)

where the first five item in the bracket represent the five branches of the core circuit and current output circuit consist of M11,M12 and M13. $|V_{GS9}|$ and $|V_{G59}|$ have set to 260mV and 300mV at room temperature, respectively, the $V_{DSS}$ is chosen about 100mV, and $V_{GS1}$, $V_{GS4}$ can be lower than 400mV. According to above-mentioned, the minimum supply voltage can be lower than 0.5V in theory.

III. SIMULATION RESULTS AND COMPARISON

To evaluate the performance of the design, the simulations based on Chartered 0.18-µm CMOS process have been carried out. With a clock frequency of 1 kHz, Fig. 2 (a) shows a timing diagram of $V_{ref}$ at multiple temperatures under the supply voltage of 0.58V. $V_{ref}$ is a temperature-compensated output reference voltage during the phase $\Phi_1$. Fig. 2(b) zooms in the timing diagram of $V_{ref}$ at multiple temperatures. Fig. 2(c) shows the temperature coefficient of the $V_{ref}$ during phase $\Phi_1$ is 7.67ppm/°C over the range from -40°C to 85°C under the supply voltage of 0.58V.

Fig. 3 (a) shows a timing diagram of $V_{ref}$ at multiple power supply. The same as Fig.2 (a), the $\Phi_1$ is the phase which $V_{ref}$ is a temperature-compensated output voltage. Fig.3 (b) zooms in the timing diagram of $V_{ref}$ at multiple power supply. Fig.3 (c) shows $V_{ref}$ variation is 5.6mV when the power supply varies from 0.58V to 2V during the phase $\Phi_1$.

In this work, total supply current include the amplifier is 210nA at room temperature when the power supply is 0.58V. Fig. 4 displays the layout of the proposed circuit, it shows the layout area is only 0.018 mm². Moreover, the comparisons among different voltage references are listed in Table 1. It can be noted that the proposed circuit has much lower supply voltage and smaller chip area. As compared with [7] and [12], the proposed circuit does not need extra high threshold voltage device. And, it also has a quite low temperature coefficient.
reference voltage varied only 7.67ppm/℃ for the temperature range of −40℃ to 85℃ and the line regulation is 3.94nm/V for a power supply voltage varies from 0.58V to 2V. The layout occupies only 0.018 mm² because this structure does not need any resistor and BJT. The power supply voltage can be sub-0.6V and the quiescent current is only 210nA at 0.58 V supply that lead to a very low power consumption. Using a simple S&H circuit, this structure is very suitable for low-voltage and low-power applications.

**Fig. 4. Layout of the proposed circuit.**

![Diagram](image)

**TABLE I. COMPARISON OF THE VOLTAGE REFERENCE**

<table>
<thead>
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<tr>
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<td>0.98V~1.5V</td>
<td>0.9V~4V</td>
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<tr>
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<td>2.2µA</td>
<td>18µA</td>
<td>0.04µA @0.9V</td>
<td>0.25µA @0.9V</td>
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<td>0.24 mm²</td>
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**REFERENCES**