Co-Design of Efficient Low Power Successive Approximation Quaternary Analog to Digital Converter

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Abstract—An implementation of quaternary logic in varied application areas which is based with orientation of successive adder is been proposed in terms of flip-flops performed with higher speed, considerable power optimization and precise organized processing is obtained in CMOS based arrangements of flip-flop such that scaling of values preamble with single digit based quaternary addition with circuits using Analog to Digital Converters (ADCs). Energy efficiency in SAR based VLSI based processor is necessary and been performed in terms of quaternary flip-flop. There is an optimization of power with increase of threshold voltage values in terms of its redundancy of bits. Design of quaternary flip-flop based optimization and quantization of Micro-Core based SIMD processor to achieve minimum rescaled value of resolution in terms of power optimization. This estimation of quaternary flip-flop based optimized values and enhanced data-transfer resulting in higher speed with power reduced to 0.675µW CMOS simulation in corresponding to its CMOS based design implementation.

Keywords: power optimization, CMOS, preamble, VLSI, SIMD, ADC, Micro-Core.

I. INTRODUCTION
As in terms of power dissipation in CMOS VLSI chips has been getting a serious problem in recent nanoscaling regime. Power density in VLSI chips is increased by k0.7, where k (> 1) is a device scaling factor, causing a doubling of the power dissipation every 6.5 years. It is assumed that the power dissipation in CMOS chips will increase steadily as a natural result of device scaling. From the viewpoint of the technology trend in special-purpose VLSI processors, its performance improvement is still strongly required in multimedia-application fields. Especially, large-scaled parallel arithmetic operations must be performed in such VLSI processors. Hence, energy efficiency is one of the most important factors in the recent high-performance VLSI processors. In order to solve the above problem, energy-efficient multi-core SAR VLSI processors have been intensively developed in recent era. In such energy-efficient VLSI processors, it is important to enhance the performance of their processing elements themselves with maintaining less power dissipation. On the other hand, it is known that one of the key circuit techniques for reducing power dissipation in a desired circuit is to use Adder parameters with multiple-valued current-mode circuitry. Since the use of the differential-pair ADC circuit makes input voltage swing small yet circuit driving capability high, the rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuits with respect to DAC.

II. PROBLEM REVIEW
In terms of their processing elements (PE) based complexity to single digit based quaternary SAR based addition is been seen under power optimization with latch in build master for error quantization for comparing as well as storing [1] [2]. Though the reduction of errors is constrained to about 55 to 65% with reference to Micro-Core SIMD processor [2][3].

III. PROBLEM DEFINITION
As is considered to reduce the delay for the precision in processing of SIMD based processor it is required for Vertical (V-Channel) and Horizontal (H-Channel) [2] [5] [6] optimization with power optimization and increase in speed with respect to gates for various quaternary states. Providing low power with increased threshold voltage VT as in terms VT >> P_{optimized} (reduced).

IV. PROBLEM ANALYSIS
There is a consideration of sates in terms of values having a symmetrical value in terms of its transition from absolute low< medium low< medium high< absolute high.

V. OBJECTIVES
Design of processing element using Quaternary differential logic [4]. Under this objective, different processing elements are designed for MP-SOC SIMD processor [3] [8] [9]. With reference to master latch and threshold detector the variation of power in terms of its optimized values is obtained from 1.0V to 3.0V which is pre-scaled from 0.39V to 0.49 V at 0.675µW for conversion under ADC level triggered.

VI. DESIGN ANALYSIS
As there is an implementation of basic gates for implementation of Quaternary D flip-flop provided for threshold detection [5] [10] referred to master latch confined with its slave latch CMOS based output generator of V-Ch and H-Ch based CMOS [3] format as shown in reference to Figure 1 and Figure 2.

VII. METHODOLOGY
It has been seen as in CMOS based implementation from the master latch to slave latch [7] [12] [14] there is considerable increase in its threshold values such that V_{T1}>V_{T2}>V_{T3} considerable speed is increased with respect to G output and G inverted output thus, optimizing the power at a reduced rate [5] [16] as shown in reference to table below Table 1.
When the MVs (Multi Valued) quaternary values are been considered in terms of its master latch and threshold detectors [8] with respect to latch inverter at 3.0 V with considerable clock pulse there is optimization [6] of time period as speed rate is been increased with respect to the Figure 3.

VIII. TOOLS USED
In terms of various simulations an integrated environment based with Tanner Tools is been used compatible with operating systems based on 32-bit Windows XP, Windows 7 with supported DOS environments.

IX. FEATURES
1. Increased bus efficiency [17].
2. Less area with increased complexity.
3. Reduced chip area.
4. Higher radix -4 number system has redundancy [18].

X. EVALUATION RESULT
Constrained with the respective dynamic values of MV contained in terms of PE [2][3] we consider that

\[ P = VR \]

Equation (i)

Then considering the relative values of power with accuracy of single bit addition for CMOS based values up to \( \pm 0.06 \) to \( \pm 0.04 \) as shown in table 2 depicted with Figure 4 below obtains the result of simulations 1 and 2. Thus, the dynamic resistance values obtained for the CMOS based quaternary logic is \( R_1 = 3.2 \mu \Omega \), \( R_2 = 2.4 \mu \Omega \) and \( R_3 = 1.4 \mu \Omega \).

Table 1. Quaternary values with provided outputs (G1, G2)

<table>
<thead>
<tr>
<th>( V_{gr} )</th>
<th>( (Q_1, Q_1') )</th>
<th>( (Q_2, Q_2') )</th>
<th>( (Q_3, Q_3') )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.1</td>
<td>0.1</td>
<td>0.0</td>
</tr>
<tr>
<td>1</td>
<td>1.0</td>
<td>0.1</td>
<td>0.0</td>
</tr>
<tr>
<td>2</td>
<td>1.0</td>
<td>0.1</td>
<td>1.1</td>
</tr>
<tr>
<td>3</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Table 2. Threshold Voltage vs. Power

<table>
<thead>
<tr>
<th>Threshold Voltage</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.39 v</td>
<td>1.24 ( \mu W )</td>
</tr>
<tr>
<td>0.45 v</td>
<td>1.07 ( \mu W )</td>
</tr>
<tr>
<td>0.49 v</td>
<td>0.675 ( \mu W )</td>
</tr>
</tbody>
</table>

XI. CONCLUSION AND FUTURE SCOPE
A high-performance PE using quaternary differential logic is proposed for a multi-core SIMD processor with successive addition is been obtained under ADC to DAC optimization initially shown in Figure 5. The rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuit. In fact, the power dissipation and VLSI based MP-SOC counts of the proposed PE based MEs [5][6][9], respectively, under almost the same delay in comparison with those of the two-bit binary DAC CMOS implementation. By using multiple-valued current-mode logic, the complexity of wires would be reduced, which could result in higher-speed with reference to dynamic scaled data transfer.

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Figure 1. Block diagram of a SAR ADC

Figure 2. Quaternary D-flip flop

Figure 3. Block diagram of SAR based Master Latch
Figure 4. Schematic of SAR ADC- DAC based Master Latch

Figure 5. Obtained Initial Output of DAC