Development of a Digital Tool for the Simulation of a Readout System Dedicated for Neutrons Discrimination

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Abstract—The development of a digital tool dedicated for the test and simulation of a reading system for neutron detection is presented. This study takes place in the framework of the I_SMART* European project. This system will have to work in harsh environment in terms of temperature and radiations what makes necessary the development of specifications for operation and reliability of the components and also the investigation of margins of interplay of the components. The specifications of the implemented tool are presented here with the different results of simulation related to the input designed parameters of the readout system.

Index Terms—Particles detector, readout chain, digital processing, Analog to Digital Convertor, Multi-Channel Analyzer.

I. INTRODUCTION

In order to ensure a high level of safety in operation in harsh environment where sources of radiation are present, it could be necessary to place one or many detectors as close as possible to the source to control the operative space.

In recent years, radiations detectors that are based on semiconductor materials have received considerable attention due to their compact sizes and their fast charge collection time in comparison with other types of detectors (gas filled) [1]. Crossing a semi-conductor detector (p-n junction for example), a particle delivered by a source of radiation will generate a number of electron-holes pairs proportional to its own energy [2]. Then, electrons drift within the semi-conductor and diffuse towards a collecting anode inducing an output current [1]. Thus, a single event effect can occur, which differs from cumulative effects (dose effects) that are linked to the presence of oxide in the component [2]. Since the amplitude of the currents is so low that it cannot be directly exploited, one or many pulse processing chains are then necessary in order to identify the incident particle.

The majority of the existing processing chains are providing a direct reading of the input current and are mainly composed by i) blocks ensuring amplification, based on a charge sensitive amplifier (CSA), ii) pulse-shaping that is ensured by a pulse shaping amplifier (PSA) iii) an analog to digital conversion (ADC) which provides a digital data ready to pass on to iv) digital signal processing (DSP) [3],[4].

This study takes place in the framework of the I_SMART European project. The final I_SMART system will consist of one or more detectors in silicon carbide (spectroscopic detector, neutron, gamma …), processing chains and microprocessor for the signal recognition. This system will have to work in harsh environment in terms of temperature and radiations. This makes necessary the development of specifications for operation and reliability of the components and the investigation of margins for the interplay of the components. In a previous study, first investigations on the feasibility of integration of the system under harsh conditions have been presented [5]. A first prototype (system approach) of the pulse processing chain based on a direct reading of the generated currents was characterized and evaluated. First evaluations of the designed system have shown a high sensitivity, high resolution and a good linearity of the response.

In this context, a digital tool, dedicated for the simulation of the global system, has been developed in order to generate a prototype able to evaluate the response of the processing chain, related to different input designed parameters of the system. Then this tool allows to test different solutions and to investigate the margins of interplay of the several components of the readout chain.

The rest of the paper is organized as following: The global processing chain is presented in section II. Section III is devoted to analog to digital conversion concept and section IV focuses on the characterization of the developed tool. Last part is devoted to the conclusion.
II. PRESENTATION OF THE PROCESSING CHAIN

The processing of the input current delivered by the sensor is divided in an analog processing followed by a digital processing. The analog processing which is ensured by a readout chain composed by several blocks will provide an analog image of the deposited energy related to the incident particle. Then, the digital processing which is ensured by an analog to digital convertor, a pile up rejector and finally a multi-channel analyzer (MCA) will provide a detailed spectrum related to the input energies of the detected particles [3].

A. Analog Processing (CSA+PSA)

The analog processing chain is composed by a charge sensitive amplifier (CSA) (Fig. 1) followed by a pulse shaping amplifier (PSA) (Fig. 2). The CSA will convert the deposited charge in the sensor to an output voltage. The PSA will work as a bandwidth filter which is added in order to reduce the noise contribution of the CSA and improve the signal to noise ratio (SNR) of the analog chain [5]. The SNR is the most important output parameter of the analog chain since it presents the level of digital resolution that can be ensured by the system.

\[ SNR_{db} = 6.02 N + 1.76 \]  

(1)

Where \( N \) defines the digital resolution.

The output of the PSA is a semi-Gaussian pulse presented in Fig. 3.

B. Digital Processing (ADC+MCA)

As mentioned previously, the digital processing chain is responsible of the analog to digital conversion of the input analog data that is ensured by the ADC, the detection and rejection of the pile up events, and finally the discrimination of the deposited energies which is provided by the MCA and presented as a detailed output spectrum.

Thus, the ADC placed on the head of the digital chain is without doubt the most critical and important component since it is responsible to provide a digital output with extremely low additional noise, high linearity and high sensitivity.

III. ANALOG TO DIGITAL CONVERSION

Several architectures of analog to digital convertors can be found in the literature (Fig. 4). Depending on the need, the choice of the appropriate architecture can be based on several parameters. We have chosen in our case to work with a Sigma-Delta convertor because of its high resolution and its facility to implementation since it is composed by only one comparator contrary to the Flash convertor for example that needs a very high number of comparators.
The Sigma-Delta convertor is composed by two blocks, a sigma –delta Modulator that will convert the analog input to a one bit digital output and a decimation filter that will increase the resolution of the final output data [6], [7].

### A. Sigma-Delta Modulator

Basically composed by integrators, a comparator, and a digital to analog convertor (DAC) (Fig. 5) the delta sigma modulator will have to decrease the noise quantification level and so improving the signal to quantization noise ratio (SQNR) of the ADC [6]. A maximum SQNR is needed in order to inhibit the limitation of the SNR generated by the analog processing chain.

Thus, the principle of operation of a Sigma-Delta modulator is characterized by the oversampling concept [6], [7], [8]. A higher sampling frequency will increase the bandwidth of the input signal and so limiting the amount of noise generated by the quantization that will be distributed on a higher volume. The oversampling ratio (OSR) can be presented as:

\[
OSR = \frac{F_s}{2 \times BW}\tag{2}
\]

Where OSR is the oversampling ratio, 

\(F_s\) is the sampling frequency,

\(BW\) is the bandwidth of the signal.

Moreover, after oversampling, integrators will work as a high pass filter which will push the noise at higher frequencies as well as the number is larger. So, the oversampling ratio and the number of integrators are the most important parameters for the design of the Sigma-Delta modulator and especially for the output generated SQNR.

As mentioned in (1), the digital resolution that can be provided by the ADC is then directly related to the generated SQNR. In order to ensure a resolution higher than 10 bits, an SQNR higher than 62 dB must be provided. However, we can affirm from Table I that designing an ADC with a good SQNR is not an easy issue: First, an OSR of 16 is eliminated since it cannot provide ten bits of resolution whatever the number of integrators. Second, for an OSR of 32 and 64, 2 integrators at minimum are required in order to achieve a good resolution. Thus, a high SQNR can be achieved only with a very high OSR, that requires a very fast clock and at minimum 2 integrators.

### B. Decimation

After modulation, a decimator filter is needed in order to remove the noise that had been pushed to higher frequencies and increase the resolution of the ADC. The filter will decrease the sampling frequency to the original one (Nyquist frequency) [7], [8]. A Cascaded Integrator Comb (CIC) filter is used for decimation.

Thus, the output digital data with a high resolution is now ready for further digital processing. One of the important treatments that is provided is the pile up rejection. The digital proposed solution consists on detecting the pulse width at half maximum of every Gaussian pulse and comparing it with a standard value which is the same whatever the input energy. If the measured value is greater than the standard one, a pile up event (Fig. 6) is detected and has to be removed. Then the remaining pulses will be passed to the multichannel analyzer (MCA) which will detect the channel corresponding to the amplitude of the Gaussian input.

The number of channel is proportional to the resolution provided by the ADC and is equal to \(2^N\) where \(N\) is the resolution of the ADC. So, the corresponding channel will be incremented by one for each detected particle. As explained in [5], the amplitude of each Gaussian pulse is directly linked to the deposited energy of the particle.
Thus, since each channel is related to an amplitude value, a given channel will correspond to a definite level of energy.

IV. CHARACTERIZATION OF THE DEVELOPED TOOL

In order to investigate the margins of interplay of the different components of the detection system, a digital tool has been developed using MATLAB. This tool gives the possibility to simulate and test the response of the system versus the designed parameters of each block presented in section III. Then, a graphic interface related to this tool has been created (Fig. 7). This interface is composed by three pages: the first page allows the simulation of the output of the analog part of the chain, the second page is dedicated to the simulation of the ADC and the last page allows a global simulation of all the system with the pile up rejection and the multichannel analyzer (MCA). Thus, a fast sizing of the readout system is provided with possibility of modeling the input signals, image of the currents generated by the sensor.

A. Simulation of the Analog Chain

This page contains 3 different panels:

- A panel allowing the control and the choice of the input spectrum distribution necessary to test the response of a given solution. Five channels can be chosen for different values from 1 to 1024 (considering the best case where the conversion will provide 10 bits of resolution). Moreover, the width of each chosen channel can be also defined, allowing to the spectrum to be more distributed (Fig. 8).

- A panel permitting the simulation of the output of the analog blocks (CSA+PSA), image of the current generated in the sensor due to a new particle crossing.

Three different parameters can be controlled and modified which are the length that presents the duration of simulation expressed on seconds, the percent parameter that presents the probability of apparition of every pulse (This parameter controls the random generation of the pile up events) and finally the offset parameter that permits the shift of all the generated pulses if needed.

The equation used to describe the Gaussian pulses form is:

\[
V_{out}(t) = \frac{Q}{e^2} e^{-t/\tau_f} \frac{A^n}{n!} \frac{L}{\tau_p} e^{-nt/\tau_p} \tag{4}
\]
Where Q is the deposited charge in the sensor, $C_f$ is the feedback capacitance of the CSA, $\tau_f$ is the time constant of the CSA, A is the DC gain of the integrators of the PSA, $n$ is the number of integrators, $\tau_p$ is the peaking time of the Gaussian pulse.

A series of Gaussian pulses are then generated which are related to the specified channels values that have been chosen previously. The duration of each pulse is about 10 $\mu$s and every two successive pulses are shifted by 1 $\mu$s. Since the percent parameter will define the probability of appearance of every pulse, the higher this value is, the higher the occurrence of pile up events will be.

- The final panel permits the visualization of the output Gaussian pulses of the analog block distributed on the chosen length (Fig. 9).

B. Simulation of the Sigma-Delta Modulator

Once the CSA-PSA output is generated, the different pulses will pass to the ADC for the conversion and further digital processing. So, the second page of the graphic interface is dedicated for the Sigma-Delta modulator design. Different parameters can be chosen and defined manually which are the OSR, the number of integrators, DC gain and time constant of every integrator and the quantization levels. Then, a specific button will launch the simulation and allows the frequency visualization of the Sigma-Delta modulator designed from the input parameters (Fig. 10). Moreover, as outputs, several parameters will be calculated and appeared which are: the SQNR, the Nyquist frequency ($2 * BW$ of the signal), the oversampling frequency and the slew rate of the modulator.

C. Global Simulation of the whole System

Finally, the last page is dedicated for the global simulation starting from the input generated spectrum until the pile up rejector. Five buttons are available permitting the launch of the simulation related to every treatment:

- Generate random series: This button allows the visualization of the spectrum of the generated pulses specified in the first page of the graphic interface.

- Conversion: This button will convert the Gaussian pulses issued from the CSA-PSA into a pulse density modulation using the Delta-Sigma modulator designed on the second page.

- Decimation Filter: Launches the decimation operation of the Sigma–Delta modulator outputs. The order of the CIC decimator filter can be specified manually.

- Interpolation: The pile up rejection treatment requires a high number of samples in order to correctly find the pulse width at half maximum of every pulse. However, since the decimation operation will decrease the oversampling frequency and so the number of samples, an interpolator filter has to be added in order to improve the precision of the pulse width at half maximum detection. A CIC interpolator filter is added and the order of the filter can be chosen manually.

- Pile up rejection: Finally, the operation of rejection of the pile upped events can be launched by this button. The pile up rejector will detect the pile upped events and remove them and only the correct pulses will pass the MCA for discrimination.

An example of simulation is presented here: the generated pulses are about 100 pulses with a percentage of pile up about 50%. The input spectrum is presented on Fig. 8.

![Fig. 9. Example of simulation of the output of the CSA-PSA block (Gaussian pulses).](image)

![Fig. 10. Frequency visualization of the Sigma-Delta modulator.](image)
From Fig. 11, we can remark a strong variation of the output spectrums in comparison with the input one shown in Fig. 7. First, for the red one that presents the output spectrum without pile up rejection, we can remark that the number of particles in low channel values has decreased. This is due to the pile upped events that have generated pulses with higher amplitudes which will correspond to higher channel values. Moreover, saturation is visibly clear in the last channel due to the exceeding of the alimentation value for high number of overlapped pulses. Therefore, a pile up rejection is required to prevent this kind of problems. The output spectrum of the MCA with pile up rejection is presented in yellow in Fig. 11. In comparison with the red one, important remarks can be deduced: First, the saturation event had been detected and deleted by the pile up rejector. Moreover, since there are some pile uped pulses whose amplitude did not exceed the alimentation value, we can remark that these events had been found and removed from the corresponding channels inducing a little diminution of the total number of the detected particles.

V. CONCLUSION

The presented work is based on the development of a new digital tool dedicated for the global simulation of a readout system for neutrons discrimination. The aim is to test the response of the processing chain for different input parameters related to the input signal and the ADC specifications. In a first time, we have presented and detailed the two types of treatments that will be applied to the current generated by a detecting sensor. Then, the analog to digital conversion concept was characterized by detailing the several blocks of the chosen ADC. Finally, the developed tool was totally detailed by characterizing the used graphic interface page by page. The results of the several treatments were also presented and commented.

Since the system has to work later in harsh environment in terms of radiations and very high temperatures, an ADC providing ten bits of resolution may be a critical issue. Thus, the perspectives of this work are to simulate the global system with lower digital resolution in order to define the eventual limits of harsh environment integration.

REFERENCES