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Using Redundancy to Break the Link between Accuracy and Speed in an ADC

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Abstract – Analog redundancy breaks the link between accuracy and speed in analog circuits. This technique has particular relevance to analog to digital conversion. As feature size and supply voltage shrink, calibration based on redundancy of flash analog-to-digital converters is becoming attractive. This new scheme allows accuracy to be achieved through the use of redundancy and reassignment, effectively decoupling analog performance from component matching. Very large comparator offsets (several LSBs) are tolerated, allowing the comparators to be small, fast and power efficient.

INTRODUCTION

Almost all analog-to-digital conversion techniques depend on component accuracy or accurate component matching. Conversion techniques that rely on matching are preferred, since variations in processing and in temperature can significantly affect absolute component values. Most integrated converters rely on accurately matched transistors, resistors or capacitors. Careful layout minimizes offset, however even optimally placed devices suffer from random mismatch. Often this random matching error is related to component area. For MOSFETs and capacitors, mismatch is dominated by area related terms [1]. Improved accuracy can be achieved though the use of larger components but this invariably results in increased power consumption [2]. Calibration or trim techniques are often used as an alternative means of achieving accuracy. Production trim is expensive and only viable for high margin parts. Analog calibration techniques, along with analog processing in general, are becoming increasingly difficult to implement in advanced, low voltage CMOS processes. Techniques that rely on digital processing are more attractive. Here we describe a technique based on analog redundancy and simple digital processing.

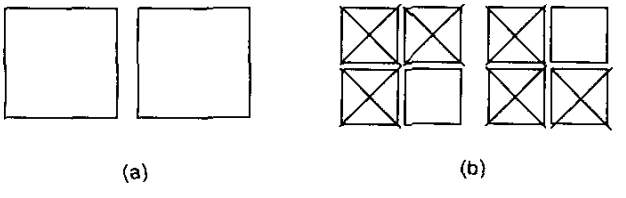

Fig. 1. Accurate matching can be achieved by (a) using a pair of large devices or (b) by selecting a pair of devices from a group of the same total area.

The basic concept of redundancy is illustrated in Fig 1. Adequate matching can be achieved through the use of sufficiently large component values (Fig 1(a)). Alternatively, a pair of accurate components can be selected from an array of smaller, less accurate components (Fig 1(b)). In principle, the latter approach is far more efficient since smaller devices have smaller parasitics, and only the selected components are used in the active circuit. Redundancy can be applied in almost any ADC architecture. In this paper, we discuss the use of redundancy in a flash ADC.

ANALOG REDUNDANCY IN A FLASH ADC

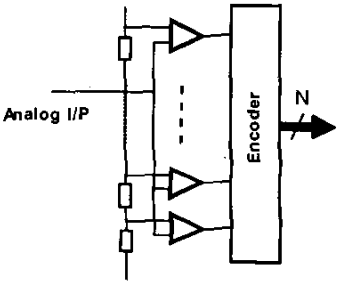

Fig. 2. Traditional flash ADC

Comparator offset must be controlled to avoid non-monotonicity or large errors in flash ADCs. Traditionally in CMOS, this is accomplished through device sizing (i.e. larger devices) [1],[3] offset nulling [3],[4] averaging, and digitally-controlled trimming. Offset nulling techniques, often implemented with the help of switched-capacitor (SC) offset-cancelled preamplifiers, are more power efficient [3]; however, these techniques may not allow continuous conversion and SC circuits are difficult to implement in low-voltage processes. Preamplifier output offset can be reduced through spatial filtering [5]. In another technique, digitally-controlled currents cancel comparator offset. We propose digital calibration based on comparator redundancy and simple digital processing to cancel offset. This technique allows good performance to be achieved in the presence of large comparator offsets, without preamplifiers or analog-

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offset cancellation. Earlier in [6], we presented a 6 bit prototype ADC along with experimental results.

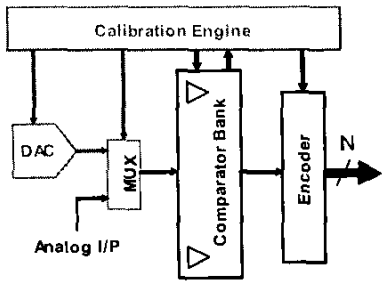

Fig. 3. Block diagram of a flash ADC calibrated with redundancy

In a traditional N-bit flash ADC (Fig. 2), the input voltage is quantized by 2^N-1 comparators, with monotonically increasing, trip-voltages. The outputs of the comparators form a *thermometer* code that is encoded to give the N bit output of the converter. A block diagram of the flash ADC with calibrated redundancy introduced by the authors in [6] is shown in Fig. 3. Instead of 2^N-1 comparators, the ADC has a bank of R(2^N-1) comparators, with R comparators assigned to each code. During a calibration sequence at power-on, a finite state machine (the calibration engine) directs the search of the entire bank of comparators for the most suitable comparator for each code. Throughout this search, the resistor ladder is configured as a resistor digital-to-analog converter (DAC) and generates test input voltages to the comparators. During calibration, a MUX connects the output of the resistor ladder DAC to the input of the comparator bank, while in normal operation, the ADC analog input is connected to the comparators.

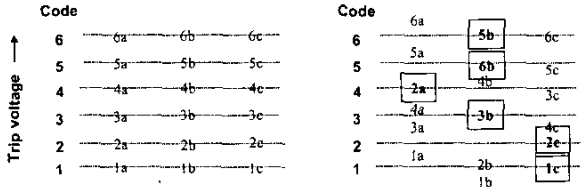

Fig. 4. (a) Ideal and (b) an example of actual trip voltages in a flash ADC with 3 comparators per code.

Fig. 4. shows an example with R equal to 3. Fig. 4(a) shows the nominal trip-voltages with the trip-voltage of each of the R comparators for each code at the ideal value. In practice, the comparator trip-voltages differ from the ideal trip-voltages because of offsets caused by device mismatch. Fig. 4(b) shows an example of actual comparator trip-voltages. The trip-voltages of the comparators that are selected from the bank of comparators are high-lighted. For example, comparator 1c is chosen to represent code 1, and comparator 3b represents code 3. It should be noted that a comparator may be selected to identify a code other than the one associated with its nominal trip voltage. To illustrate this, again referring to the example in Fig. 4(b), we see that comparator 2a is reassigned to represent code 4. Comparator reassignment is an important part of the overall technique.

To summarize, 2^N-1 comparators are chosen from a bank of R(2^N-1) redundant comparators. Comparators may be reassigned to represent codes other than those associated with their nominal trip voltages. Instead of a traditional thermometer encoder, a *counting encoder* [6] is better suited to the scheme since such an encoder handles comparator reassignment transparently.

ANALYSIS

We use an approach similar to that applied by Pelgrom et al. in their analysis of a conventional flash ADC [3] to estimate the yield of a flash ADC that incorporates redundancy. Because of random comparator offsets, the actual trip-voltages will not be uniformly spaced and may not increase montonically. If redundancy is introduced, then the probability p of not finding a trip-voltage within the tolerated range of DNL values is reduced. If there are R comparators per code, then the probability p and the yield become:

$$p_k = \prod_{i<k}^{2^N-2} [P(|V_{x,i} - V_{x,k} - 1LSB| > DNL_{max})]^{R-1} \times \prod_{i>k}^{2^N-2} [P(|V_{x,i} - V_{x,k} - 1LSB| > DNL_{max})]^{R}$$

$$Yield = \prod_{k=1}^{2^N-2} (1 - p_k) \quad (1)$$

This estimate accounts for trip-voltages that have already been allocated by assuming that fewer trip-voltages are unassigned for codes below k.

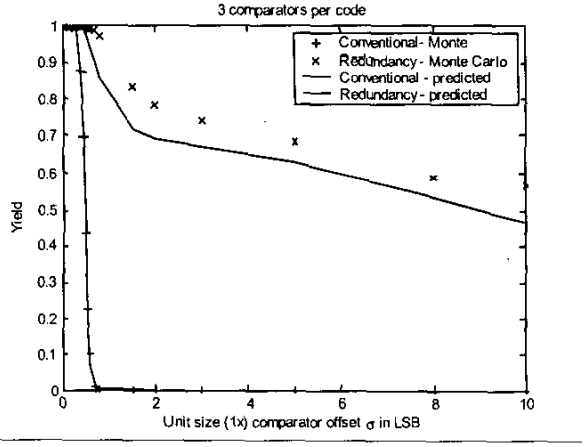

Fig. 5. The predicted yield and that found through Monte-Carlo analysis for 3 comparators per code in a 6 bit ADC. The yield of a conventional ADC of the same total comparator area is also shown. A good ADC has DNL values between -1 LSB and 1 LSB.

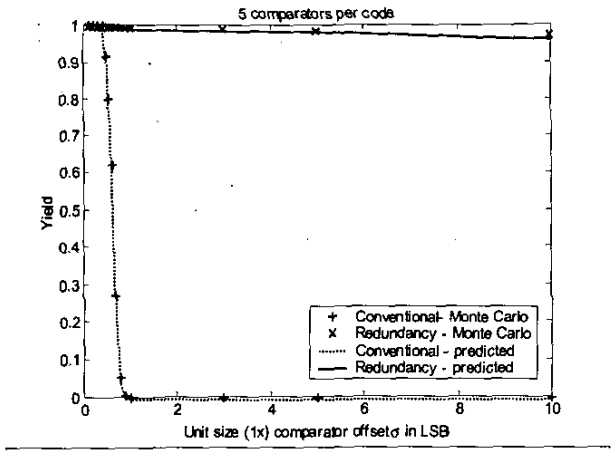

Fig. 6. The predicted yield and that found through Monte-Carlo analysis for 5 comparators per code in a 6 bit ADC. The yield of a conventional ADC of the same total comparator area is also shown for both cases. A good ADC has DNL values between -1 LSB and 1 LSB.

Fig. 5 and 6 compare the yield predicted by equation (1) with the yield determined by Monte-Carlo analysis for a 6 bit ADC. In this comparison, a good ADC has a worst case DNL greater than -1 LSB and less than 1 LSB. These plots show that the prediction of yield is good over a range of redundancy values.

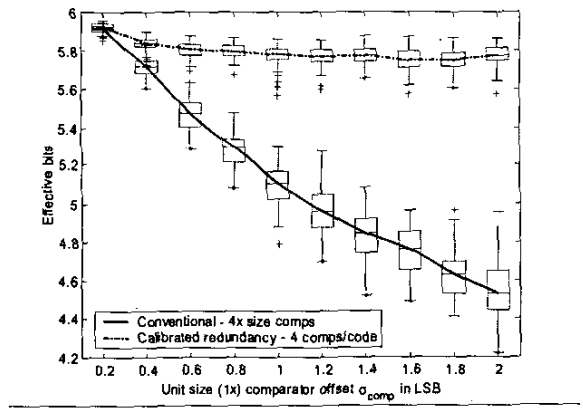

Fig. 7. The resolution in effective bits predicted by Monte-Carlo analysis for a standard 6 bit flash ADC and a 6 bit ADC with redundancy of the comparator area.

Once there is a certain amount of redundancy, the scheme is surprisingly resilient to comparator offset. This is illustrated by the Monte-Carlo simulation data presented in Fig. 7 and Fig 8. Fig. 7 shows the effective resolution of a 6 bit ADC versus comparator offset for a traditional ADC and one with redundancy. In this simulation both ADCs have the same comparator area. Even with very large offsets the effective resolution of the scheme with redundancy stays close to the ideal value. On the other hand, the mean effective resolution of a traditional ADC (i.e. without redundancy) drops steadily with increasing offset. Fig. 8 shows the variation of maximum DNL in the same simulation.

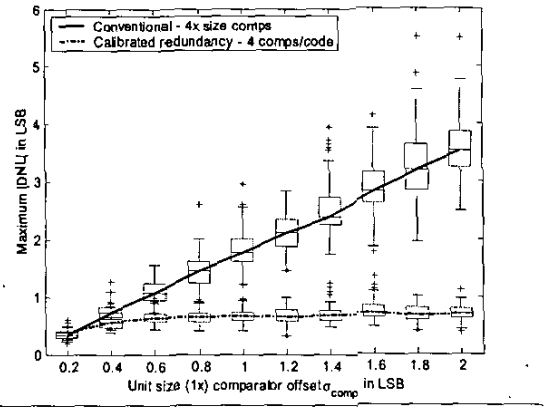

Fig. 8. The maximum DNL in LSBs predicted by Monte-Carlo analysis for a standard flash ADC and an ADC with redundancy.

With sufficient redundancy, good effective resolution is achieved, even in the case of very large comparator offsets. For a 6 bit ADC, a yield of 98.9% is achieved with σ_{comp} = 5LSB with a redundancy of 5 comparators per code, whereas a conventional ADC would need more than 120 times more comparator area to achieve the same yield. Fig. 9 and 10 show that very poor comparator accuracy can be tolerated when redundancy is used in 6 and 8 bit ADCs.

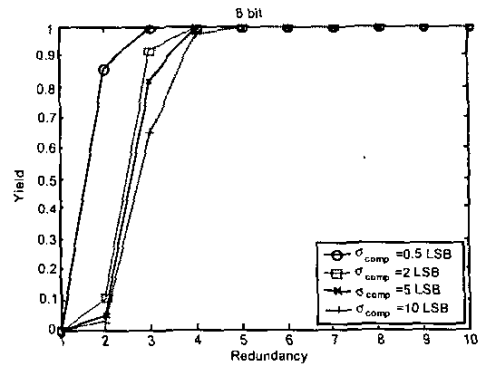

Fig. 9 Yield versus redundancy for a 6 bit ADC.

CONCLUSIONS

Calibrated redundancy is an attractive alternative to traditional flash ADC schemes, particularly in deep-submicron CMOS. Since analog accuracy is traded for digital complexity, this scheme allows us to take advantage of the increasing speed of CMOS transistors.

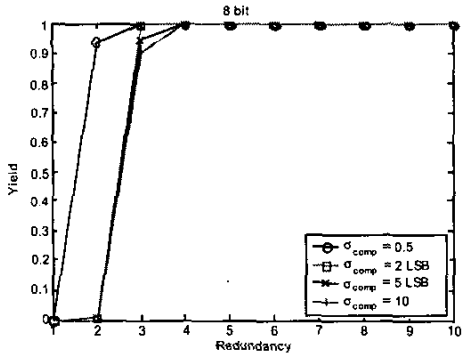

Fig. 10 Yield versus redundancy for an 8 bit ADC.

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