A Fully Integrated Dual-Mode Frequency Synthesizer for GSM and Wideband CDMA in 0.5µm CMOS

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Abstract
A fully integrated dual-mode frequency synthesizer for GSM and Wideband CDMA (WCDMA) is presented. The synthesizer is designed to maximize hardware sharing between the two modes by applying fractional frequency synthesis to GSM mode and integer frequency synthesis to WCDMA mode. The shared components include phase frequency detector (PFD), charge pump (CP), loop filter, integer frequency divider and VCO, which is 70% of the entire synthesizer in term of die area. A high-speed low power dual modulus prescaler is proposed to operate up to 2.1GHz at 3.3V supply voltage with 11.6mW power consumption by simulation. A dual mode VCO is also proposed for the enhanced tuning range with an accumulation mode NMOS varactor for band-to-band tuning and a p’n junction varactor for in-band tuning. The simulation result shows that the synthesizer phase noise is –112dBc/Hz at 600kHz offset frequency for WCDMA mode and –117dBc/Hz for GSM mode.

1. Introduction
GSM is the most popular cellular standard in the 2nd generation wireless communication. It has approximately 65% of the cellular subscribers in the world with primary service of voice transmission and internet access. In the 3rd generation wireless communication, GSM will evolve into WCDMA standard, which provides more frequency bandwidth for voice, data and video transmission. A dual-mode transceiver [1,2] that incorporates both standards with smooth migration and backward compatibility, therefore, becomes very necessary.

Frequency synthesizers are widely used in the wireless transceivers to provide precise and fine-tunable local oscillation frequencies. In the multi-standard frequency synthesizer design, hardware sharing is an important issue that mandates maximum component reuse between the two modes for small die area, low power consumption and low cost. In this paper, a dual-mode frequency synthesizer is proposed to maximize hardware sharing in GSM and WCDMA modes. The system architecture is discussed in Section 2, followed by the circuit description in Section 3. The simulation results are provided in Section 4 and the conclusion in Section 5.

2. System architecture
Some of the specifications for frequency synthesizer design in GSM and WCDMA are listed in Table 1. The two standards are very different in the frequency range and channel spacing. The goal of the design is to maximize hardware sharing between the two modes. The block diagram of the dual-mode synthesizer is shown in Figure 1. Since the frequency range of WCDMA is close to twice of that of GSM, a single VCO may be sufficient if a divide-by-2 frequency divider is used for GSM. Choosing the intermediate frequency (IF) as 145MHz, we can determine the VCO output frequency range as 1785-1845MHz for WCDMA and 1580-1630MHz for GSM. If process and temperature variation is considered, the VCO tuning range must be designed much larger with enough safety margin. A dual-mode LC VCO, which will be described in more detail in Section 3, is proposed for the enhanced tuning range with an accumulation mode NMOS varactor for band-to-band tuning and a p’n junction varactor for in-band tuning.

Table 1. Selected specifications of GSM and WCDMA.

<table>
<thead>
<tr>
<th></th>
<th>Frequency range (MHz)</th>
<th>Channel spacing</th>
<th>Number of channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>890-915 (Tx)</td>
<td>200kHz</td>
<td>124</td>
</tr>
<tr>
<td></td>
<td>935-960 (Rx)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WCDMA</td>
<td>1850-1910 (Tx)</td>
<td>5MHz</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>1930-1990 (Rx)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The channel spacing of WCDMA is 5MHz, 25 times that of GSM, 200kHz. This would result in very different frequency divide ratio and loop bandwidth if an integer frequency divider was used for both modes. If their frequency dividing ratios were more than one order of magnitude apart, the charge pump current would be different for loop gain compensation. The loop filter would need to be designed individually also due to different loop bandwidth and charge pump current, which means large die area to implement loop capacitors, especially for GSM loop filter.

To maximize hardware sharing, a fractional frequency divider is employed in GSM mode as shown in Figure 1. The reference frequency is 3.2MHz instead of 200KHz, leading to frequency divide ratios ranging from $246^{14/16}$ to $254^{11/16}$ with a step of $1/16$. A one-bit 2nd order \( \Delta \Sigma \) modulator is used for phase compensation. For WCDMA, an integer frequency divider is used, whose divide ratios are 357 ~ 369 and step is 1. The reference frequency is 5MHz. Since the reference frequency and divide ratio is chosen close for the two modes, similar loop gain and loop bandwidth can be obtained, and the charge pump and loop filter become shared components. To use a single external crystal oscillator as the frequency reference, two frequency dividers with divide ratios of 16 and 25 are used for WCDMA and GSM, respectively. The crystal oscillator frequency is 80MHz.
A summary of system configuration is given in Table 2. The shared components include phase frequency detector, charge pump, loop filter, integer frequency divider and VCO.

Table 2. Summary of the dual-mode synthesizer configuration

<table>
<thead>
<tr>
<th>Shared components</th>
<th>Non-shared components</th>
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<tr>
<td>VCO (MHz)</td>
<td>Integer divider</td>
</tr>
<tr>
<td>GSM 1580-1630</td>
<td>Divided by 246-254</td>
</tr>
<tr>
<td>W-CDMA 1785-1845</td>
<td>Divided by 357-369</td>
</tr>
<tr>
<td></td>
<td>PFD, CP, loop filter</td>
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<td>2(^{nd}) ΔΣ modulator, Reference frequency dividers</td>
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3. Circuit Description

In this section, some of the loop components including the dual modulus prescaler and VCO are described.

**Divide-by-15/16 Dual modulus prescaler (DMP)**

As one of the two components that operate at the full output frequency in the synthesizer, the DMP presents an important challenge to the design of multi-gigahertz synthesizers in the standard CMOS process. A conventional divide-by-16/17 DMP consists of a synchronous divide-by-4/5 stage and an asynchronous divide-by-4 stage. Because all three DFF’s in the 1st stage operate at the full-speed of the VCO output, they consume a great portion of the overall power and present as large clock load on the VCO or VCO buffer. In addition, the speed of the DMP is severely limited by the delay introduced by the NAND gates in the critical path [3].

A new high-speed low-power DMP topology is proposed. In this DMP, the synchronous part is designed as a divide-by-3/4 divider using the state-selection scheme. Compared with the conventional divide-by-4/5 prescaler, it has a higher speed by eliminating the NAND-gate introduced critical path delay, as well as a lower power consumption by minimizing the number of full-speed D-type flip-flops (DFF’s) in the 1st stage.

Figure 1. Block diagram of the dual-mode frequency synthesizer.

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Figure 2. (a) State diagram of the divide-by-3/4 DMP (solid line: /4 state transition, dash line: /3 state transition), (b) block diagram with the state-selection scheme, (c) Timing diagram of the state-selection in the /15 operation.

Figure 2(a) shows the state diagram of the divide-by-3/4 stage. A circuit implementation of the divide-by-15/16 DMP is shown in Figure 2(b). A standard 2-input multiplexer (MUX2) with two CMOS transmission gates serves as the state selector. When the state-selection signal S is asserted, it forwards logic 0 to D2. As a result, the DMP returns back to state 1 without going through state 4, leading to a /3 operation as shown by the dash line in Figure 2(a). The on-resistance of the transmission gates can be made very small by proper sizing, so the extra delay introduced in the critical signal path is much smaller than that of the NAND gates in the conventional DMP. In addition, because one less full-speed DFF is used, the proposed DMP is also superior to the conventional DMP in power consumption.

The timing diagram of the state-selection in the /15 operation is illustrated in Figure 2(c). Denote Q1* and Q2* as the outputs of the two DFF’s in the 2\(^{nd}\) stage /4 divider. Assume the /15/16 control signal is set high to enable /15
When both $Q_1^*$ and $Q_2^*$ are high, i.e., once every period of the output signal $F_{div}$, the state-selection signal $S$ becomes high (shown as transition ‘a’ in Figure 2(c)). This leads to logic 0 being selected by the MUX2 as the input of DFF2. Upon the arrival of the next rising edge of the input clock signal $F_{in}$, DFF2 will become 0 (shown as transition ‘b’ in Figure 2(c)). The 1st stage returns to state 1 from state 3 without going through state 4, so one input signal period is skipped, resulting in a /3 operation for the 1st stage. The output of DFF1 ($Q_1$) is also necessary in the state-selection logic, because the MUX2 must restore its normal condition to select $Q_1$ as the input of DFF2 as soon as both DFF1 and DFF2 reach 0 (shown as transition ‘c’ in Figure 2(c)). Thus normal /4 operations can be performed afterwards until the condition $Q_1^* Q_2^*=11$ is satisfied again.

**Dual band LC VCO**

![Figure 3. Simplified resonant LC-tank.](image)

![Figure 4. Simplified VCO circuit schematic.](image)

A dual band, LC tuned VCO is designed using integrated varactors and spiral inductors. Dual-band operation is accomplished by tuning the VCO with two control lines, one for continuous tuning and the other for digital band selection as shown in Figure 3 where C_SW is for digital tuning and C_FINE for continuous tuning. The continuous tuning is used for PLL control and channel selection. The digital tuning is used for RF band selection.

The active circuit of VCO consists of a cross-coupled NMOS transistor pair to form a negative resistance. The VCO core circuit topology is similar to the ones presented in [4,5] as shown in Figure 4. The negative resistance compensates the loss in the resonator LC-tank. The small-signal resistance seen at the drain of M1-M2 transistor pair is equal to $-2g_{m}$, where $g_{m}$ is the transconductance of each transistor. In order to start and sustain oscillation, the magnitude of the negative equivalent small-signal resistance, $-2g_{m}$ must be at least 20% greater than the resonator tank equivalent resistance [6].

The continuous tuning scheme uses p’n diode for analog tuning with control voltage, $V_{FINE}$, provided by the loop filter. Previously, the digital tuning scheme has been reported in reference [4]. The MOS transistors are used to switch in and out fixed amounts of capacitance or inductance from total LC tank that suffers from loss due to ON and OFF resistance of the MOS transistor seen by the tank.

In this work, the digital tuning is done using NMOS transistor as a varactor that operates in the accumulation and depletion region, while the mode selection voltage, $V_{SW}$, takes values of either GND or VDD [7]. In both operation modes, the NMOS transistor capacitance has high quality (Q) factor [7] that presents much lower loss than reference [4].

### 4. Simulation results

**Dual modulus prescaler**

![Figure 5. Simulated waveforms /15 and /16 operations. ($F_{in}$=2.15GHz, $V_{dd}$=3.3V).](image)

![Figure 6. Simulated maximum operating frequency and power consumption of the divide-by-15/16 DMP as a function of power supply voltage.](image)

The divide-by-15/16 DMP has been simulated with Cadence Spectre and AMI-C5N 0.5µm CMOS parameters. Figure 5 shows the input waveform at 2.15GHz and the output waveforms for /15 and /16 respectively with a 3.3V supply. In Figure 6, the maximum operating frequency and the corresponding power consumption is given at different

Supply voltage (V)
supply voltages. For 3.3V supply, the maximum operating frequency is 2.15GHz, while the power consumption is 11.6mW.

**Dual band LC VCO**

The simulated phase noise is –112dBc/Hz at a frequency offset of 600kHz. The tuning range and VCO gain is also simulated for both bands and is shown in Fig. 7. The VCO performance is summarized in the Table 3.

![Figure 7. VCO tuning range for the two RF bands.](image)

![Table 3. Summary of VCO Performance](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Oscillator core current</td>
<td>5mA</td>
</tr>
<tr>
<td>Tuning range</td>
<td>1500-1850MHz (22%)</td>
</tr>
<tr>
<td>VCO gain</td>
<td>80 MHz/V</td>
</tr>
<tr>
<td>Phase noise at 600KHz</td>
<td>–112dBc/Hz</td>
</tr>
<tr>
<td>Process</td>
<td>0.5µm CMOS (AMI C5N)</td>
</tr>
</tbody>
</table>

**Loop settling and phase noise**

A mixed-mode closed-loop simulation is performed for loop parameter adjustment before finalize the design for layout. A typical transient response of the VCO control voltage in the closed-loop simulation is shown in Figure 8. The synthesizer phase noise is –112dBc/Hz at 600kHz for WCDMA mode and –117dBc/Hz for GSM mode. The chip layout is shown in Figure 9. Implemented with 0.5µm CMOS process, the chip has an area of 1.6 mm².

**5. Conclusions**

A fully integrated dual-mode frequency synthesizer for GSM and WCDMA in 0.5µm CMOS is presented. The hardware sharing issues are discussed in the system architecture design that makes the PFD, charge pump, loop filter, integer frequency divider and VCO all shared between the two modes. This is accomplished by applying fractional frequency synthesis to the GSM mode and integer frequency synthesis to the WCDMA mode.

A high speed low power dual modulus prescaler is proposed using a state-selection scheme. It has a higher speed by eliminating the NAND-gate introduced critical path delay, as well as a lower power consumption by minimizing the number of full-speed D-type flip-flops (DFF’s) required. A dual band LC VCO is also proposed that increases the frequency tuning range with an accumulation mode NMOS varactor for band-to-band tuning and a p’n junction varactor for in-band tuning. The simulation result shows that the synthesizer phase noise is –112dBc/Hz at 600kHz offset frequency for WCDMA mode and –117dBc/Hz for GSM mode.

![Figure 8. Transient simulation of the VCO control voltage.](image)

![Figure 9. Frequency synthesizer layout.](image)

**References:**