Non-volatile Multi-Context FPGAs
Using Hybrid Multiple-Valued/Binary Context Switching Signals

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Abstract - Multi-context (MC) FPGAs have multiple memory bits per configuration bit forming configuration planes for fast switching between contexts. Large amount of memory causes significant overhead in area and power consumption. This paper presents two key technologies. The first is a floating-gate-MOS functional pass gate that merges storage and switching functions area-efficiently. The second is the use of a hybrid multiple-valued/binary context switching signal that eliminates redundancy of a conventional MC-switch with high scalability. The transistor count of the proposed MC-switch is reduced to 7% in comparison with that of a SRAM-based one. Although the FGFP-based MC-switch is compact, it has a large data path delay. Using a ferroelectric-based functional pass-gate, the delay of the proposed MC-switch is same as that of the SRAM-Based one while reducing the transistor count to 86%.

Keywords: FPGA, Floating MOS transistor, Ferro-electric capacitor

1 Introduction

Dynamically-programmable gate arrays (DPGAs) provide more cost-effective implementations than conventional FPGAs. One typical DPGA architecture is a multi-context one which has multiple memory bits per configuration bit forming configuration planes for fast switching between contexts. The additional memory planes cause significant overhead in area and power consumption.

An MC-FPGA has a cellular array structure where each cell consists of a programmable Logic Block (LB) and a programmable Switch Block (SB); Both of them consist of multi-context switches (MC-switches). Figure 1 shows the structure of a conventional SRAM-based MC-switch for 4 contexts. Each MC-switch selects a configuration bit between pre-stored configuration bits according to the context switching signal (CS). A conventional SRAM-based MC-switch requires N SRAM bits for N contexts. In order to reduce the overhead of configuration memory in MC-FPGAs, we employ two types of functional pass-gates that merges storage and switching function. Two types of functional pass-gate are employed: an floating-gate MOS functional pass-gate (FGFP) and a ferroelectric-based functional pass-gate (FEFP).

2 Hybrid multiple-valued/binary context switching signals

Figure 2 shows the conventional MC-switch using only multiple-valued CS for 4 contexts. A window literal is implemented by AND-ing an up-literal and a down-literal. The up-literal and down-literal are respectively, a monotonely-increasing function with a threshold and a monotonely-decreasing function with a threshold. In the conventional MC-switch, both pass turn ON redundantly for some configuration patterns. To eliminate this redundancy, a hybrid multiple-valued/binary context switching signal is used for context switching. The proposed MC-switch has only 2 FGMOSs, each of which is exclusively ON. Although the proposed MC-switch requires more complex circuit for generating the context switching signal, they can shared among several MC-switches, and its overhead is negligible.

3 Field-programmable VLSI using FGFPs

An single FGFP provides a threshold operation, and an MC-switch is implemented only by two FGFPs as shown in Fig. 3. By using the proposed MC-switches, the number of transistors of a switch block (10x10 MC-switches) is reduced to 7% compared to that using the SRAM-based MC-switches. Figure 4 shows the micro photograph of the prototype chip implemented in a 0.35 0.35μm CMOS process.

Fig. 1 : SRAM-based MC-switch.

Fig. 2 : Conventional FPFP-based MC-switch only using multiple-valued signal.
4 Field-programmable VLSI using FEFPs

An FGFP-based MC-switch has two disadvantages. The first one is that the use of FGMOSs requires a special process technology not suitable for a standard CMOS process technology. The second is that the use of the multiple-valued signal imposes the large delay of the data path. To overcome this problem, we use FEFPs since a ferro-electric capacitor is suitable to be integrated on the same chip together with CMOS circuits. Figure 5 shows the schematic diagram of the FEFP. The data retrieved from the ferro-electric capacitors are fed back to the gate of the pass-transistor via the buffer for binarization. Then, 0 or 1 are provided to the gate of the pass-transistor, and the pass-transistor is turned ON or OFF completely. Therefore, the delay and the power consumption of the data path are reduced. The number of transistors of the 10x10 MC-SB using the FEFPs is reduced to about 80% compared to that using SRAM-based MC-switches. Moreover, the static power consumption due to leakage current is reduced to 38%.

5 Conclusion

The non-volatile logic like FGFP and FEFP is useful for mobile applications such as digital cameras, cell phones and PDAs. This is because the power consumption due to reprogramming increases when the power should be tuned ON/OFF frequently.