

A High Precision Temperature Insensitive Current and Voltage Reference Generator

Kimberly Jane S. Uy, Patricia Angela Reyes-Abu and Wen Yaw Chung

Abstract—A high precision temperature insensitive current and voltage reference generator is presented. It is specifically developed for temperature compensated oscillator. The circuit, designed using MXIC 0.5 μ m CMOS technology, has an operating voltage that ranges from 2.6V to 5V and generates a voltage of 1.21V and a current of 6.38 μ A. It exhibits a variation of ± 0.3 nA for the current reference and a stable output for voltage reference as the temperature is varied from 0°C to 70°C. The power supply rejection ratio obtained without any filtering capacitor at 100Hz and 10MHz is -30dB and -12dB respectively.

Index Terms—Current reference, voltage reference, threshold voltage, temperature compensation, mobility.

I. INTRODUCTION

A voltage reference is an essential part of electronic systems and is widely used for both analog and digital circuits. An ideal voltage reference is one that is independent to both voltage supply and temperature variations. Numerous approaches to achieve a low voltage supply drift as well as low temperature drift voltage reference exist in literature. Voltage references normally are realized through the use of bandgap reference. Other principles used for implementation of voltage reference are threshold-voltage difference, flat-band voltage difference, work function difference and weighted gate-source voltage difference [1, 3, 4].

For most applications, the need for a precise current and voltage reference is essential. In order to achieve a high performance circuit, its current and voltage reference should be independent of both the change in voltage supply and temperature and thus are important factors to determine the performance of the current and voltage reference to be used.

In this paper, a current and voltage reference is designed that is specifically suitable to be used in on chip oscillators. Ideal on chip oscillators provide a precise clock frequency that is invariant to environmental conditions such as temperature. In order to achieve this, the current and voltage reference to be used in such application should be temperature insensitive.

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The development of a high precision temperature insensitive circuit and voltage reference circuit is illustrated in this paper. The circuit is designed using MXIC 0.5 μ m CMOS technology.

Section II discusses important parameters to consider in the design of temperature insensitive current and voltage reference. Section III tackles the circuit design in detail and its experimental results are illustrated in Section IV.

II. TEMPERATURE EFFECT IN CMOS DEVICE

One major limitation in CMOS device is its apparent changes with respect to the temperature change. It is therefore important to understand the effect of temperature to some of the variables of the CMOS device. The drain current equation shown in Eq. (1) is the equation used for the designing of a CMOS device application.

$$I_D = ((\mu_n C_{ox})/2)(W/L)(V_{GS} - V_T)^2 \quad (1)$$

The primary parameters that are affected by temperature in the drain current equation are the carrier mobility μ_n and threshold voltage V_T . In addition to these two parameters, the effect of temperature to resistance is another important parameter that needs to be considered in the design of a temperature insensitive circuit.

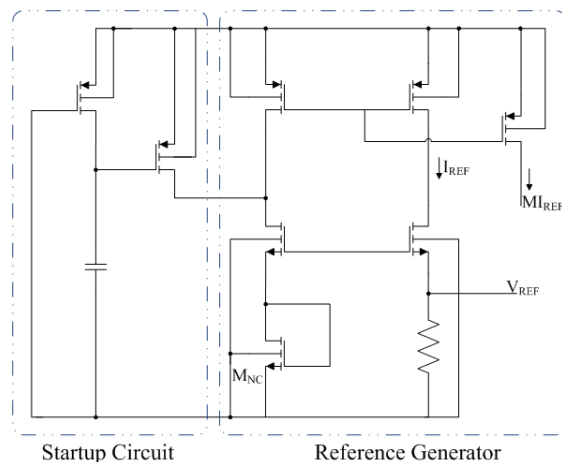


Fig. 1. Proposed current and voltage reference circuit.

A. Carrier Mobility

The carrier mobility μ_n is expressed as

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_n} \quad (2)$$

α_μ is the temperature coefficient for mobility whose typical value is -1.5. The effect of temperature to carrier mobility is illustrated in Fig. 2 for both N and P channel MOSFET. The graph in Fig. 2 illustrates that as the temperature increases, the mobility μ_n (or μ_p) decreases. Referring to the drain current in Eq. (1), μ_n (or μ_p) is directly proportional to I_D therefore also decreases I_D .

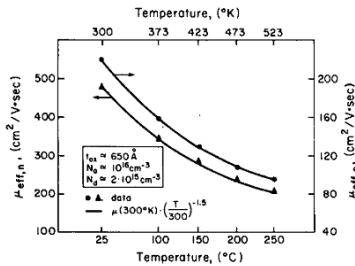


Fig. 2. Effective channel mobility versus temperature characteristics for n and p channel MOSFET. [2]

B. Threshold Voltage

The dependence of the threshold voltage V_T to temperature variations is expressed as

$$V_T(T) = V_T(T_0) - \alpha_{VT}(T-T_0) \quad (3)$$

The threshold voltage temperature coefficient (α_{VT}) for a CMOS device typically range from -1mV/°C to -4mV/°C. And, it is computed to be at -1.22mV/°C and -1.783mV/°C for NMOS and PMOS respectively for MXIC 0.5 μ m technology. The dependence of V_T to the change in temperature is shown in Fig. 3. From the graph, V_{Tn} (or V_{Tp}) decreases as the temperature is increased which clearly illustrates the effect of temperature to the threshold voltage V_T .

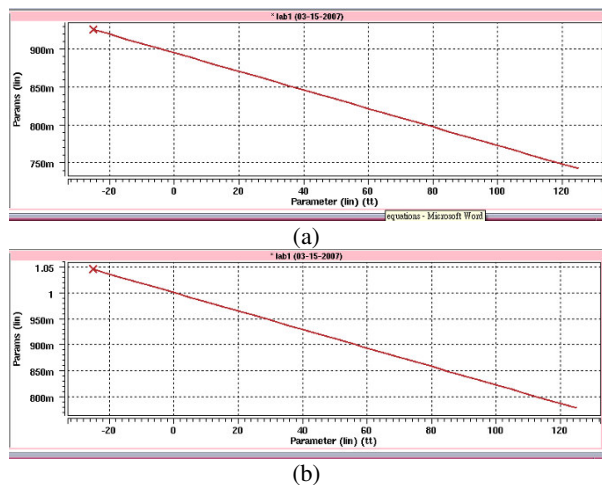


Fig. 3. Threshold voltage versus temperature characteristic curve of MXIC 0.5um technology for: (a) NMOS and (b)PMOS

C. Resistance

Another important parameter to consider in analog circuit design is resistivity that is also dependent on temperature variation as shown in the expression

$$R(T) = R(T_0)[1+10^{-6}TC_1(T-T_0)] \quad (4)$$

where

- $R(T)$ = resistance at the desired temperature
- $R(T_0)$ = resistance at some other temperature
- TC_1 = linear temperature coefficient of resistivity (ppm/°C)

Resistors ideally have a linear relationship between voltage and current. Resistors dissipate power which causes internal heating and thus increases the temperature. Resistors typically have a large temperature coefficient. Table 1 lists the typical temperature coefficients of resistivity for HSR implant, polysilicon and N-well. The variation in the resistance value with regard to temperature is dependent on the temperature coefficient of the material being used. Table 1 shows a list of the commonly used material to produce an on chip resistor.

Material	ppm/°C
2k Ω /□ HSR implant (P-type)	+3000
500 Ω /□ Polysilicon (4kÅ N-type)	-1000
25 Ω /□ Polysilicon (4kÅ N-type)	+1000
10k Ω / N-well□	+6000

Table 1. Typical linear temperature coefficients of resistivity ($T = 25^\circ\text{C}$).

III. DESIGN CONCEPT AND CIRCUIT TECHNIQUES

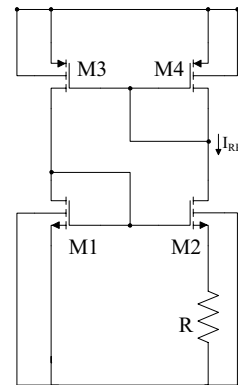


Fig. 4. PTAT current reference.

The circuit used in this work is shown in figure 1. It is made of two sub circuits, the startup circuit and reference generator. The startup circuit is provided to ensure that the current reference generated from the circuit will be moved from the undesired bias point where all current are equal to zero and work on the right equilibrium point. [3][5] The reference generator circuit is a hybrid of a proportional to absolute temperature (PTAT) current reference circuit as shown in figure 4. The PTAT circuit operates by causing the two branch of the circuit to have equal current flowing through

them. This is done through the use of mirrored PMOS transistor. The current generated with this circuit is given by Eq. (5).

$$I_{ref} = (U_T/R)\ln(S_2S_4/S_1S_3) \quad (5)$$

where I_{ref} is the current generated from the circuit U_T is the thermal voltage and S is the transistor aspect ratio. The thermal voltage value is dependent to the temperature. This tells us that as the temperature change, the current will change as well according to the value of the thermal voltage.[3] An increase in the thermal voltage will cause an increase in the threshold voltage of the CMOS device. The additional active load transistor (M_{NC}) placed in the proposed circuit will compensate for the thermal voltage change. This will ensure that the threshold voltage change in the circuit will be compensated as the temperature changes since the threshold voltage of the active load also changes as the temperature change.

IV. EXPERIMENTAL RESULTS

The proposed temperature insensitive current and voltage reference generator shown in Fig. 1 generates a current and voltage of $6.38\mu A$ and $1.21V$ respectively at room temperature ($25^\circ C$). Figure 5 shows the output current while figure 9 the output voltage of the circuit at varying temperature. For the temperature range of commercial IC varying from $0^\circ C$ to $70^\circ C$, a variation of $\pm 0.3nA$ for the

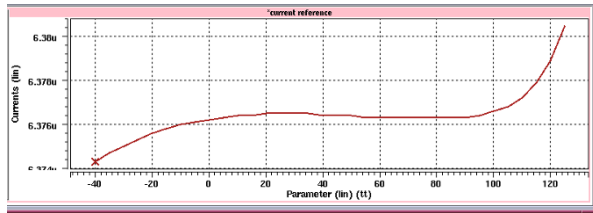


Fig. 5. Output current at varying temperature.

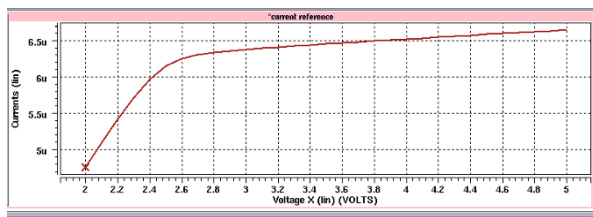


Fig. 6. Output current under varying supply voltage.

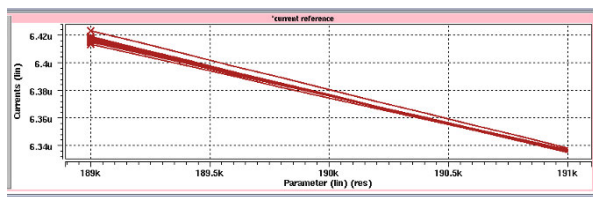


Fig. 7. Output Current at Varying Resistor Value With Respect to Temperature

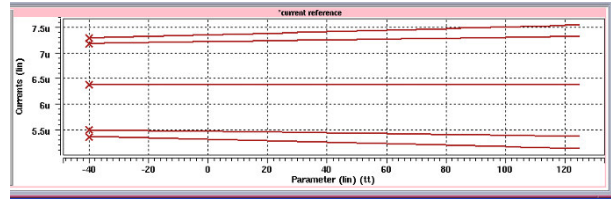


Fig. 8. Current reference under the five corner condition.

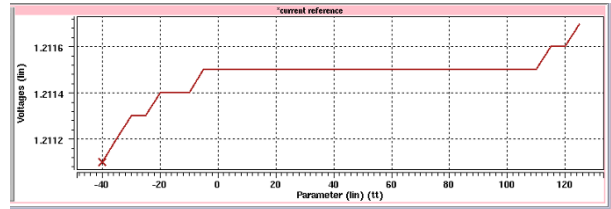


Fig. 9. Output voltage at varying temperature.

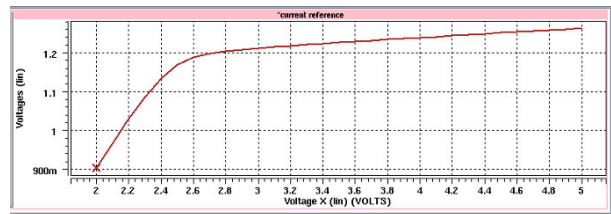


Fig. 10. Output voltage under varying supply voltage.

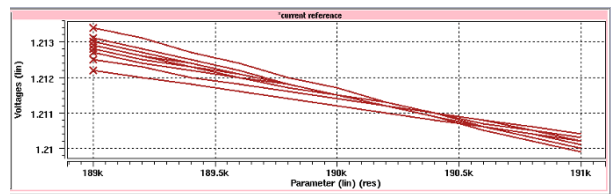


Fig. 11. Output Voltage at Varying Resistor Value With Respect to Temperature

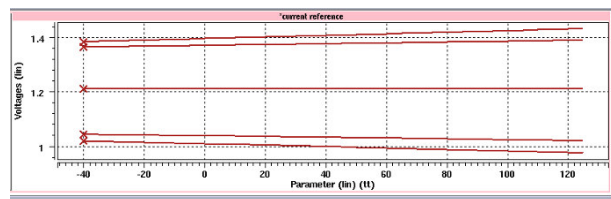


Fig. 12. Current reference under the five corner condition.

current reference was observed and a stable voltage reference was achieved. Further observation of the circuit with an increase in the temperature range from $-40^\circ C$ to $125^\circ C$, which is for military application, a variation of $\pm 4nA$ and $\pm 0.6mV$ was obtained for the current reference and voltage reference respectively. It operates at a supply voltage range of $2.6V$ to $5.0V$ and reveals a variation of $\pm 0.27\mu A$ and $\pm 0.052V$ for the current and voltage respectively. Figure 6 shows the variation in current and figure 10 shows the variation in voltage as the supply voltage of the circuit is changed. The measured PSRR is $-30dB$ at $100Hz$ and $-12dB$ at $10MHz$. The circuit was also observed to have a power consumption of $55.58\mu W$. Figure 7 and 11 shows the behavior of the current and voltage

reference of the circuit respectively at varying resistor value and temperature. While figure 8 and 12 shows the behavior of the current and voltage reference respectively for the five corners simulation.

V. CONCLUSION

Since carrier mobility, threshold voltage and resistance value are temperature dependent parameters, consideration of these parameters are important in the design of MOS circuit in order to optimize the performance of the circuit over a wide range of temperature. A high precision temperature insensitive current and voltage reference circuit has been presented in this paper which took into account the three said parameters. The circuit was designed using MXIC 0.5um CMOS technology and experimental results were illustrated. It shows that the proposed circuit can provide a low variation of $\pm 0.3\text{nA}$ for the current and a stable voltage as the temperature is varied from 0°C to 70°C . The current and voltage reference variation for temperature range for military applications (-40°C to 125°C) was also calculated and shows to be still within acceptable range. The proposed current and

voltage reference circuit provides a very low temperature drift current and voltage reference. Such circuit is designed for use in applications that may be in need of a stable current and voltage reference such as LDO voltage regulators and oscillators.

REFERENCES

- [1] G. De Vita, and G. Iannaccone, "An Ultra Low Power, Temperature Compensated Voltage Reference Generator", *IEEE 2005 Custom Integrated Circuits Conference*, pp. 751-754, 2005.
- [2] F. S. Shoucair, "Design Considerations in High Temperature Analog CMOS Integrated Circuits", *IEEE Trans. On Components, Hybrids, and Manufacturing Technology*, , vol. CHMT-9, pp. 242-251, Sept. 1986.
- [3] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutri, "A Low Voltage Low Power Voltage Reference Based on Subthreshold MOSFETs", *IEEE J. Solid States Circuits*, vol. 38, pp.151-154, Jan 2003.
- [4] K. N. Leung, and P. K. T. Mok, "A CMOS Voltage Reference Based on Weighted ΔV_{GS} for CMOS Low-Dropout Linear Regulators", *IEEE J. Solid-State Circuits*, vol. 38, pp. 146-149, Jan. 2003.
- [5] P. E. Allen, and D. R. Holberg, "CMOS Analog Circuit Design, Second Edition", New York: Oxford University Press Inc., 2002.
- [6] A. Hastings, "The Art of Analog Layout", New Jersey: Prentice Hall, 2001.