A balanced rail-to-rail all digital comparator using only standard cells

Bo Wang, Kezhi Li, Zhongjian Chen, Xin’an Wang

An all-digital comparator with full input range is presented. It outperforms the nowaday all-digital comparators with its large rail-to-rail input range. This is achieved by the proposed “Yin-yang” balance mechanism between the two logic gates: NAND3 and OAI (Or-And-Invert). The important design considerations to achieve this balance are presented, such as the driving strength manipulation and the use of pre-distortion technique. Constructed only by commercially available digital standard cells, the layout of the proposed comparator is generated automatically by standard digital Place & Route routine within several minutes. The Verilog code for the proposed circuit is given, and the circuit is successfully implemented in 130nm CMOS technology with the power consumption of 0.176mW at the clock of 330MHz.

Introduction: The analog circuits are indispensable in SoC system. However, tedious fine tuning, painful layout, and the difficulty to scale down, all these become the bottleneck. On the other hand, if the analog circuit can be constructed by standard digital cells, then the layout will be automatically generated by digital tools, and a lot of time and effort can be saved, thus allowing for a much easier design scaling down. Recently, some advancements have been made for DAC, oscillators, ADPLL and TDC [1-3].

Also, an all-digital comparator was proposed by Weaver et al. in [4] using NAND3 gate, shown in Fig.1. It’s a simple discrete-time comparator similar to a latch composed of digital cells instead of discrete MOSFET. When the clock is low, the output goes high; when is high, the output will be discharged proportional to the input. Through positive feedback, the outputs will be forced to the supply rail.

What’s more, the comparator is compatible with digital synthesis and the layout can be generated automatically. Although the mismatch of the offset voltage is inevitable due to auto Place & Route, it is however acceptable in stochastic flash ADC [4] if only it’s under certain level.

Fig.1 Weaver’s comparator made from digital NAND3 gate [4]

However, Weaver’s comparator using NAND3 gates shows an obvious limitation: its input common-mode voltage must be high enough to ensure the cut-off of the PMOS (MP1,MP2) connected to the input, because the digital cells inputs must connect a NMOS and a PMOS, which is different from an ordinary analog circuit. This defect largely reduces the input range of the comparator. Philosophically we consider this limitation of input voltage at high level as a result of excessive “yang” (NAND3 gate) in the circuit and should be balanced by additional “yin” (OAI gate) to pull it down, such that the low input voltage can be applicable. In this letter, we propose an enhanced auto P&R comparator which enjoys rail-to-rail input range as well as better accuracy. It can be readily used in a stochastic flash ADC.

Architecture: We can see in Weaver’s comparator, when input voltage is low, the PMOS will charge the output, meanwhile if , the comparator won’t work. So we must ensure the at the initial state even the input voltage is low. To enhance the pull-down strength, we add two OAI31 gates (Or-And-Invert), which is a common digital standard cell available in most of foundries, shown in Fig.2.

\[
V_{BL} = V_{SS},\ V_{RH} = V_{SS} + (V_{DD} - V_{SS}) \cdot \frac{Q_{OAI}}{Q_{OAI} + Q_{OAI}}, \quad \text{if} \ Q_{OAI} > Q_{OAI} \\
V_{BL} = V_{SS},\ V_{RH} = V_{DD} \quad \text{if} \ Q_{OAI} = Q_{OAI}
\]

\[
V_{BL} = V_{DD} - (V_{DD} - V_{SS}) \cdot \frac{Q_{OAI}}{Q_{OAI} + Q_{OAI}}, \ V_{RH} = V_{DD} \quad \text{if} \ Q_{OAI} < Q_{OAI}
\]

The full schematic of the proposed comparator is shown in Fig.3. The outputs of the 4 gates are cross-coupled. When clock signal is low, the two outputs go high; when is high, the outputs start to charge and discharge. Since the OAI31 gates supply MN5, MN6, MN7, MN8 to discharge, no matter what the , we can ensure at the initial state, as long as the driving strength of OAI31 gates are strong enough. Consider , so , at the same time . For other MOSFETs, as the gate voltage is VDD, I_{OAI} = I_{MN7}, I_{MN8} = I_{MN8}. The discharge rate of the node OP is higher than the node. So V_{ON} < V_{OP}. Then the cross-coupled connection creates positive feedback, . As a result, V_{ON} is forced to low, V_{OP} is forced to high. This comparator makes it easy to compare the rail to rail input voltage, since whatever the input is, on each side there is at least one of the PMOS and NMOS working.

In fact, this is not the only benefit of OAI31 gates. The OAI31 gates can also enhance the positive feedback, leading to the speedup of comparison. What’s more, the additional OAI31 gate together with the original NAND3 gate, helps to balance the offset caused by auto P&R, hence enjoys better accuracy, shown in table 1, compared with the circuit using only NAND3 gate.

To design the comparator, it’s crucial to choose the gates with suitable driving strength, which is the key to the circuit balance and large input range. Clearly, if the driving strength of NAND3 gate is too strong, and the input voltage is low, we can’t ensure at the initial state; on the other hand, if the driving strength of OAI31 gate is too strong and the input voltage is high, the outputs would discharge too quickly causing the positive feedback unable to force the outputs to the supply rail. All these will decrease the input range of the comparator.

The equation (1) gives the relationship between the driving strength of OAI31 gate (Q_{OAI}), NAND3 gate (Q_{NAND}), and the upper and the lower limit of input voltage (V_{RH} V_{BL}), showing that the largest rail-to-rail input range occurs with the balanced Q_{OAI} and Q_{NAND}.

Fig.2 A standard digital OAI31 gate and its transistor schematic

Fig.3. The proposed comparator made from NAND3 and OAI31 gates
To further improve the balance we propose a "pre-distortion technique". We notice that if we design a balanced pre-layout circuit, then after layout it will inevitably introduce some wire mismatch and consequently impair the balance. This implies that to get a balanced post-layout circuit we should "pre-distort" the circuit before layout. Furthermore we find in our circuit that the non-ideal mismatch tends to enhance the strength of OAI31 gate. So before layout we would intentionally design a stronger NAND3 gate in order to finally get a balanced post-layout circuit.

The complete comparator structure is shown in Fig.4a with buffers and SR-latches added to the output to hold the voltage while the comparator is reset. The corresponding RTL Verilog code using the smic013 process is shown in Fig.4b.

Fig.4. a. Gate-level schematic of the comparator buffered to a SR-latch. b. RTL Verilog code using smic013 process.

Results: Using SMIC 130nm CMOS technology we design 8 comparators Q1-Q8 by auto P&R, and one comparator Q by hand. For Q1, the area is 25um*25um. With 1.2V VDD, the power dissipation is 0.197mw at 330MHz for the common mode input voltage of 600mv. The offset voltages of post-layout simulation are shown in Table 1. The results of Q1-Q8 show smaller offset than [4] which was about 45mV.

Table 1: The offset voltage of Q and Q1-Q8 at different input common mode voltages (0.05V, 0.35V, 0.65V, 0.95V and 1.05V)

<table>
<thead>
<tr>
<th>Comparator</th>
<th>Offset (mv)</th>
<th>0.05V</th>
<th>0.35V</th>
<th>0.65V</th>
<th>0.95V</th>
<th>1.05V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>-7</td>
<td>3</td>
<td>-10</td>
<td>26</td>
<td>14</td>
<td>18</td>
</tr>
<tr>
<td>Q2</td>
<td>-4</td>
<td>17</td>
<td>-8</td>
<td>29</td>
<td>19</td>
<td>17</td>
</tr>
<tr>
<td>Q3</td>
<td>-3</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>Q4</td>
<td>-3</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>Q5</td>
<td>-2</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>Q6</td>
<td>-2</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>Q7</td>
<td>-2</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>Q8</td>
<td>-2</td>
<td>12</td>
<td>-16</td>
<td>24</td>
<td>22</td>
<td>5</td>
</tr>
</tbody>
</table>

Fig.5 (a-c) shows the transient post-layout simulation results for successful voltage comparison at various common mode input voltages: 50mV, 0.6V, 1.15V. Note that the comparison speed slightly slows down if the input common mode voltage is too high.

Conclusion: A balanced all digital comparator with rail to rail common mode input range using only digital standard cells is proposed. Fully compatible with digital synthesis, the layout is generated by auto P&R. The proposed comparator can be readily used in a stochastic flash ADC.

References


Acknowledgments: This research is supported by R&D projects of Shenzhen government and NSFC (61471011).

Bo Wang, Kezhi Li, Zhongjian Chen, Xin’an Wang (The Key Lab of IMS, School of ECE, Peking University, Shenzhen Graduate School) E-mail: wangxa@pku.edu.cn