Design for Manufacturability - or the meaning of '*subtle*'

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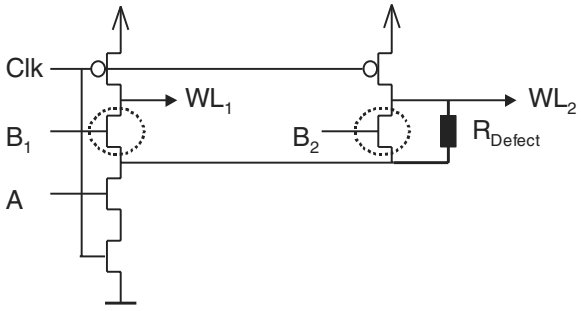
It used to be that *DfM* meant simple recipes such as spreading wires equally across all available space or to double vias where possible. Today, wire spreading is competing with strict density rules and tiling requirements, via doubling is competing with the added stress caused by the additional holes. Still, these *simple* cases of DfM need nothing more than detailed understanding of process mechanics and a seamless implementation in automated layout tools – the latter could arguably use some more attention!

Increasingly however, one observes *subtle* interactions between topological features stretching process capabilities and particular circuit diagrams leading to sensitivities to such defects. This is exemplified in the following example:



It depicts the shared row decoder for two word-lines of a memory. The circled transistors had a layout feature causing increased stress to the substrate, resulting in crystal dislocations. As a consequence, additional source-drain leakage (R_{Defect}) would cause WL_2 to be selected simultaneously with WL_1 that was addressed. This was only possible due to the netlist property of relying on pre-charged word-lines. R_{Defect} would not have affected static addressing. The mechanism caused approximately 1 in every 200'000 word lines to fail.

Let's assume a lead product in a new process contains 50 memories with 10'000 word lines total, covering 15mm^2. With a yield model $Y = e^{-A \cdot D_0}$, we may reach a random yield loss of 14% assuming $D_0 = 1cm^{-2}$ during process ramp. The systematic loss due to the mechanism described however will cost 5% yield – clearly a major concern!

Now, consider an early phase of process development: D0 will be much larger and – more importantly – highly instable. It is easy to draw scenarios where a test chip has 20% ± 10% random yield loss and the systematic problem is responsible for only 1%. It will thus be highly difficult to detect and analyze the shown issue at such an early process state.

Similar cases can easily be constructed where yield remains essentially untouched but quality is affected. Just assume for a second the – obviously unrealistic case – that a simplistic test algorithm would result in both addressed words always to carry equal data. The defect would be invisible in test and a *test validation procedure* needs be put in place to discover this inadequacy.

Since customers typically require «100ppm, validation procedures would need to look at 10^8 word lines or $>10^6$ memories of 1000 rows each. Such an experiment would provide ~10 devices for detailed physical failure analysis.

These are *big* experiments – especially because they need be made for all relevant building blocks of a large *SOC* device. Consequently, some of the learning will occur during early product ramp. Thus, *DfM* is about tightening the learning cycles, integrating all relevant know-how from process technology, design, test, failure analysis and providing feedback. Potentially, a mapping of the findings to design tools capabilities is needed to close the loop.

DfM is about using this feedback information at the highest possible rate to achieve improvements and thus lowest cost and best quality.

Learning opportunities exist within the same process node – process adaptations, implementation of improved test algorithms, but in severe cases even design fixes come to mind. Learning opportunities of course also exist towards the next node, where weak structures should be avoided up front.

The shorter the feedback loops, the less organizational hurdles there are to bring all disciplines together, the more subtle defects we can diagnose and learn from. If all the mechanisms were known, we'd be happily integrating the 15nm node today! The trend to fragmentation of the semiconductor value chain into independent entities is thus a major concern.

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