

CMOS-compatible, athermal silicon ring modulators clad with titanium dioxide

Stevan S. Djordjevic,^{1,*} Kuanping Shang,¹ Binbin Guan,¹ Stanley T. S. Cheung,¹ Ling Liao,² Juthika Basak,² Hai-Feng Liu,² and S. J. B. Yoo¹

¹Department of of Electrical and Computer Engineering, University of California, Davis, California 95616, USA

²Intel Corporation, 3600 Juliette Lane, Santa Clara, California 95054, USA

*sdjordjevic@ucdavis.edu

Abstract: We present the design, fabrication and characterization of athermal nano-photonics silicon ring modulators. The athermalization method employs compensation of the silicon core thermo-optic contribution with that from the amorphous titanium dioxide (a-TiO₂) overcladding with a negative thermo-optic coefficient. We developed a new CMOS-compatible fabrication process involving low temperature RF magnetron sputtering of high-density and low-loss a-TiO₂ that can withstand subsequent elevated-temperature CMOS processes. Silicon ring resonators with 275 nm wide rib waveguide clad with a-TiO₂ showed near complete athermalization and moderate optical losses. Small-signal testing of the micro-resonator modulators showed high extinction ratio and gigahertz bandwidth.

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1. Introduction

One of the most challenging obstacles in the path of silicon photonic integration on electronic processor chips is the issue of thermal stability. With increasing processor clock speeds, ever larger amounts of energy are dissipated on die. Joule losses on silicon-on-insulator (SOI) platform turn into heat. Due to the Buried Oxide (BO_x) layer, made of poor thermal conductor, generated heat propagates primarily over the surface of the die. This implies that silicon photonic devices must perform within the temperature range of CMOS components.

However, relatively large Thermo-Optic Coefficient (TOC) of silicon means that the temperature drift will induce significant change of the refractive index of silicon core. This changes the effective index and propagation constants of the waveguide and disrupts the designed phase relation in the silicon device. All interference-based silicon devices, including silicon rings, Mach-Zehnder Interferometers (MZIs), Arrayed Waveguide Gratings (AWGs) and other, are sensitive to temperature change.

Active control of the die temperature is relatively energy inefficient and may be difficult to implement, as the heating patterns over the die are unpredictable in general due to the varying ambient conditions. Passive athermalization of silicon waveguides has been demonstrated [1–3] using polymer cladding materials. Negative TOC of polymer cladding can offset the positive TOC of silicon core, when the ratio of confinement factors is correct. Low TOC polymers, such as Poly-Methyl-Meth-Acrylate (PMMA) require high cladding confinement, necessitating the use of slotted silicon waveguides. These are challenging to fabricate and may have higher losses than rib waveguides, due to high intensity of Transversal Electric (TE) field inside the slot. Advances in high TOC acrylate polymers allowed athermal operation at lower cladding confinement values, using deep etched rib waveguides [3, 4].

However, polymer materials are known to suffer from moisture absorption, chemical instability, photo-degradation and are mechanically weak [5–7]. This makes them incompatible with CMOS process and a poor candidate for integration.

A different, CMOS-compatible approach has been proposed in [8, 9], integrating the ring resonator with MZI, that compensates thermal drift of the ring. This solution, however, increases the total footprint of the device and may show significant wavelength dependence.

This paper presents the development of solid and chemically stable optical cladding material, titanium dioxide, which can be deposited on silicon as part of the CMOS fabrication process in the future [10]. Fabricated ring modulators exhibit near perfect athermal operation [11] and 2 GHz small-signal modulation bandwidth.

2. Design of athermal Si-TiO₂ waveguide

A silicon photonic waveguide on SOI platform consists typically of silicon core, BOx under-cladding and deposited overlcladding layer. We can express the waveguide effective index as:

$$n_{eff} = \Gamma_{core} n_{core} + \Gamma_{overclad} n_{overclad} + \Gamma_{underclad} n_{underclad} \quad (1)$$

Here, Γ_{core} , $\Gamma_{underclad}$ and $\Gamma_{overclad}$ are the percentage of power of an optical mode located within the core (silicon), the under-cladding (BOx) and the overlcladding (TiO₂), respectively. We will refer to these as core, under-cladding and overlcladding confinement factors. The effective TOC of the waveguide is given as the first derivative of the effective index of the waveguide with respect to temperature. Under the assumption that Γ_{core} , $\Gamma_{underclad}$ and $\Gamma_{overclad}$ change with temperature is negligible, we can write:

$$\frac{\partial n_{eff}}{\partial T} \approx \Gamma_{core} \frac{\partial n_{core}}{\partial T} + \Gamma_{overclad} \frac{\partial n_{overclad}}{\partial T} + \Gamma_{underclad} \frac{\partial n_{underclad}}{\partial T} \quad (2)$$

The TOC of the BOx layer (silicon dioxide, $\text{TOC}_{\text{SiO}_2} \approx 10^{-5} \text{ K}^{-1}$) is negligible compared to those of the silicon core ($\text{TOC}_{\text{Si}} = 1.81 \times 10^{-4} \text{ K}^{-1}$) and the TiO₂ overlcladding. Neglecting the contribution from the BOx under-cladding to the TOC of the waveguide effective index, we derive the simplified condition of athermal operation of silicon photonic waveguide:

$$\frac{\partial n_{eff}}{\partial T} \approx \Gamma_{core} \frac{\partial n_{core}}{\partial T} + \Gamma_{overclad} \frac{\partial n_{overclad}}{\partial T} \approx 0 \quad (3)$$

$$\frac{\Gamma_{overclad}}{\Gamma_{core}} \approx - \frac{\frac{\partial n_{core}}{\partial T}}{\frac{\partial n_{overclad}}{\partial T}} \quad (4)$$

This simple equation has three important implications. First, the upper cladding material must have negative TOC (or, in general, opposite sign of TOC of the core material). Second, the magnitude of the negative TOC should be as large as possible, as it will allow athermal operation at lower overlcladding confinement factor, leading to lower loss waveguide design. Third, it is advantageous to have higher refractive index cladding, as the desired overlcladding-to-core confinement factor ratio can be reached at larger core dimensions. The latter two conclusions stem from reasoning that waveguides with wider cores will exhibit lower propagation loss than narrower ones.

Athermalization requires balancing of the ratio of the over-cladding to core confinement factors against the ratio of the core to over-cladding TOC magnitude. To allow the high confinement of TE field in the overlcladding region, we considered deeply-etched silicon rib waveguides. Core height is 250 nm, etch depth is 200 nm and rib width is in 250 nm – 500 nm range. Figure 1 shows calculated overlcladding-to-core confinement factor ratio for different waveguide widths and various values of the overlcladding refractive index, expected for TiO₂.

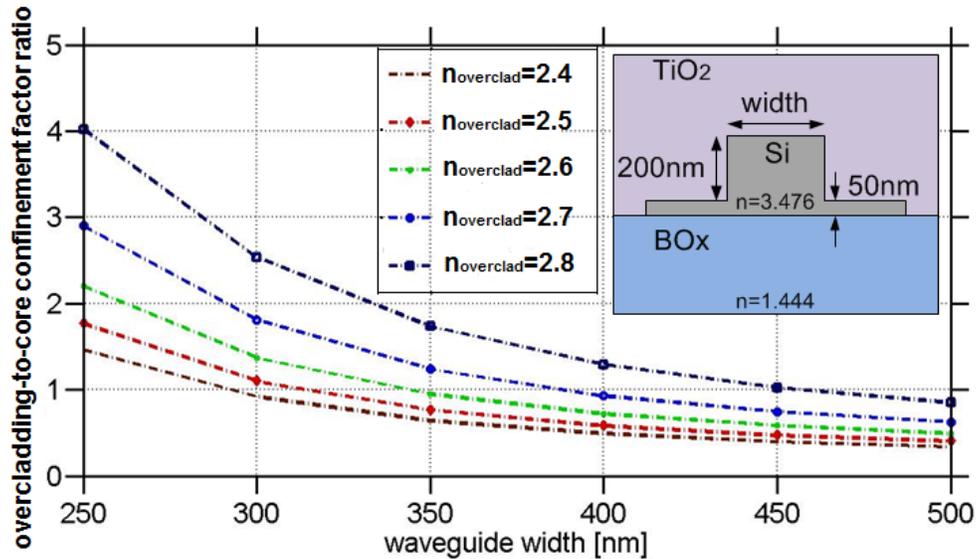


Fig. 1. Design of athermal Si-TiO₂ waveguide: overcladding-to-core confinement factor ratio versus waveguide width for different possible values of TiO₂ cladding refractive index. Considered are TE polarized optical modes. Inset shows waveguide cross-section, with marked critical dimensions

3. Development of negative TOC cladding

Negative TOC materials are far less common in nature than the ones with positive TOC. One of the few CMOS compatible materials that are known to exhibit negative TOC values is titanium dioxide (TiO₂). Unlike polymer materials, TiO₂ is mechanically hard, chemically stable material [12], with fabrication-related properties similar to more established hafnium-dioxide (HfO₂). TiO₂ has been successfully integrated in CMOS device design and fabrication process [13–15]. TiO₂ deposition and processing can result in amorphous or poly-crystalline structures depending on the temperature, pressure, and other conditions. In nature, TiO₂ comes in amorphous form or in one of at least three crystalline forms, namely anatase, rutile and brookite. Of the three, anatase and rutile were registered by X-ray Diffraction (XRD) analysis of deposited films. Among them, anatase is less stable and annealing above 600 °C forces phase transition into rutile. Thus, the deposition condition of TiO₂ and the thermal budget of TiO₂ after the deposition are very important considerations for integration on a CMOS platform, as it must be able to withstand the Back End Of the Line (BEOL) processes, without changing the desired film structure.

We determined the crystalline structure by XRD analysis, with acceleration voltage of 45 kV and emission peak Cu Kα1 line at 1.5 A. Emission slit sizes were 4 mm and 2 mm, detector slit sizes 0.4 mm and 0.2 mm, goniometric angles 5-90 degrees and step size 0.05 degrees. Detector count time was 0.5 seconds at each step. We deposited test samples on single crystal silicon substrate by RF magnetron sputtering. XRD traces in Fig. 2(a) show that the sample deposited with substrate temperature of 350 °C had amorphous structure. In all subsequent XRD traces, main peak at ~69 degrees is the reflection from single-crystal silicon substrate. After 6 hours of annealing in nitrogen atmosphere at 850 °C, sample showed two distinct and large XRD peaks, first at 62 degrees with ~9000 Counts Per Second (CPS) and second at 66 degrees, with ~6000 CPS. Both are associated with the rutile phase. This temperature induced phase transition is consistent with the findings of Martin *et al.* [16].

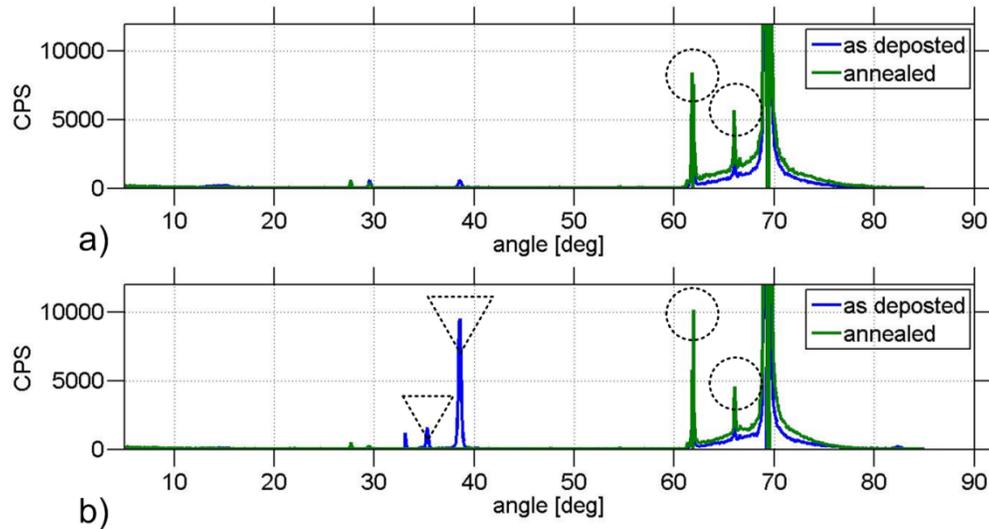


Fig. 2. Phase transitions in TiO₂: a) Annealing experiment at 850 °C using films deposited at 350 °C and b) Annealing experiment at 750 °C using films deposited at 400°C. XRD traces show anatase peaks with triangular markers and rutile peaks with circular markers. Blue lines represent XRD traces of 'as deposited' samples and green lines are XRD traces of annealed samples.

XRD traces in Fig. 2(b) show that the sample deposited at 400 °C had dominant anatase phase, with the main peak appearing at 38 degrees with ~10000 CPS. After annealing at 750 °C, the anatase phase could not be detected any more, as sample transitioned to rutile phase, similar to the one shown in Fig. 2(a). Polycrystalline films in optical cladding can lead to strong scattering of guided light due to formation of granular structures. Furthermore, thermally annealed samples showed cracking induced by shrinkage and accumulation of stress during the transition from the anatase to the rutile phase [16].

To obtain low loss optical cladding on silicon rib waveguide cores, it is necessary to deposit and to retain the amorphous structure of a TiO₂ film. Towards this goal, the deposition conditions using magnetron sputtering utilized active cooling of the substrate to 15 °C and maintaining of low sputtering power, since the sputtered particles reaching the substrate with high energy favor the creation of crystalline phases [16, 17]. This condition also helps creation of a high density TiO₂ film [18] which possesses high refractive index and large magnitude negative TOC value. As discussed before, this allows the athermal condition to be satisfied at wider core dimensions, which reduces the propagation loss.

The RF magnetron reactive sputtering used 99.995% pure 3-inch titanium target in a chamber with the base pressure of 8×10^{-7} Torr. The oxygen and argon gas with a fixed flow ratio were introduced by using the two gas mass flow controllers running in master-slave configuration, while maintaining the total process chamber pressure at 2×10^{-3} Torr. Rotation of the substrate at 5 rpm during the deposition improved film uniformity. We conducted optical reflectometry measurements at different sample temperatures to obtain the refractive index and TOC of 100 nm thick deposited films and Atomic Force Microscopy (AFM) to determine Root-Medium-Square (RMS) surface roughness.

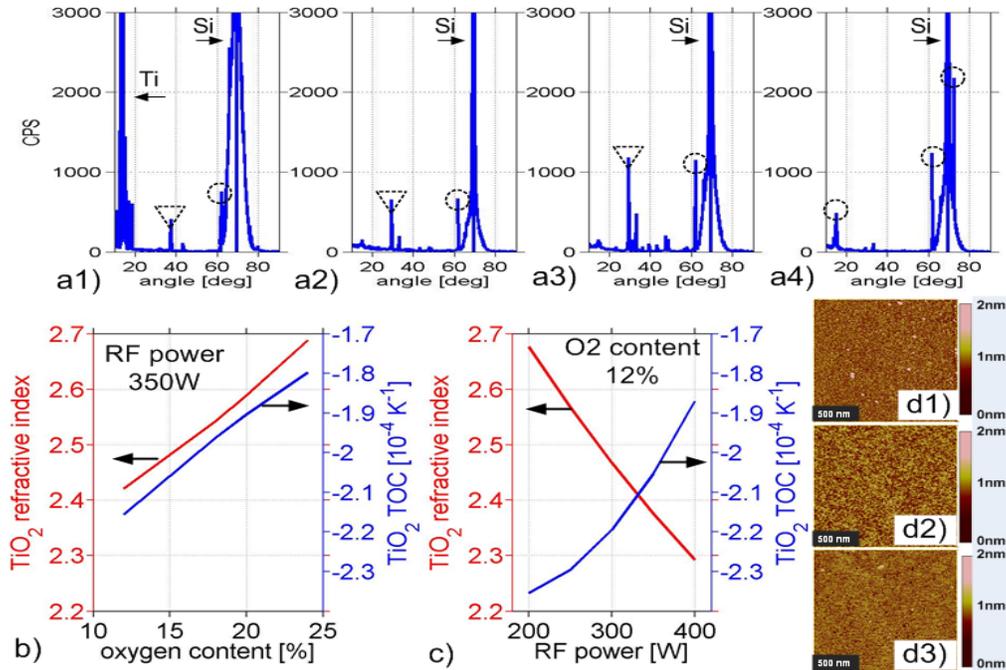


Fig. 3. Characterization of TiO₂ films a1-a4) XRD traces of films with 6%, 12%, 18% and 24% O₂ content; Marked are silicon substrate peaks and Ti peak in a1); triangles mark anatase and circles mark peaks attributed to rutile; b) refractive index (red line) and TOC (blue line) as function of O₂ content (at 350 W RF power); c) refractive index (red line) and TOC (blue line) as function of RF power (at 12% O₂ content); d1-d3) atomic force microscope images of films with 12%, 20% and 24% O₂ content. Respective RMS roughness values measured are 0.463 nm, 0.226 nm and 0.237 nm.

The principal optimization parameters for high quality and low loss TiO₂ film are reactive gas content and RF power. The oxygen content is critically important parameter in reactive sputtering and small variations can dramatically affect the film morphology [17, 19]. Also, since the target is run in fully poisoned mode, the oxygen content dictates the speed of superficial oxidation of the target, which is in delicate balance with the sputtering rate and sputtered particle energy. This is why the crystalline structure is also affected by the O₂ content [Fig. 3(a1) - 3(a4)]. Here, 6% O₂ content does not fully oxidize the deposited Ti film, 12% and 18% result in an amorphous structure with trace amounts of anatase phase, whereas 24% gives amorphous film with traces of rutile. TOC reduces with increased oxygen content [Fig. 3(b)] and with increased RF power [Fig. 3(c)]. We believe the latter is due to larger sputtered cluster size leading to less dense films. We support this hypothesis by observed increase in refractive index with reduced power, seen in Fig. 3(c).

Oxygen content of 12% yields amorphous films with very low surface roughness of 0.463 nm rms measured on the AFM. The refractive index of the a-TiO₂ film deposited at 360W RF power using 12% O₂ showed $n_{\text{TiO}_2} = 2.420$ and $\text{TOC} = -2.15 \times 10^{-4} \text{ K}^{-1}$. Based on these values, to satisfy athermal condition, the cladding-to-core confinement factor ratio ($\Gamma_{\text{TiO}_2}/\Gamma_{\text{Si}}$) of 0.837 is necessary. With reference to Fig. 1 we expect athermal operation for waveguides with 305 nm wide cores.

4. Device fabrication

Modulator device design uses ring configuration and forward biased transversal P-i-N junctions for phase tuning by free carrier injection. Mask layout includes devices with waveguide widths ranging from 250 nm to 450 nm, increasing with 25 nm step. Bending radii

on the die are selected to be much larger than the smallest possible radii producing acceptable optical losses in the resonator, in order to allow integration of potentially very high refractive index cladding materials. Bending radius for the narrowest (250 nm) waveguide is 340 μm , and is reduced by 25 μm with each 25 nm increase in waveguide width, while the predicted acceptable radii for $Q > 5000$ in the resonator for 250 nm waveguide width was 80 μm . A unique feature is the cladding trench, which opens the cladding around the waveguides only in the ring resonator region. The rest of the die retains SiO_2 cladding. The final step of fabrication process includes filling of the etched trench with $\alpha\text{-TiO}_2$. Cantilevered edge couplers measure ~ 3 dB/facet coupling loss to lens single-mode fiber.

We fabricated the devices using ASMLTM PAS 5500 300 deep-UV lithography stepper technology on 6-inch SOI wafers with 250 nm silicon device layer. Figure 4 shows the principle steps of the fabrication process. In the figure, left device illustrates the edge coupler structure, whereas the right device illustrates the phase shifting section of the ring modulator, as marked in the last plot in Fig. 4.

Fabrication starts with deposition of 32 nm thick Low Stress silicon Nitride (LSN) film by Low Pressure Chemical Vapor Deposition (LPCVD). This thin film will serve as oxidation barrier for the definition of inverse taper edge coupling structures. Waveguides are lithographically defined and etched using the hydrogen-bromide (HBr) transformer coupled plasma system [20]. Sidewall oxidation in dry oxygen atmosphere further reduces etched surface roughness. After stripping dry grown oxide, we pattern a 950 nm thick Low Temperature Oxide (LTO) oxidation mask and anneal it at 1050 $^\circ\text{C}$ for densification. The purpose of the mask is to protect devices from the following deep oxidation process, while exposing only the inverse taper structure tips. This step is shown in Fig. 4(i) and 4(h). The width of the inverse taper tips is reduced by oxidation of silicon from 250 nm after lithography, to 115 nm. We observed no reduction in height, due to the presence of LSN oxygen diffusion barrier on top. Phosphorus and boron ions are implanted at $5 \times 10^{15} \text{ cm}^{-2}$ doses to form current injection trenches. We annealed the wafers at 900 $^\circ\text{C}$ for 30 min for dopant activation. Upon cladding deposition and via etching, argon plasma sputter-etch removes the native oxide in contact area. Without breaking vacuum (to avoid native oxide formation), we deposited tantalum and silicon inter-layers for low contact resistance. Aluminum electrodes are sputtered, then patterned by lithography and etching. Annealing at 450 $^\circ\text{C}$ in forming gas (10% hydrogen 90% nitrogen mixture) alloys the contacts and fills the domain wall traps in the sputtered metal. Trenches are open in the ring resonator areas for local application of $\alpha\text{-TiO}_2$ cladding. We fabricate cantilevered edge coupler structures, similar to [21] by isotropic dry etching. Deep silicon etch allows lens fiber access to facet for coupling.

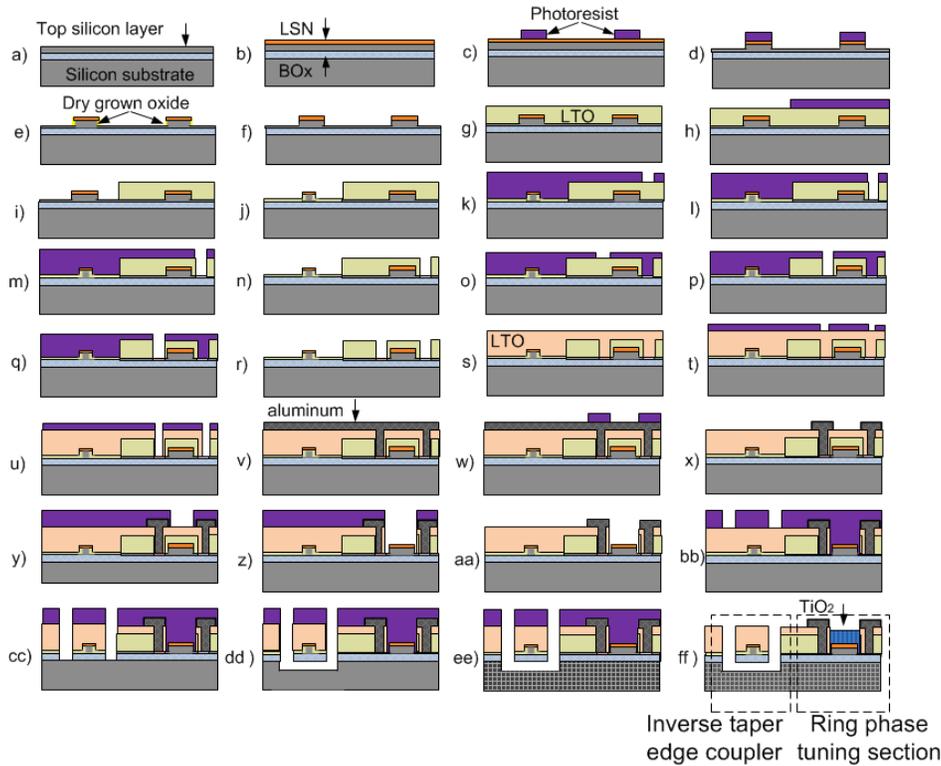


Fig. 4. Fabrication process flow. Left device represents coupling structure (at the facet) and right device represents modulator phase tuning section (middle of the die): a) starting SOI wafer b) LSN hard mask deposition c) waveguide layer lithography d) waveguide etching e) sidewall smoothing by dry oxidation f) oxide stripping g) LTO deposition for oxidation mask h) oxidation mask patterning lithography i) oxidation mask patterning etch j) selective deep oxidation process k) – r) P and N implant lithography, etch and implant steps, s) cladding deposition and dopant activation anneal t) via lithography, u) via etch, v) contact metal deposition, w) electrode patterning lithography, x) electrode patterning etch and forming gas anneal y) trench layer patterning lithography z) trench layer patterning etch aa) O₂ plasma ashing and oxide descum step bb) cantilever patterning litho cc) cladding and BOX etch dd) cantilever release etch ee) deep facet etching dd) TiO₂ deposition and final device structure. Marked are inverse taper coupler (edge of die) and ring phase tuning section (middle of die).

Figure 5(b) - 5(d) shows SEM images of the fabricated device, prior to filling the trench. The final step is the deposition of 900 nm thick a-TiO₂ cladding in the etched trenches, which coats the silicon waveguides that build the ring resonator.

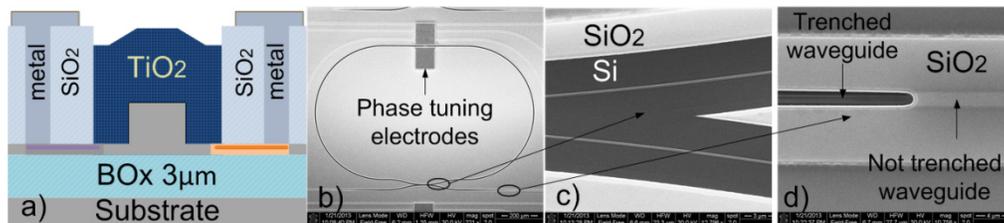


Fig. 5. fabricated devices: a) cross-section schematic of the phase tuning section in the ring resonator after filling the trench with TiO₂; b) SEM image of the ring resonator with 275 nm wide waveguide, prior to TiO₂ deposition; c) magnified view of the section of waveguide to ring directional coupler, illustrating the principle of trenching; d) transition of trenced waveguide to waveguide clad with SiO₂ (not trenced).

4. Device characterization

We characterized the fabricated devices using Optical Vector Network Analyzer (OVNA) coherent measurement tool. Time domain traces (impulse responses) and frequency domain transfer functions of a-TiO₂ clad ring resonators with different waveguide width are shown in Figs. 6(a1)-6(a4) and 6(b1)-6(b4). Time domain impulse responses are obtained by coherent OVNA measurement. In Figs. 6(a1)-6(a4), the successive impulses correspond to optical signal outputs from the ring resonator after consecutive revolutions. The rings with waveguide core widths of 400 nm, 350 nm and 300 nm are coupled to the input waveguide via a 500 nm wide gap and show progressive reduction of the extinction ratio and Q-factor. This is attributed to higher losses occurring in narrower waveguides. The ring with 250 nm wide core is coupled via a 600 nm wide gap, hence the measured extinction ratio and Q-factor increase. This gap value is also used in the ring devices with 275 nm wide waveguide. From the frequency domain responses, we can determine the Q-factor values to be 16500, 12380, 4075 and 6150, for 400 nm, 350 nm, 300 nm and 250 nm wide waveguide resonators, respectively. These correspond to photon lifetimes of 13.5 ps, 10.2 ps, 3.3 ps and 5.1 ps, that represent the ultimate limit to the speed of the modulator response [22].

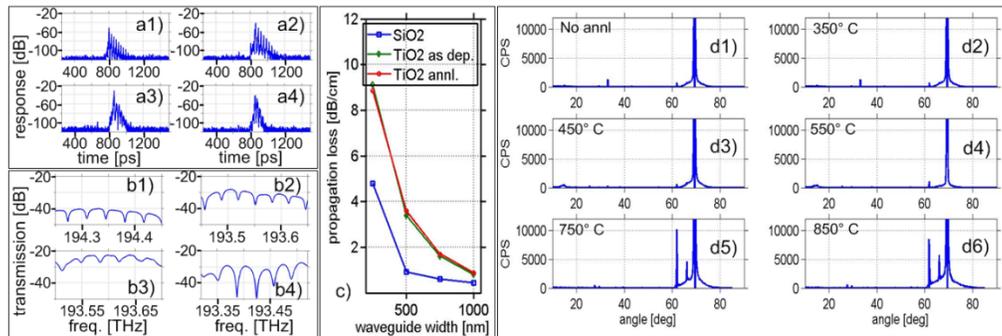


Fig. 6. a1-a4) OVNA recorded impulse responses of devices with 400 nm, 350 nm, 300 nm and 250 nm wide waveguides; b1-b4) respective frequency responses; c) comparison of propagation loss values for SiO₂ and TiO₂ (prior and post 450 °C anneal) cladding with respect to the waveguide width; d1) XRD of 'as deposited' sample and d2-d6) XRD traces of samples annealed at 350 °C, 450 °C, 550 °C, 750 °C, and 850 °C. Clear evidence of crystallization is present in d5) and d6) with dominant rutile peaks at ~62 deg and ~66 deg.

As crystallization of titanium dioxide is a potential obstacle to low loss athermal silicon photonics, we examined the thermal budget of the fabricated chips. Figures 6(d1)-6(d6) show XRD traces of rapidly thermally annealed samples. The annealing process lasted one hour in a nitrogen atmosphere, with a ramp rate of 25 °C/min and spontaneous cooling at approximately 50 °C/min. No evidence of crystallization appeared below annealing temperature of 550 °C, whereas strong rutile formations appeared at higher annealing temperatures after the same duration. The comparative optical propagation loss measurements took place for SOI ridge waveguides with SiO₂ and a-TiO₂ overclad waveguides before and after thermal annealing. We determined propagation loss values on separate waveguide test structures by Optical Time Domain Reflectometry (OTDR) method similar to [23], using the OVNA. Figure 6(c) summarizes the measured propagation loss, for three cladding materials: LPCVD SiO₂, a-TiO₂ as sputtered and a-TiO₂ after 450 °C anneal for one hour. We found no noticeable difference prior and post a-TiO₂ annealing. For instance, a 500 nm-wide a-TiO₂ over-clad waveguide measured 3.5 dB/cm loss, whereas a SiO₂ clad counterpart had about 1 dB/cm loss. 250 nm-wide waveguides measured 4.8 dB/cm loss with SiO₂ cladding and 9 dB/cm with a-TiO₂ cladding. The larger propagation loss in a-TiO₂ clad waveguides is probably due to the presence of scattering points created by imperfect filling of small gaps during the titanium dioxide sputtering process. It is worthy of mentioning that rutile formation

that occurs in samples annealed at and above 750 °C carries with it a drastic increase in waveguide propagation loss. It can only be estimated at >70 dB/cm, based on chip insertion loss, as we cannot precisely measure the propagation loss at such low output power levels. Furthermore, stress-induced cracking and delamination of the cladding often occur upon creation of rutile phase, damaging the device.

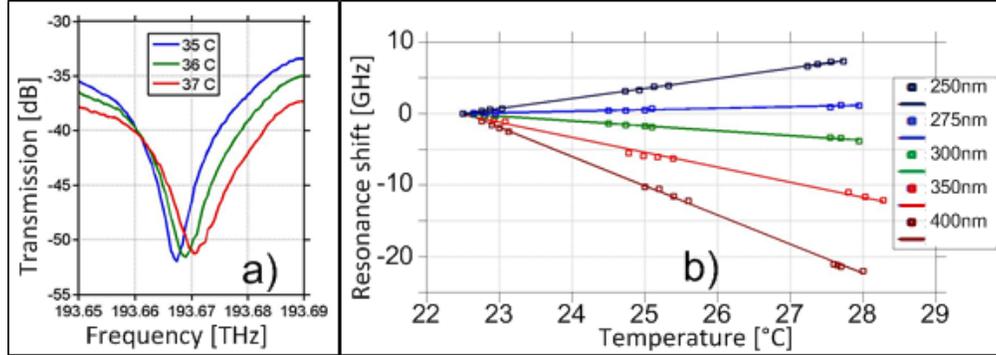


Fig. 7. a) evidence of blue shift with temperature increase in 250nm wide waveguide device b) summary of measured (square markers) and fitted values of resonant frequency shifts for different waveguide width devices. Inset marks the waveguide width.

Figure 7(c) summarizes thermal tuning measurements of ring resonator devices. Temperature was controlled by a thermo-electric cooler with Peltier element connected to the brass chuck holding the silicon chip. As expected, reducing the silicon core width increases optical confinement factor in a-TiO₂ cladding, leading to more blue-shift with temperature increase. Devices with 300 nm and wider cores show dominant red-shift, whereas the devices with narrower cores exhibit dominant blue-shift. Figure 7(b) shows strong blue shift of $-11.3 \text{ pm}/^\circ\text{C}$ ($+ 1.41 \text{ GHz}/^\circ\text{C}$) in 250 nm wide waveguide ring resonator. Of the devices available on die, one with 275 nm wide waveguide approaches the athermal condition the closest, with measured resonance blue-shift of $-1.60 \text{ pm}/^\circ\text{C}$ ($0.20 \text{ GHz}/^\circ\text{C}$). Based on the measurements, we expect that perfect athermalization would occur in 280 nm – 285 nm wide waveguide. The slight difference between this and designed value (305 nm) can result from a number of reasons. Most probable are: 1) the presence of 30 nm thick LSN layer on top of silicon waveguide core, that reduces the value of overcladding confinement factor; 2) small deviation of etch depth in fabricated waveguides; 3) presence of nano-voids that lead to imperfect coverage of waveguide by a-TiO₂, again leading to lower overcladding confinement factor; 4) small deviations in refractive indices of a-TiO₂, silicon and BOx used in calculation, from the actual values.

5. Small signal modulation bandwidth measurement

The forward resistance of P-i-N current injection trenches measured 28Ω at the bias point of $1.5 V_{\text{DC}}$. Turn-on voltage is $0.9 V_{\text{DC}}$. When statically biased to $2.3 V_{\text{DC}}$, the ring modulator with 275 nm wide waveguide showed high extinction ratio of 35 dB at the optical frequency of 193.295 THz.

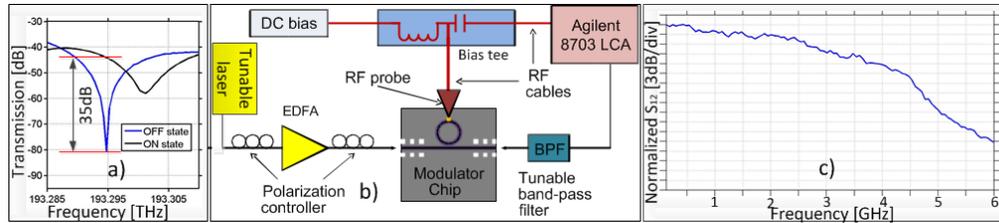


Fig. 8. Modulation performance a) static modulation by carrier injection showing blue shift of ring resonance at the bias value of $2.3V_{DC}$ b) small signal modulation bandwidth measurement setup c) LCA trace of modulation response as function of frequency.

The athermal ring waveguide design did not include high-speed operation considerations. Small-signal modulation bandwidth measurements used Agilent 8703 Light-wave Component Analyzer (LCA) at the forward bias point $1.5 V_{DC}$ and the RF signal with peak-to-peak voltage of $0.3 V_{pp}$ applied via bias tee. Figure 8(b) shows the measurement setup schematic and Fig. 8(c) shows recorded LCA trace. We observed 3 dB modulation bandwidth of about 2 GHz and 6 dB bandwidth of 2.7 GHz. Device response cuts-off sharply around 4.5 GHz. The measured bandwidth is similar to reported values [24] for carrier injection based devices, typically limited by carrier lifetime and junction capacitance [25]. Carrier injection-based ring modulators optimized for high speed show less than order of magnitude higher bandwidth [22, 26]. Design of high speed athermal modulators is in progress.

7. Conclusion

We demonstrated carrier injection based small signal modulation in silicon rings clad with high negative TOC amorphous titanium dioxide. Nearly complete athermalization of silicon ring resonators is reported. The a-TiO₂ clad silicon photonic waveguides exhibited higher losses than SiO₂ clad counterparts at 8 dB/cm near the athermal condition, and achieved a high thermal budget of more than 450 °C at one hour annealing, making this approach a candidate for BEOL CMOS integration on novel optical-electronic platforms. In addition, we are investigating methods to increase the thermal budget to beyond 450 °C for > 1 hour, for more robust and stable operation beyond standard CMOS BEOL processes. We will also investigate trimming methods for a-TiO₂ over-clad devices, incorporating possible doping materials to allow UV or other trimming to match the wavelength of the athermal devices to the desired operating wavelengths [27].

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