Concurrent error detection for finite state machines implemented with
embedded memory blocks of SRAM-based FPGAs

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Abstract

We propose a cost-efficient concurrent error detection (CED) scheme for finite state machines (FSMs) designed for implementation with embedded memory blocks (EMBs) available in today’s SRAM-based FPGAs. The proposed scheme is proven to detect each permanent or transient fault associated with a single input or output of any component of the circuit that results in its incorrect state or output. The experimental results obtained using our proprietary FSM synthesis tool show that despite the heterogeneous structure of the proposed CED scheme, the overhead is very low. For the examined benchmark circuits, the circuitry overhead in terms of extra EMBs is in the range of 6.3–56.3%, with an average value of 27.2%, whereas the combined overhead (EMBs and logic cells) calculated under pessimistic assumptions is in the range of 20.7–63.8%, with an average value of 32.2%. This compares favorably with the earlier proposed solutions applicable to conventional FSM designs based on gates and flip-flops for which an overhead exceeding 100% is quite typical.

Keywords: FPGA; Embedded memory; Finite state machine (FSM); Concurrent error detection (CED); Single event upsets (SEUs)