Design of High-Performance Analog Circuits Using Wideband $g_m$-Enhanced MOS Composite Transistors

Yang TIAN†(a) and Pak Kwong CHAN††(b), Members

SUMMARY In this paper, we present a new composite transistor circuit design technique that provides superior performance enhancement to analog circuits. By adding a composite transistor to the cascode-compensated amplifier, it has achieved a 102 dB DC gain, and a 37.6 MHz unity gain bandwidth while driving a 2 nF heavy capacitive load at a single 1.8 V supply. In the comparison of power-bandwidth and power-speed efficiencies on figures of merit, it offers significantly high values with respect to the reported state-of-the-art works. By employing the composite transistor in a linear regulator powered by a 3.3 V supply to generate a 1.8 V output voltage, it has shown fast recovery response at various load current transients, while a 1% settling time of 0.36 μs for a maximum 735 mA step under a capacitive load of 10 μF with a 1 Ω ESR resistor. The simulated load regulation is 0.035% and line regulation is 0.488%. Comparing its results with other state-of-art LDO reported results, it also validates the significant enhanced performance of the proposed composite-transistor-based design in terms of speed, current driving capability and stability against changes in environmental parameters. All the proposed designs are simulated using chartered semiconductor (CSM) 1.8 V/3.3 V 0.18 μm CMOS triple-well process technology with thin/thick oxide options and BSIM3 model parameters.

**Key words:** composite transistor, cascode compensation, regulator, gain enhancement, slew rate enhancement

1. Introduction

Composite transistors have found a very wide range of applications in analog circuits. This stems from the fact that conventional MOS transistors have their own limitations in terms of finite output resistance and small transconductance parameter from nonideal transistor characteristics. To solve the problems, different types of composite transistors [1]–[3] in the form of circuit design techniques are proposed to enhance the desired performance of analog circuits. For instance, the fundamental NMOS-PMOS composite transistor [1] shown in Fig. 1(a) gives flexibility of building cross-coupling structures on the basis of high-impedance nodes associated with the top and bottom terminals. Therefore, popular analog circuits like operational transconductance amplifiers (OTAs) for filter design, analog multipliers for communication circuits or class-AB input-stage operational amplifiers (op-amps) for high-slew-rate applications can be built in a versatile way. Moreover, the use of series transistors with a common gate [2] in Fig. 1(b) can form a composite transistor that aims at output impedance enhancement whilst permitting the use of short-channel devices for cascode-based low-voltage or wide-bandwidth analog circuit applications. Furthermore, when dealing with an amplifier output stage design as an example, the super transistor [3] shown in Fig. 1(c) can be employed to increase the $g_m$ of a single-MOS transistor by about A times by adding a differential amplifier having an open-loop gain in the feedback configuration, thus leading to a composite transistor with bootstrapped driving characteristics. Consequently, all of these examples demonstrate the benefits of applying composite transistors in MOS analog circuit designs.

The transconductance $g_m$ is regarded as one of the key parameters in analog circuit design. For high-performance analog circuits that require high $g_m$ transistors for reasons of speed, drive, gain or regulation as common examples, the design often encounters large size, high biasing current, tradeoff among frequency responses, device size and power consumption or eventually the choice of suitable process technology that suits the applications, particularly for MOS devices operating in a saturation region where $g_m$ per bias current is not as efficient as that of bipolar devices. As a result, there is a large tradeoff in the design of analog circuits, leading to a significant degradation in actual performance despite the use of advanced deep-submicron process technologies. Therefore, our objective in this paper is to propose a new economical composite transistor structure having both wideband and high-$g_m$ characteristics whilst consuming reasonable biasing power as well as a small silicon area.

Following the Introduction, Sect. 2 introduces a new NMOS composite transistor, which is developed by the $g_m$-enhanced technique, comprising a wideband embedded gain stage and a single-transistor transconductor. Section 3 gives circuit application examples, which include a new high-power-bandwidth-efficiency op-amp having a very high ca-
pactive load driving ability by employing a CMOS wide-
band $g_m$-enhanced composite transistor design approach and a new fast-settling high-drive regulator using a PMOS wide-
band $g_m$-enhanced composite transistor design approach. Section 4 presents the detailed transistor-level simulation results for validating the composite-transistor-based circuits and compares prior-art works to confirm the effectiveness of the proposed composite transistor circuit techniques. Con-
cluding remarks are drawn in Sect. 5.

2. Proposed Wideband $G_m$-Enhanced Composite Trans-
sistor

A dedicated transimpedance amplifier (TIA) [4], which aims to improve the operation bandwidth whilst keeping low power consumption for optocoupler systems, is shown in Fig. 2. The first embedded gain stage comprises (i) a voltage-to-current (VI) converter formed by a transistor $M_1$ and a current source $I_1$ and (ii) a transimpedance gain stage formed by a transistor $M_2$, a source $I_2$ and a resistor $R_{f1}$. The key advantage of using the shunt-shunt feedback in the first gain stage is to achieve power-bandwidth efficiency because the effective impedance at the input/output of the transimpedance gain stage will be significantly reduced by the shunt feedback, thus overcoming the Miller effect in the conventional inverting voltage amplifier configuration (for instance, a driving transistor with a diode-connected active load). The embedded gain stage, therefore, facilitates broadband circuit applications with a low power consumption. To achieve a higher open-loop gain in a feedback sys-

tem, a second gain stage composed of the transistor $M_3$ and the current source $I_3$ is cascaded. Hence, the overall trans-

impedance of the TIA is now defined by the outer loop feed-

back resistor $R_{f2}$. By observing the circuit architecture, part of the TIA can form the framework for devising new com-

posite transistors.

The $g_m$-enhanced technique [5] has been reported to boost the transconductance parameter through the cascade of a voltage amplifier and a transconductor to form a com-

posite gain-enhanced feedforward stage for the purpose of pole-zero cancellation in frequency compensation applications. Herewith, replacing the voltage amplifier [5] by the wideband embedded-gain stage [4] as indicated by the dotted box in Fig. 2 and arranging it to cascade with a

Fig. 2 Transimpedance amplifier using Embedded Gain Stage for broadband gain enhancement.

Fig. 3 Proposed composite transistor.

Fig. 4 Small signal model of proposed composite transistor.
\[
A_f = \frac{V_2}{V_g - V_s} = \frac{g_m R_c}{(1 + S(C_{gs} + C_g))(1 + S(C_{gs} R_c))},
\]

where \(C_1, C_2 \text{ and } C_3\) represent the lumped output parasitic capacitances for each respective stage, which are expressed as follows:

\[
\begin{align*}
C_1 & \approx C_{gs2} + C_{db1} + C_{db4}, \\
C_2 & \approx C_{gs3} + C_{db2} + C_{db5} + C_{gs3}(1 - A_c), \\
C_3 & \approx C_{db3};
\end{align*}
\]

hence, the effective frequency-dependent transconductance of the composite transistor becomes

\[
G_m = A_f \cdot g_m 3.
\]

Note that \(A_c\) in (5) is defined as the ac gain of an inverting amplifier formed by the transistor \(M_3\) and the load network being connected to the drain of \(M_3\) in the application circuit. Since \(C_1\) and \(R_c\) are not high in practice, the second pole is usually located in few GHz range. Since the enhanced-gain stage permits smaller size in \(M_3\) as another implementation advantage, the resultant \(C_2\) arising from the translated Miller effect through \(C_{gs3}\) does not become a pre-dominant term, leading to the first pole frequency being located in typical few hundred MHz range. If the circuit operation frequencies are less than the dedicated two pole frequencies, (3) and (7) can be further approximated as

\[
\begin{align*}
A'_f & \approx g_m 1 \cdot R_c, \\
G'_m & = g_m 1 R_c g_m 3;
\end{align*}
\]

and they will not lose much accuracy through simplification. These two equations will be used for circuit analysis in the subsequent sections.

## 3. Composite Transistor Exemplary Applications

### A. Amplifier using \(g_m\)-Enhanced Composite Transistor

For amplifiers driving very heavy capacitive loads, cascode compensation [3], [6] is a natural choice because the heavier the load, the more efficient the compensation is. Unlike other compensation schemes that rely on accurate pole-zero cancellation at a specific capacitive load, the cascode compensated amplifiers usually display higher robustness because there is no need to maintain pole and zero tracking even in the case of a large variation in capacitive load. The remaining problem is solving the slew rate issue under a heavy capacitive load since slew rate is strongly linked to power consumption.

In cascode compensation, the increase in cascode ratio, which is defined as the ratio of compensation capacitance to internal node parasitic capacitance, can shift the output pole at higher frequencies but inducing a peaking effect and the reduction in gain and phase margin for stability. To circumvent the problem, the increase in the driving device’s \(g_m\) becomes another option but it suffers from the substantial increase in current consumption due to the square root relationship between \(g_m\) and bias current. Consequently, the \(g_m\)-enhanced approach, making use of a wideband composite transistor, is a good choice because it does not require a large cascode ratio. There are many methods of blocking the feedforward zero; the use of a current buffer [6] or a voltage buffer [7] or the feeding of the cascode compensation capacitor to the current mirror [3]. Herewith, the proposed design is based on the latter approach.

Figure 5 shows the simplified schematic of the cascode-compensated amplifier with a class-AB output stage. The transistors \(M_0 - M_6\) form a standard differential input stage having a high-swing cascode current mirror as active load. The new output stage is synthesized by the embedded gain stage [4] and the economic CMOS push-pull structure [8], [9]. Such a cascaded entity forms a wideband \(g_m\)-enhanced CMOS composite transistor output stage dedicated to boost the gain as well as the bandwidth of the amplifier circuit. As illustrated, the compensation capacitor \(C_c\) bridges between the output and the low-impedance source terminal of the cascode transistor, thus blocking the feedforward zero in an economical way [3]. By referring to Fig. 5, the internal nodes X and Y are level-shifted by a floating battery capacitor \(C_{bat}\), which serves as a voltage divider with respect to the lumped parasitic capacitance \(C_{gs}\) at node Y, thus producing some attenuation of small ac signals according to

\[
V_y = \eta \cdot V_x,
\]

where \(\eta = C_{bat}/(C_{bat} + C_y)\) is defined as the coupling ratio. The transistor \(M_{16}\) functions as a very large resistor \(R_{surge}\), which is often called a pseudoresistor, and is realized using a minimum size diode-connected PMOS transistor having its source and substrate terminal connected together. It operates in a cutoff region where its resistance is extremely high. The effective resistance is based on the leakage resistance in pn junctions. The PMOS transistor is relatively weaker than its NMOS counterpart. In order to improve the slew rate of the PMOS output transistor, a modified slew rate enhancement circuit (formed by the transistors \(M_7 - M_9\)) is added to the amplifier. The transistor \(M_7\) is designed in such a way that it is only activated during large positive transient condition. Under a large-signal operation, the transistor \(M_1\) turns off whereas the transistor \(M_2\) turns on. The voltage at point G surges high, thus turning on the transistor \(M_7\). As a result, current starts to be drawn in the
transistor $M_b$ and this will be bootstrapped further by another mirror transistor $M_b$ to ultimately increase the sourcing current to the load. On the other side, the potential of node A decreases simultaneously, and it is amplified by the embedded gain stage that further pulls the gate potential of $M_3$ to low for sourcing current to load. Compared with the reported method [10], it also consumes no power under normal operation but it produces a much larger slewing current due to the combined sourcing effect of the mirror transistor $M_b$ and the output transistor $M_{13}$. This looks like a double slew rate enhancement effect.

Figure 6 shows the small-signal model of the proposed amplifier. The transistors $M_1$ and $M_2$ are assumed identical to the transistors $M_3$ and $M_6$. Note that $g_m$ and $r_{oi}$ are respectively defined as the transconductance and output resistance of the respective device, whereas $C_i$ denotes the lumped output parasitic capacitance of the stage. As $R_{o2} \gg 1/g_m$, the voltage at node G is approximately equal to $g_m V_i/(1+g_m r_{oi2}) \approx g_m V_i/g_m r_{oi2}$, the current flowing through the transistor $M_3$ becomes $g_m V_i = g_m V_i/(1+g_m r_{o2}) \approx g_m V_i/g_m r_{o2}$.

From the push-pull output stage composed of the transistors $M_{12}$ and $M_{13}$, the combined transconductance is $g_{m12} + \eta \cdot g_{m13}$. Further incorporating the $g_m$-enhanced $A_f$ stage, the effective transconductance of the composite transistor becomes $G_m = A_f (g_{m12} + \eta \cdot g_{m13})$. To derive the transfer function of this new amplifier from the small-signal model denoted in Fig. 6, the KCL is applied at nodes A, B and C to yield the nodal equations as follows:

$$\begin{align*}
\frac{g_{m1} V_i}{2} + \frac{V_A}{R_{OA}} + SC_A V_A - g_{m3} V_B - \frac{V_B - V_A}{r_{03}} &= 0, \\
\frac{g_{m2} V_i}{2} + \frac{V_B}{R_{OB}} + SC_B V_B + g_{m3} V_B + S C_V (V_B - V_O) + \frac{V_B - V_A}{r_{03}} &= 0, \\
G_m V_A + \frac{V_O}{R_L} + SC_L V_O + S C C (V_O - V_B) &= 0.
\end{align*}$$

(10) (11) (12)

Since $r_{03}$ is in the $\Omega$ range, the term $V_B - V_A/r_{03}$ is much smaller than the term $g_{m3} V_B$ in (10) and (11). To simplify the analysis, the term $-V_B - V_A/r_{03}$ is ignored. From the above equations, the transfer function of the new topology can be derived as

$$\frac{v_A(S)}{v_i} = \frac{n_0 + n_1 S + n_2 S^2}{a_0 + a_1 S + a_2 S^2 + a_3 S^3},$$

(13)

where the coefficients are obtained as follows:

$$\begin{align*}
a_0 &\approx 2 g_{m3} R_o B, \\
a_1 &\approx 2 g_{m3} C C R_o A R_o B R_L, \\
a_2 &\approx 2 g_{m3} C A R_o A R_o B (C_C + C_L), \\
a_3 &\approx 2 C_A C C C_L R_o A R_o B R_L, \\
η_0 &\approx 2 g_{m3} C C R_o A R_o B R_L, \\
n_1 &\approx g_m C C R_o A R_o B R_L, \\
n_2 &\approx -g_m C C R_o A R_o B R_L, \\
\end{align*}$$

(14) (15) (16) (17) (18) (19) (20)

the assumptions are based on $g_m > 1/R_o$.

From the transfer function, DC gain is estimated as

$$\begin{align*}
A_{DC} &\approx \frac{n_0}{a_0} = A_f (g_{m12} + \eta \cdot g_{m13}) R_o A R_L, \\
\end{align*}$$

(21)

where $A_f = g_{m10} R_o$. It is apparent that the overall DC gain of the proposed two-stage op-amp will be increased by the push-pull output structure incorporating the embedded gain stage. It offers higher open-loop gain than that of the standard two-stage architecture whilst having an advantage of supporting high-gain high-speed operation. In contrast, the multistage amplifiers larger than the two stages often suffer from a severe tradeoff between speed and gain in design considerations. If the dominant, second and third poles are widely separated, they can be estimated as follows:

$$\begin{align*}
p_1 &\approx -\frac{a_0}{a_1} = -A_f (g_{m12} + \eta \cdot g_{m13}) C_C R_o A R_L, \\
p_2 &\approx -\frac{a_1}{a_2} = -A_f (g_{m12} + \eta \cdot g_{m13}) C_C (C_C + C_L) C_A, \\
p_3 &\approx -\frac{a_2}{a_3} = -g_m (C_C + C_L) C_A C_L.
\end{align*}$$

(22) (23) (24)

As can be seen in (22), the dominant pole $p_1$ is now shifted to a very low frequency owing to the $A_f$ term in the composite transistor. The $g_m$-enhanced gain factor $A_f$ and the combined conductance of the push-pull stage and cascode ratio significantly push the nondominant pole $p_2$ towards higher frequencies, which permits the cascode compensated op-amp exhibiting a larger unity gain bandwidth despite its very heavy capacitive load. This illustrates the technical merit of the proposed composite transistor. Besides, the nondominant pole $p_3$ is also located at a high frequency when the value of the compensation capacitor is made small. No peaking effect occurs as long as $p_3$ and $p_2$ do not collide with each other to create complex poles during pole splitting.

Similarly, the two zeros are obtained by solving the roots of $n_0 + n_1 S + n_2 S^2 = 0$ in (13), resulting in a left-half-plane (LHP) zero and a right-half-plane (RHP) zero as follows:

$$\begin{align*}
Z_1 &= A_f (g_{m12} + \eta \cdot g_{m13}) C_A C_L, \\
Z_2 &= \frac{n_1}{n_2}. \\
\end{align*}$$

(25)
B. Regulator Using $g_m$-Enhanced Composite Transistor

Using the proposed composite transistor as a replacement of the power transistor in the conventional regulator is an excellent solution. The rationales are that of keeping a reasonably small power transistor size and a small static biasing power whilst offering a high current driving capability. The embedded gain of the composite transistor offers the same function as the buffer stage and provides a gain to improve the current driving capability of the regulation transistor. The composite transistor topology is quite simple when compared with the canonical techniques using the buffer stage. The block diagram of the improved regulator is shown in Fig. 7. It consists of an error amplifier, a compensation capacitor $C_C$ for the error amplifier, a composite transistor, a feedback network and an external parallel load consisting of a resistive load $R_L$ and an external capacitor $C_{OUT}$ having a series resistance $R_{ESR}$. The error amplifier in Fig. 8 is a typical folded cascode configuration. Therefore, it is not explained further here. The composite transistor in Fig. 9 is a PMOS version of its NMOS counterpart in Fig. 3.

In a conventional regulator circuit [11], transient response time can be estimated as

$$Z_2(RHP) = \frac{-n_1 + \sqrt{n_1^2 - 4n_0 \cdot n_2}}{2n_2} \approx \frac{2g_{m3}}{C_C} \quad (26)$$

Since they are usually located at much higher frequencies, they are of no importance in the compensation design. Assume that $P_2, P_3, Z_1$ and $Z_2$ are much larger than the unity gain frequency $GBW$, which is identical to that for the typical two-stage Miller compensated amplifier.

The improved regulator benefits the design as follows: (i) the size of the pass transistor is significantly reduced through the enhanced gain stage, resulting in a reduction in the slew time on the basis of the reduced $C_{par}$, (ii) the shunt feedback of the embedded gain stage reduces effective output resistance, which in conjunction with $C_{par}$ further reduces the time constant of the third pole such that it is easy to keep what far away from the unity-gain frequency of the regulator system, and (iii) the power consumption of the error amplifier can be reduced without being constrained by the pass transistor. Consequently, the first pole of the new regulator is defined by the output resistance of pass transistor and external capacitor load. The second pole is defined by the time constant at the output of error amplifier. The second zero is generated from the output capacitance and its ESR resistance. The second zero is also made closer to the second pole so as to cancel the phase shift effect such that the overall open-loop gain response of the regulator is approximated as a one-pole system. The third pole arising from the reduced time constant at the output of the embedded gain stage is located at a much higher frequency than the usual unity gain frequency of a regulator system. This gives more headroom for the increase in unity gain frequency by increasing load current. As a result, the composite transistor-based regulator is sta-
4. Results and Discussions

The composite-transistor-based analog circuits are designed on the basis of Chartered Semiconductor (CSM) 1.8 V/3.3 V 0.18 μm CMOS triple-well process technology with thin/thick-oxide options and BSIM3 model parameters. In order to verify the operation and assess the performance of the proposed circuits, all the simulations were performed using a Cadence Spectre simulator.

A. Simulation Results of the Proposed Amplifier

Table 1 shows a list of each transistor parameter together with its transconductance. As can be seen, the aspect ratios of the output transistors $M_{12}$ and $M_{13}$ are small, demonstrating how the embedded gain stage helps reduce the driving devices’ size. Table 2 shows a summary of the performance parameters of the proposed cascode op-amp under typical conditions. From the Bode plot in Fig. 10, it can be observed that the amplifier is stable and shows the absence of the peaking effect at a capacitive load of 2 nF. Owing to the wideband and gain-enhanced characteristics of the composite transistor for improved cascode compensation, the obtained unity gain-bandwidth is huge as well as the corresponding small settling times, as observed consistently in Fig. 11. Moreover, the slew rates in Fig. 11 are reasonably good even under heavy capacitive load, which is due to the improved driving characteristic of the composite transistor as well as the slew rate enhancement. From the robustness viewpoint, it is desirable for the amplifier to drive a capacitive load with a wide tolerance. For instance, the improved cascode op-amp can serve as an error amplifier to drive the gate-source capacitance load arising from an external discrete power device, having a typical value of about 1 nF or much larger. In order to confirm that the amplifier is stable against the variation in capacitive load, a Bode plot is presented in Fig. 12. It is interesting to observe that a very light peaking effect starts to appear when the capacitive load is reduced to 1.13 nF (−43.5% of nominal value of 2 nF), whilst still getting an acceptable gain margin of −5 dB and a phase margin of 56.9 deg. This means that no significant peaking effect occurs when the load capaci-
tance is from 1.13 nF onwards, indicating a wide tolerance of the amplifier. These figures support that the amplifier has robust characteristics against environmental changes in parameters. In other words, it also confirms the effectiveness of the composite transistor design approach for realizing natural frequency compensation without the need for accurate pole-zero compensation at a specific capacitive load. The embedded gain stage circuit consumes 353 μA, which is 43% of total current consumption of the proposed amplifier. However, as can be seen in the later results, the ultimate bootstrapped performance outweighs the increase in power as the tradeoff.

In order to validate the effectiveness of the proposed composite transistor design methodology, the results of previously reported high-performance frequency compensation amplifiers are summarized for comparison in Table 3. Here-with, the key op-amp parameters together with the well known figures of merit in terms of $FOM_g = GBW \cdot C_L/\text{power}$ and $FOM_{SL} = SR \cdot C_L/\text{power}$ from the power dissipation perspective are presented; $IFOM_g = GBW \cdot C / \text{IDD}$ and $IFOM_{SL} = SR \cdot C_L/I_{DD}$ from the total supply current consumption perspective are included. It is apparent that the results of the proposed amplifier either outperform or compare favorably with the reported results on critical figures of merit on the basis of power-bandwidth efficiency and power-speed efficiency. This demonstrates that the proposed composite transistor can enhance the performance of analog circuits significantly. Its simplicity is also favorable for economical implementation as well as for robust applications.

### B. Simulation Results of the Proposed Regulator

The size of each component in the embedded gain stage is given in Table 4. The embedded gain stage circuit consumes 94.8 μA, which is 67.95% of the total regulator power consumption. As can be seen in later results, the superior performance enhancement justifies the increase in power as the tradeoff. The aspect ratio of the power transistor is 1000. It is based on a parallel system of 100 unit transistors having an aspect ratio of 30 μm/0.3 μm. Consider the current six-metal process; it can support the given unit transistor to handle the worst-case maximum of 10 mA by overlapping metals for power routing in a multiple-finger-based transistor structure. Hence, a power transistor comprising 100 unit transistors will draw a maximum current of 1A. For the design of a sub-Ampere regulator, metal electromigration (EM) is considered. The voltage generated from the bandgap circuit is 1.2 V. To set the regulator’s output voltage to be equal to 1.8 V, the feedback resistance are as $R_{FB1} = 200 \, k\Omega$ and $R_{FB2} = 400 \, k\Omega$. The error amplifier has an open-loop gain of 62.2 dB, a unity gain bandwidth of 1.53 MHz and a phase margin of 83.49° at a capacitance load of 10 pF.

The conventional regulator and composite-transistor-based regulator drive one off-chip capacitor $C_{out} = 10 \, \mu F$ with $R_{ESR} = 1 \, \Omega$. The performance comparison with those in other reported works is summarized in Table 5.

![Fig. 12](image-url) Bode plot of proposed amplifier with ±43.5% load variation.

### Table 3 Comparison with published frequency compensation techniques.

<table>
<thead>
<tr>
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<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.6 μm CMOS</td>
<td>0.8 μm CMOS</td>
<td>0.5 μm CMOS</td>
<td>0.18 μm CMOS</td>
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<td>Gain(dB)</td>
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<td>&gt; 100</td>
<td>100</td>
<td>99.5</td>
<td>102</td>
</tr>
<tr>
<td>GBW(MHz)</td>
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<td>1</td>
<td>2.87</td>
<td>27.27</td>
<td>37.6</td>
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<td>PM</td>
<td>63.7°</td>
<td>58.6°</td>
<td>59°</td>
<td>59.4°</td>
<td>67.2°</td>
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<tr>
<td>Mean SR(V/μS)</td>
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<td>0.36</td>
<td>1.55</td>
<td>0.845</td>
<td>3.5</td>
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<tr>
<td>$C_L$(pF)</td>
<td>300</td>
<td>1000</td>
<td>500</td>
<td>500</td>
<td>2000</td>
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<td>$C_p$(pF)</td>
<td>6</td>
<td>$C_a = 55$</td>
<td>$C_a = 69$</td>
<td>5764</td>
<td>5753</td>
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<td>$FOM_g$(MHz/μF/mW)</td>
<td>1273</td>
<td>2347</td>
<td>5764</td>
<td>5753</td>
<td>49311.5</td>
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<tr>
<td>$FOM_{SL}$(V/μS/μF/mW)</td>
<td>429</td>
<td>845</td>
<td>5112</td>
<td>1782.7</td>
<td>49902.2</td>
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<tr>
<td>$IFOM_g$(MHz/μF/μA)</td>
<td>3819</td>
<td>4694</td>
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<td>52188</td>
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<td>$IFOM_{SL}$(V/μS/μA)</td>
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<td>8264.5</td>
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<tr>
<td>$V_{ref}$(V)</td>
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<td>3</td>
<td>1.5</td>
<td>1.8</td>
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<tr>
<td>$I_{sat}$(mA)</td>
<td>0.817</td>
<td>0.2</td>
<td>0.083</td>
<td>0.16</td>
<td>0.847</td>
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<tr>
<td>Power(mW)</td>
<td>2.45</td>
<td>0.0426</td>
<td>0.249</td>
<td>0.237</td>
<td>1.525</td>
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### Table 4 Value of each component in the embedded gain stage.

<table>
<thead>
<tr>
<th>Components</th>
<th>Size</th>
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<tbody>
<tr>
<td>$M_1$</td>
<td>10 μm/0.36 μm</td>
</tr>
<tr>
<td>$M_2$</td>
<td>30 μm/0.36 μm</td>
</tr>
<tr>
<td>$M_3$</td>
<td>6 μm/1 μm</td>
</tr>
<tr>
<td>$M_5$</td>
<td>0.16 μm/1 μm</td>
</tr>
<tr>
<td>$R_c$</td>
<td>100 kΩ</td>
</tr>
</tbody>
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Table 5 Comparison with published LDO techniques.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SRE LDO [17]</th>
<th>DFC LDO without Cap. [18]</th>
<th>DFC LDO with Cap. [18]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.6μm CMOS</td>
<td>0.6μm CMOS</td>
<td>0.6μm CMOS</td>
<td>0.18μmCMOS</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>3 V</td>
<td>3 V</td>
<td>3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>$I_{out}$</td>
<td>N.A.</td>
<td>38 μA</td>
<td>38 μA</td>
<td>139.5 μA</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>N.A.</td>
<td>0 μF</td>
<td>10 μF</td>
<td>10 μF</td>
</tr>
<tr>
<td>$R_{ESR}$</td>
<td>N.A.</td>
<td>0 Ω</td>
<td>1 Ω</td>
<td>1 Ω</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>N.A.</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.035%</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>N.A.</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.488%</td>
</tr>
<tr>
<td>1% settling time (1 mA→50 mA)</td>
<td>1.8 μS</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.1 μS/0.06 μS</td>
</tr>
<tr>
<td>1% settling time (1 mA→100 mA)</td>
<td>N.A.</td>
<td>2 μS/2 μS</td>
<td>1.6 μS/1.6 μS</td>
<td>0.1 μS/0.07 μS</td>
</tr>
<tr>
<td>1% settling time (1 mA→735 mA)</td>
<td>N.A.</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.36 μS/0.25 μS</td>
</tr>
</tbody>
</table>

For the transient load current step of 50 mA in Fig. 13, it can be shown that the worst 1% settling time is 0.1 μS in the new regulator. This is faster than that reported in [17] by 18-fold. Similarly, for a transient load current step of 100 mA in Fig. 14, the worst 1% settling time is 0.1 μS. Compared with the DFC regulator [18] at the same transient step current, the new regulator is significantly faster by at least 20- or 16-fold with respect to the two types of design in Table 5. According to Fig. 15, the regulator using the composite design approach can drive a maximum current of 735 mA while the 1% settling times for the rising and falling edges are 0.36 μS and 0.25 μS, respectively. The simulated open-loop responses of the proposed regulator at respective 1 mA, 50 mA, 100 mA and 735 mA are shown in Fig. 16. The unity gain bandwidth is obtained as 0.29 MHz, 4.1 MHz, 5.5 MHz and 8.7 MHz, respectively. This has validated the notion that the critical third pole, contributed by the embedded gain stage and the input gate capacitance of the power transistor, is located above the unity gain frequencies and hence an approximate one-pole system is always maintained at different load currents. This confirms that the composite transistor offers huge current driving capability in regulator design. Besides, the unity-gain frequency of 5.5 MHz at a 100 mA load current is much higher than those of the reported designs having typical unity-gain fre-
frequencies of 300–500 kHz. This confirms the theory that the composite transistor can improve the transient response time of the regulator. By referring to Fig. 17, the new regulator output voltage stays almost constant even up to approximately 735 mA load current, yielding 0.035% in load regulation. The line regulation indicates 0.488% in Fig. 18. All of these performance characteristics demonstrate improvements in the speed efficiency, and stability of the composite-transistor-based design.

5. Conclusion

A new composite transistor circuit design technique is presented in this paper, and different types of composite transistors are introduced for different application scenarios. They have demonstrated significant improvement in analog circuit performance through a series of circuit design examples such as the cascode-compensated amplifier and linear regulator. The circuit simulation results have confirmed the efficiency, effectiveness and superiority of the design employing the composite transistor design approach. This is also supported further by a series of comparisons with state-of-art works, confirming the technical merits of reliability, robustness and performance-enhanced characteristics using the proposed composite transistor design approach.

References

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