Efficient Application of Modern Logic Synthesis in FPGA-based Designing of
Information and Signal Processing Systems

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Abstract

The goal of this paper is to promote application of logic synthesis methods and tools in different tasks of modern digital designing. The paper discusses functional decomposition methods, which are currently being investigated, with special attention to balanced decomposition. Since technological and computer experiments with application of these methods produce promising results, this kind of logic synthesis will probably dominate the development of digital circuits for FPGA structures. Many examples confirming effectiveness of decomposition method in technology mapping in digital circuits design for cryptography and DSP applications are presented.

1. Introduction

The influence of advanced logic synthesis procedures on the quality of hardware implementation of signal and information processing systems is especially important in case of applications targeted to FPGA structures based on look-up tables (LUT). Direct cause of such situation is imperfection of technology mapping methods that are currently widely used such as minimization and factorisation of Boolean function, which are traditionally adapted to be used for structures based on standard cells. These methods transform Boolean formulas from the form of sum-of-products into multilevel, highly factorised form that is then mapped into LUT cells. This process is at variance with nature of LUT cell, which from the logic synthesis’ point of view is able to implement any logic function of limited input variables. For this reason in case of implementation targeted to FPGA structure the decomposition is much more efficient method. The decomposition allows synthesizing the Boolean function into multilevel structure that is build of components, each of which is in form of LUT logic block specified by truth tables. Efficiency of functional decomposition has been proved in many theoretical papers [1, 2, 11, 12, 13, 14, 15]. However, there are relatively few papers where functional decomposition procedures were compared with analogous synthesis methods used in commercial design tools. Direct cause of such situation is lack of appropriate interface software that would allow transforming description of project structure obtained outside commercial design system into description compatible with its rules. Moreover, the computation complexity of functional decomposition procedures makes it difficult to construct efficient automatic synthesis procedures. These difficulties – at least partially – have been eliminated in so called balanced decomposition [5, 6, 9].

In this paper, first DEMAIN system that implements balanced decomposition is presented. Next, on the example of simple binary to BCD encoder, the influence of the method on technology mapping in FPGA structure is shown. Following that, the efficiency of decomposition procedures in hardware implementation of cryptographic and DSP algorithms is discussed.

2. Balanced functional decomposition

Here we review only some information that is necessary for an understanding of this paper. More detailed information concerning balanced functional