Continuous-conduction-mode SEPIC converter with low reverse-recovery loss for power factor correction


Abstract: A continuous-conduction-mode SEPIC converter with low reverse-recovery loss is proposed for power factor correction. The proposed SEPIC converter can reduce the reverse-recovery loss of the diodes and improve the power efficiency. By utilising a coupled inductor and an additional diode, zero-current turn-off of the output diode is achieved. The reverse-recovery current of the additional diode is reduced by the leakage inductor of the coupled inductor. The proposed SEPIC converter provides high power efficiency and high power factor compared to the conventional PFC circuits employing the SEPIC converter. An operation principle and a detailed analysis of the proposed converter are presented. Experimental results are discussed for a 300 W (330 V/0.9 A) prototype under the universal input voltage (90–265 V). It is shown that the efficiency of the SEPIC converter can be significantly improved.

1 Introduction

High current harmonics and high pulsating current drawn from a full-bridge diode rectifier are the main causes of line current harmonic pollution in power supply systems. Stringent international standards such as IEC 61000-3-2 and IEEE 519 impose harmonic restrictions on recent electronic equipment, which have resulted in significant research efforts on PFC circuits [1, 2]. Among various power factor correction (PFC) circuits, the single-ended primary inductance converter (SEPIC) has the desirable features of its continuous input current, ripple current reduction, and wide output voltage range [3, 4]. To achieve high power density and fast transient response, the SEPIC converter should operate with high switching frequency. However, as the switching frequency increases, the reverse-recovery current of the output diode affects the switching devices in the form of additional switching losses. Other adverse effects of the reverse-recovery problem include electromagnetic interference (EMI) noises and additional thermal management. Also, the switch utilisation factor in the SEPIC converter is much lower than that of other topologies, such as the buck and boost converters [5]. In other words, the power-handling capabilities of the semiconductor devices in the SEPIC converter are much lower than those of the buck or the boost converter at the same power level. Thus, the reduction of reverse-recovery loss is particularly important for the SEPIC converter.

To deal with these problems, discontinuous-conduction-mode (DCM) SEPIC converters were presented [6, 7]. The converters make the line current naturally follow the sinusoidal input voltage waveform without the need for sensing and controlling the input current. The reverse-recovery loss of the output diode can be eliminated. However, high current stress degrades the converter efficiency and limits its application range. The boundary-conduction-mode (BCM) SEPIC converter [8] and its modified topology [9] were proposed to minimise the reverse-recovery loss of the output diode using a variable frequency control method. The converters work with zero-current turn-on of the switch and zero-current turn-off of the output diode. Although the diode reverse-recovery problem is effectively reduced, the current stresses on the switching devices are significantly increased. Moreover, it is difficult to design the EMI filter and the control circuit owing to the variable frequency control method [8, 9].

As different alternatives, the passive and the active snubber circuits have been adopted to reduce the reverse-recovery loss of the output diode [10, 11]. In [10], regenerative passive snubber circuits were applied to the continuous-conduction mode (CCM) SEPIC converter [12]. The diode reverse-recovery current and the switching loss are reduced by the passive snubber circuits. However, the circulating current in the resonant snubber circuit increases voltage and current stresses, thus degrading the converter efficiency. Meanwhile, the active snubber circuit can alleviate the reverse-recovery loss of the output diode and enable the switches to turn-on under zero-current-switching (ZCS) condition [11]. However, an additional switch and its control circuitry are needed. The methods presented in [10, 11] require a relatively high number of switching devices, which increase the cost and complexity of the converter.

In this paper, a CCM SEPIC converter with low reverse-recovery loss is proposed for PFC, as shown in Fig. 1. The proposed SEPIC converter can reduce the reverse-recovery loss of the diodes and improve the power efficiency. Zero-current turn-off of the output diode is achieved by utilising a coupled inductor and an additional diode. The reverse-recovery current of the additional diode is reduced by the leakage inductor of the coupled inductor. The proposed SEPIC converter does not suffer from voltage and current stresses compared with the previous approaches. With a simple passive approach, the power efficiency of the SEPIC converter can be significantly improved. An operating principle and a detailed analysis of the proposed SEPIC converter can be significantly improved.
converter are presented. The design considerations are discussed in detail. Experimental results based on a 300 W (330 V/0.9 A) prototype under the universal input voltage (90–265 V) are verified to show the performance of the proposed SEPIC converter.

2 Operation of proposed converter

The circuit diagram of the proposed CCM SEPIC converter is shown in Fig. 1. The proposed converter can be divided into two parts. The first part is the CCM SEPIC converter, composed of \( L_1, L_2, C_p, C_o, D_o, D_s, D_1, D_2, S_p \) and \( S_p \). The second part is an additional branch consisting of a diode \( D_o \) and the secondary windings of a coupled inductor \( L_2 \). The second part provides zero-current turn-off of the output diode \( D_o \). The leakage inductor of a coupled inductor \( L_{lk} \) is modelled as a combination of the magnetising inductor \( L_m \) and an ideal transformer with the turns ratio of \( 1:N \) (\( N > 1 \)). The leakage inductor \( L_{lk} \) has large capacitance so that the output voltage is considered constant. Since the switching frequency \( f_s \) of the proposed converter is much higher than the frequency of the input voltage, the input voltage is considered constant as \( V_i \) in one switching period \( T_s \). Also, the voltage across the capacitor \( C_p \) follows the input voltage and can be considered constant in one switching period. The internal capacitance \( C_S \) of the switch \( S_p \) participates in the operating principle. The operating waveforms of the proposed CCM SEPIC converter are shown in Fig. 3. The freewheeling current \( i_{fsw} \) flows through \( L_m1 \) and \( L_m2 \) to satisfy the charge balance of the capacitor \( C_p \). Figure 3a shows the corresponding waveforms of the proposed converter when the converter is in boost operation mode. Figure 3b shows the corresponding waveforms of the proposed converter in the buck operation mode. The proposed SEPIC converter has five distinct operating modes in one switching period \( T_s \), as shown in Fig. 4.

Mode 1 \([t_0, t_1]\): At \( t_0 \), the switch \( S_p \) is already turned on and the diodes \( D_o \) and \( D_s \) are turned off. The magnetic energy is stored in the inductors \( L_{m1} \) and \( L_{m2} \). Since the diodes \( D_o \) and \( D_s \) are reverse-biased, the output capacitor \( C_o \) provides the load current. Then, the switch current \( i_S \) increases linearly at the rate of

\[
\frac{di_S}{dt} = V_i \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right)
\]

At the same time, the diode \( D_o \) is turned off with reverse voltage \( v_{Do} \), as follows:

\[
v_{Do} = V_o + NV_i
\]

Mode 2 \([t_1, t_2]\): At \( t_1 \), the switch \( S_p \) is turned off and the voltage \( v_S \) across the switch \( S_p \) begins to increase. The diode \( D_s \) starts conducting when the voltage \( v_S \) reaches the following voltage:

\[
v_S = \frac{V_o + NV_i}{N}
\]

When the voltage \( v_S \) reaches \( V_o + V_i \), the output diode current \( i_{Do} \) begins to increase. However, a stray inductance exists in the loop composed of the switch \( S_p \), the output diode \( D_o \), and the output capacitor \( C_o \). Then, the increasing rate of the diode currents is determined according to inductance values. At the end of mode 2, the sum of the diode currents \( i_{D_o} \) and \( i_{Do} \) becomes that of the inductor currents \( i_{L_{m1}} \) and \( i_{L_{m2}} \). Additionally, the stray inductance also gives a parasitic oscillation. This parasitic oscillation continues for some time in the next mode.

Mode 3 \([t_2, t_3]\): A constant voltage \( (N - 1)V_i \) is applied to the leakage inductor \( L_{lk} \). During this interval, the energy stored in the inductor \( L_{m2} \) is transferred to the load through the diodes \( D_o \) and \( D_s \). Then, the output diode current \( i_{Do} \)

![Fig. 1 Proposed SEPIC converter](image1.png)

![Fig. 2 Simplified circuit model of proposed converter that shows reference directions of currents and voltages](image2.png)
decreases while the diode current $i_{Ds}$ continues to increase through the leakage inductor $L_{lk}$ at the rate of

$$\frac{di_{Ds}}{dt} = \frac{(N - 1)V_o}{L_{lk}}$$

(4)

The decreasing rate of the output diode current $i_{Do}$ can be represented as

$$\frac{di_{Do}}{dt} = -V_o \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} + \frac{N - 1}{L_{lk}} \right)$$

(5)

Then, the current $i_{Lm2}$ of the coupled inductor $L_2$ decreases at the rate of

$$\frac{di_{Lm2}}{dt} = -V_o \left( \frac{1}{L_{m2}} + \frac{N - 1}{L_{lk}} \right)$$

(6)

At $t_3$, the output diode $D_o$ is turned off and zero-current turn-off of the diode $D_o$ is achieved.

**Mode 4 $[t_3, t_4]$**: The output voltage $V_o$ is applied across the leakage inductor $L_{lk}$ and the secondary windings of the coupled inductor $L_2$. The inductor currents $i_{Lm1}$ and $i_{Lm2}$ are transferred to the load through the diode $D_o$. Then, the diode current $i_{Ds}$ decreases linearly at the rate of

$$\frac{di_{Ds}}{dt} = -V_o \left( \frac{1}{L_{m1}} + \frac{N - 1}{L_{lk}} \right)$$

(7)

and the increasing rate of the inductor current $i_{Lm2}$ is represented as

$$\frac{di_{Lm2}}{dt} = \frac{NV_o}{N^2 L_{m2} + L_{lk}}$$

(8)

**Mode 5 $[t_4, t_0]$**: At $t_4$, a turn-on signal $v_{gs}$ is applied to the gate of the switch $S_p$. During the turn-on process of the switch, the diode $D_s$ is not immediately turned off because the reverse-recovery process makes the diode $D_s$ conduct reversely to discharge the reverse-recovery charge of the diode. Since the decreasing rate of the diode current $i_{Ds}$ is controlled by the leakage inductor $L_{lk}$, its reverse-recovery current can be reduced when the switch $S_p$ is turned on. During this interval, a constant voltage $V_o + NV_i$ is applied reversely to the leakage inductor $L_{lk}$ and the decreasing rate of the diode current $i_{Ds}$ is represented as

$$\frac{di_{Ds}}{dt} = \frac{V_o + NV_i}{L_{lk}}$$

(9)

The stored charge is recovered from the junction of the diode $D_o$. The diode $D_s$ blocks reverse voltage as in mode 1 at the end of mode 5. The next switching period is repeated when the diode current $i_{Ds}$ becomes zero.

### 3 Analysis of proposed converter

The voltage conversion ratio of the proposed CCM SEPIC converter can be obtained from the volt–second balance of the inductor $L_{m1}$ in one switching period $T_s$ as follows:

$$\frac{V_o}{V_i} = \frac{D}{1 - D}$$

(10)

and the input voltage $V_i$ is given by

$$V_i = \sqrt{2} V_o \sin \omega_L t$$

(11)
where $V_s$ and $\omega_L$ are the RMS value and the angular frequency of the input voltage $v_p$, respectively. Suppose that the ripple component of the inductor current $i_{Lm1}$ is negligible, the input current $i_i$ can be then represented as follows:

$$i_i = i_{Lm1,\text{avg}} = \frac{\sqrt{3}P_o}{V_s} \sin \omega_LT$$  \hspace{1cm} (12)

where $i_{Lm1,\text{avg}}$ is the average current of the inductor $L_{m1}$ and $P_o$ is the output power.

To simplify the analysis, the currents $i_D$ and $i_{LD}$ are defined as

$$i_D = i_{Do} + i_{De}$$  \hspace{1cm} (13)

$$i_{LD} = i_{Lm2} + i_D$$  \hspace{1cm} (14)

and the average current $i_{Lm1,\text{avg}}$ and the freewheeling current $i_{fw}$ are considered constant in one switching period $T_s$. From Fig. 3, the average currents $i_{Lm1,\text{avg}}$ and $i_{LD,\text{avg}}$ are related by the following equations:

$$i_{Lm1,\text{avg}} - i_{LD,\text{avg}} = 2i_{fw}$$  \hspace{1cm} (15)

and the peak switch current $i_{S,\text{peak}}$ in one switching period $T_s$ is represented as follows:

$$i_{S,\text{peak}} = i_{Lm1,\text{avg}} + i_{LD,\text{avg}} + 0.5(Ai_{Lm1,\text{avg}} + Ai_{LD,\text{avg}})$$  \hspace{1cm} (16)

where

$$Ai_{Lm1,\text{avg}} = \frac{DT_sV_o}{L_{m1}}$$  \hspace{1cm} (17)

$$Ai_{LD,\text{avg}} = \frac{L_{m1}}{L_{m2}}Ai_{Lm1,\text{avg}}$$  \hspace{1cm} (18)

To satisfy the charge balance on $C_p$ in one switching period $T_s$, there is a freewheeling current $i_{fw}$ with different signs according to the duty ratio $D$. Then, the charge balance on $C_p$ in one switching period $T_s$ is expressed as follows:

$$(i_{LD,\text{avg}} - i_{fw})DT_s = (i_{Lm1,\text{avg}} + i_{fw})(1 - D)T_s$$  \hspace{1cm} (19)

From (15), the freewheeling current $i_{fw}$ can be represented as follows:

$$i_{fw} = \frac{2D - 1}{2D + 1}i_{Lm1,\text{avg}}$$  \hspace{1cm} (20)

As shown in Fig. 3, the output diode $D_o$ is turned off before the switch $S_p$ is turned on and the output diode $D_o$ has no reverse-recovery loss. For zero-current turn-off of the output diode $D_o$, the minimum decreasing rate (5) of the output diode current $i_{Do}$ in mode 3 should be satisfied as

$$V_o \left(1 + \frac{1}{L_{m1}} + \frac{N - 1}{L_k}\right) > \frac{i_{D,\text{peak}}}{(1 - D)T_s}$$  \hspace{1cm} (21)

Since the peak switch current $i_{S,\text{peak}}$ is the same as the peak current $i_{D,\text{peak}}$ in one switching period $T_s$, the current $i_{D,\text{peak}}$ can be obtained from (16)–(18) as follows:

$$i_{D,\text{peak}} = i_{Lm1,\text{avg}} \left(\frac{4}{2D + 1}\right) + V_o(1 - D)T_s \left(\frac{1}{L_{m1}} + \frac{1}{L_{m2}}\right)$$  \hspace{1cm} (22)
4 Design considerations

This Section presents the design guidelines and the control strategies of the proposed converter according to the theoretical analysis. The specifications of the prototype converter are:

\[
\begin{align*}
V_o &= 330 \text{ V} & V_s &= 60 \text{ Hz} / 90-265 \text{ V} \\
P_{\text{max}} &= 300 \text{ W} & f_s &= 100 \text{ kHz}
\end{align*}
\]

4.1 Power stage design

From (21) and (22), the zero-current turn-off condition for the diode \(D_o\) is

\[
N - 1 \frac{L_{lk}}{V_o} > \frac{4P_o f_s (V_o + v_i)^2}{V_o (3V_o + v_i)} - \frac{V_o}{2} \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right)
\]  

(23)

This relation gives a guideline for selecting the turns ratio \(N\) as follows:

\[
N > 1 + \frac{4f_s L_{lk} k(k + \sqrt{2} \sin \omega t_1)^2}{R_o (3k + \sqrt{2} \sin \omega t_1)} - \frac{V_o L_{lk}}{2} \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right)
\]

(24)

where \(R_o\) is the output resistance and \(k\) is given by

\[
k = \frac{V_o}{V_s}
\]

(25)

According to (2), the voltage stress of the diode \(D_o\) is increased by the turns ratio \(N\) of the coupled inductor \(L_2\). Thus, the coupled inductor \(L_2\) should be designed with the minimum turns ratio satisfying (24). Also, the leakage inductance \(L_{lk}\) of the coupled inductor should be considered to control the reverse-recovery current of the diode \(D_o\). For current silicon diodes, the preferred \(di/dt\) of the diode turn-off rate is less than 100 A/\(\mu\)s [13]. According to (9), the \(di/dt\) of the diode during its turn-off is roughly determined by \(V_o/L_{lk}\) when \(N\) is close to one. Since the output voltage is 330 V for the proposed SEPIC converter with universal input voltage, a leakage inductance of about 5–10 \(\mu\)H is sufficient to achieve the desired improvement.

In the construction of the coupled inductor \(L_2\), the spacing between the primary and secondary windings of the coupled inductor can be physically adjusted, thus resulting in a sufficient leakage inductance. As an example, Fig. 5 shows the relationship between the turns ratio \(N\) and the line variation for a fixed value of the leakage inductance \(L_{lk}\) under the universal input voltage (90-265 V). From Fig. 5, for zero-current turn-off of the output diode \(D_o\), the turns ratio \(N\) is selected as 1.06 with the leakage inductance \(L_{lk}\) at the line peak of 90 V input voltage. To obtain the desired leakage inductance of the coupled inductor of approximately 8 \(\mu\)H, the coupled inductor was implemented on a PC40 EER4242 core using 37 turns for primary and 39 turns for secondary windings with 1.0 mm airgap, resulting in a magnetising inductance \(L_{m2}\) of 370 \(\mu\)H. The magnetising inductance \(L_{m1}\) was chosen as 370 \(\mu\)H for a single design.

Since the voltage across the capacitor \(C_p\) follows the input voltage within a line period and is considered constant in one switching period, the capacitance of \(C_p\) has a significant influence in the input current waveform. The resonant frequency \(f_r\) of \(C_p\), \(L_{m1}\), and \(L_{m2}\) should be much greater than the line frequency \(f_s\) to avoid input current oscillations at every line half cycle. Also, the resonant frequency \(f_r\) should be lower than the switching frequency \(f_s\) to assure the capacitor voltage constant in a switching period. A good initial approximation for \(C_p\) is given by [6]

\[
C_p = \frac{1}{(2\pi f_s)^2 (L_{m1} + L_{m2})}
\]

(26)

where

\[
f_s < f_r < f_L
\]

(27)

Considering a resonant frequency \(f_r\) of 5800 Hz, the capacitance of \(C_p\) is determined as

\[
C_p = \frac{1}{(2\pi (5800))^2 \times 0.740 \times 10^{-3}} \approx 1.018 \mu F
\]

(28)

Thus, the capacitance of \(C_p\) was chosen to be 1.0 \(\mu\)F.

Table 1 gives the voltage and current stresses on the circuit components of the proposed converter. The maximum voltage stress on the switch \(S_o\) is \(V_r + V_o\) and is approximately 700 V. The peak current stress on the switch \(S_o\) which occurs at full load and minimum input voltage, is approximately 7.8 A. Therefore, an SPP11N80C3

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**Fig. 5** Turns ratio for different values of \(k\) under universal input voltage

\[V_o = 330 \text{ V}; \ R_o = 360 \Omega; \ f_s = 100 \text{ kHz} \]

\[L_{m1} = 370 \mu\text{H}; \ L_{m2} = 370 \mu\text{H}; \ L_{lk} = 8 \mu\text{H} \]
Table 1: Voltage and current stresses of components in proposed converter

<table>
<thead>
<tr>
<th>Component</th>
<th>Voltage stress (V&lt;sub&gt;max&lt;/sub&gt;)</th>
<th>Current stress (I&lt;sub&gt;max&lt;/sub&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch S&lt;sub&gt;p&lt;/sub&gt;</td>
<td>V&lt;sub&gt;i&lt;/sub&gt; + V&lt;sub&gt;o&lt;/sub&gt;</td>
<td>2i&lt;sub&gt;l,m1,avg&lt;/sub&gt; - 2i&lt;sub&gt;l,w&lt;/sub&gt; + \frac{V_{DTs}}{2} \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right)</td>
</tr>
<tr>
<td>Diode D&lt;sub&gt;o&lt;/sub&gt;</td>
<td>V&lt;sub&gt;i&lt;/sub&gt; + V&lt;sub&gt;o&lt;/sub&gt;</td>
<td>2i&lt;sub&gt;l,m1,avg&lt;/sub&gt; - 2i&lt;sub&gt;l,w&lt;/sub&gt; + \frac{V_{DTs}}{2} \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right)</td>
</tr>
<tr>
<td>Diode D&lt;sub&gt;a&lt;/sub&gt;</td>
<td>NV&lt;sub&gt;i&lt;/sub&gt; + V&lt;sub&gt;o&lt;/sub&gt;</td>
<td>\frac{V_{DTs}}{2} \left( \frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right) \left( 1 + \frac{1}{N} - \frac{1}{L_{m1}} - \frac{1}{L_{m2}} \right)</td>
</tr>
<tr>
<td>Inductor L&lt;sub&gt;m1&lt;/sub&gt;</td>
<td>V&lt;sub&gt;o&lt;/sub&gt; (boost mode)</td>
<td>i&lt;sub&gt;l,m1,avg&lt;/sub&gt; + \frac{V_{DTs}}{2L_{m1}}</td>
</tr>
<tr>
<td>Inductor L&lt;sub&gt;m2&lt;/sub&gt;</td>
<td>V&lt;sub&gt;o&lt;/sub&gt; (boost mode)</td>
<td>i&lt;sub&gt;l,m1,avg&lt;/sub&gt; - 2i&lt;sub&gt;l,w&lt;/sub&gt; + \frac{V_{DTs}}{2L_{m2}}</td>
</tr>
<tr>
<td>Capacitor C&lt;sub&gt;p&lt;/sub&gt;</td>
<td>V&lt;sub&gt;i&lt;/sub&gt;</td>
<td>i&lt;sub&gt;l,m1,avg&lt;/sub&gt; + \frac{V_{DTs}}{2L_{m1}}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>i&lt;sub&gt;l,m1,avg&lt;/sub&gt; - 2i&lt;sub&gt;l,w&lt;/sub&gt; + \frac{V_{DTs}}{2L_{m2}}</td>
</tr>
</tbody>
</table>

\[ V_{DS} = 800 \text{ V}, \quad R_{DS} = 0.45 \Omega, \quad i_D = 10 \text{ A} \] from Infineon was used for the switch S<sub>p</sub>. For the diodes D<sub>o</sub> and D<sub>a</sub>, the maximum voltage stresses are 700 and 730 V, and the peak current stresses are 7.8 and 6.7 A, respectively. The output diode D<sub>i</sub> should have higher current rating than the diode D<sub>o</sub> has, since the RMS value of the output diode current i<sub>D,i</sub> is increased compared with that of the diode current i<sub>D,o</sub>. As a fast-recovery diode, an FFAF10U120DN (V<sub>RRM</sub> = 1200 V, I<sub>F,AVM</sub> = 10 A) from Fairchild was used for the diode D<sub>i</sub>, and an FFAF20U120DN (V<sub>RRM</sub> = 1200 V, I<sub>F,AVM</sub> = 20 A) from Fairchild was used for the diode D<sub>a</sub>.

**4.2 Control strategies**

The average current mode is used as the control reference for the proposed SEPIC converter. The proposed converter is designed to operate in CCM, employing UC3854 as the controller, which prescribes the shape and the frequency of the input current owing to its inherently synchronous feedback loop [14]. To obtain almost unity power factor, the synchronous signal is sensed from a rectified sinusoidal waveform at the output of the full-bridge diode rectifier. A current sense resistor is used for detecting the inductor current. The reference current is then generated by a multiplier/divider combination of the synchronous feedback loop, output voltage feedback loop, and input voltage feed forward loop. As already shown in [15], the voltage feedback loop should have a very low bandwidth, well below the line frequency, in order to minimise input current distortion.

**5 Experimental results**

The hardware circuit of the proposed SEPIC converter shown in Fig. 1 was implemented to verify the performance of the proposed converter. It was tested under the universal input voltage range (60 Hz/90-265 V) with switching frequency f<sub>s</sub> = 100 kHz for the maximum output power of P<sub>max</sub> = 300 W (R<sub>o, max</sub> = 360Ω).

Experimental waveforms of the input voltage v<sub>i</sub> and the input current i<sub>i</sub> are shown in Fig. 6. It is shown that the proposed converter provides high power factor at 90 V input voltage in Fig. 6a and at 180 V input voltage in Fig. 6b for full load. Figure 7a shows the experimental waveforms of the inductor currents i<sub>l,m1</sub>, the diode currents i<sub>D,o</sub> and i<sub>D,a</sub>, and the diode voltage v<sub>D,i</sub> at 90 V input voltage. Since the output voltage is higher than the input voltage, the converter operates in the boost mode. It can be seen that the diode current i<sub>D,i</sub> is transferred to the diode D<sub>i</sub> and the output diode D<sub>a</sub> is turned off without the reverse-recovery process. Figure 7b compares the detailed waveform of the output diode current i<sub>D,o</sub> of a conventional hard switching SEPIC converter and that of the diode current i<sub>D,a</sub> of the proposed SEPIC converter at 90 V input voltage for the

![Image](image-url)
same output power level. With the leakage inductor \( L_{lk} \), the turn-off rate of the diode current \( i_{Ds} \) is limited to approximately 25 A/\( \mu \)s in the proposed SEPIC converter. It can be seen that the reverse-recovery current of the diode \( D_s \) is significantly reduced by the leakage inductor \( L_{lk} \), compared to the reverse-recovery current of the output diode in the conventional hard switching SEPIC converter.

Figures 8a and b show the voltage and current waveforms of the switch \( S_p \) in the conventional hard switching SEPIC converter and in the proposed converter at 90 V input voltage. Comparing Figs. 8a and b, the switch turn-on current spike is eliminated and switching loss is reduced when the switch is turned on in the proposed converter. The voltage stress on \( S_p \) is clamped to \( V_i + V_o \) and is approximately 480 V without any increased voltage stress like the conventional SEPIC converter. Figure 9 shows the transient responses of the proposed SEPIC converter at start-up and for load and input voltage variations. Figure 9a shows a startup procedure for 200 W output power at 90 V input voltage. The input current and the output voltage increase linearly with soft-start operation at startup procedure. Figure 9b shows the dynamic behaviour of the converter at a load change from 150 to 300 W at 90 V input voltage. After three mains voltage cycles, the input current reaches its new static value again with a short overshoot in the beginning. Figure 9c shows the behaviour at a load change from 300 to 150 W. The converter reaches its new static operation point after a few mains cycle without current overshoot. Figure 9d shows the behaviour at an input voltage reduction from 180 to 110 V for 200 W output power. The input current changes its operating point according to the input voltage variations and the output voltage is regulated at 330 V with the control circuit implemented by UC3854.

Figure 10a shows the measured power factor and power efficiency as a function of load at 90 V input voltage. The
The power factor of the proposed SEPIC converter is almost unity for full load at 90 V input voltage. A power efficiency of 91.5% is measured for full load at 90 V input voltage. The proposed SEPIC converter improves the power efficiency by 2.8%, which translates into approximately 24% reduction of the losses compared with the conventional hard switching SEPIC converter at 90 V input voltage. Figure 10 shows the measured power factor and power efficiency with relation to the input voltage at full load. The proposed SEPIC converter achieves high power factor for full load in the universal input voltage range (90–265 V). The efficiency improvement is prominent at the minimum input voltage where the reverse-recovery loss is the most significant. Figure 11 shows the measured current harmonics of the proposed converter compared with the current harmonic limits of IEC 61000-3-2 Class-D at 90 V input voltage. The proposed SEPIC converter complies with IEC 61000-3-2 Class-D limits and improves by 2.8% power efficiency compared with the hard-switching SEPIC converter at 90 V input voltage.

6 Conclusions

A CCM SEPIC converter with low reverse-recovery loss has been proposed for PFC. The proposed CCM SEPIC converter has been analysed in detail. The reverse-recovery loss of the diode is reduced by utilising a coupled inductor and an additional diode. Zero-current turn-off of the output diode is achieved using a coupled inductor. The reverse-recovery current of the additional diode is reduced by the leakage inductor of a coupled inductor. The proposed SEPIC converter can improve the power efficiency and does not suffer from voltage and current stresses compared to the conventional PFC converter employing the SEPIC converter. With a simple passive approach, the proposed SEPIC converter reduces the reverse-recovery loss of the diode and achieves high power efficiency. Experimental results on a 300 W prototype of the proposed SEPIC converter have shown high performance such as almost unity power factor and a power efficiency of 91.5% at 90 V input voltage.
7 References


Fig. 10 Measured power factor and power efficiency
a Against load at 90 V input voltage
b Against input voltage at full load