Testing of Analogue Circuits via (Standard) Digital Gates

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Abstract

The possibility of using window comparators for on-chip (and potentially on-line) response evaluation of analogue circuits is investigated. No additional analogue test inputs are required and the additional circuitry can be realised either by means of standard digital gates taken from an available library or by full custom designed gates to obtain an observation window tailored to the application. With this approach, the test overhead can be kept extremely low. Due to the low gate capacitance also the load on the observed nodes is very low. Simulation results for some examples show that 100% of all assumed layout-realistic faults could be detected.

1. Introduction

Out-going quality is one of the key issues in highly reliable applications like automotive, public transportation or aerospace applications. Besides the process quality cost-effective testing is one of the parameters to achieve high quality. The most cost-effective way of testing in terms of test time optimization and also time-to-market is Design-for-Testability (DfT). Today a wide range of DfT techniques exists for digital integrated circuits (IC), but only a few proposals are known for mixed-signal ICs. Since test costs can always be traded off against die area, DfT also becomes interesting for cost sensitive products like consumer or automotive mixed-signal ICs. For those products an interesting test solution which can be easily accommodated in the production test program, consists in checking whether or not certain DC-operating points or signal levels on critical circuit nodes are within their design limits. This check can be performed at different (test) time instances, supply voltage conditions and temperatures. Furthermore, the continuous observation of critical nodes can also be used during the application to achieve on-line self-checking capabilities (similar like for digital ICs) [1] e.g. to flag failures to a control unit in safety-critical applications. This paper deals with a cost-effective method for such an on-chip evaluation/observation of signal levels. It only requires a digital window comparator that can be area effectively implemented by merely digital logic gates.

2. Previous work

In order to check the correctness of analogue voltages at (selected) nodes to be observed, analogue comparators have been proposed and a few are briefly summarised. In [2] a strobed comparator with a variable threshold is described, that can be used as a waveform digitizer. This solution, however, demands high requirements in terms of bandwidth and clock skew/jitter. Another, very specific application of on-chip analogue differential comparator [3] is used to measure the dynamic performance of the differential sense amplifier of SRAMs and to compare it with an externally applied differential signal. A bias-programmable, clocked two-mode comparator with hysteresis for mixed-signal ICs is introduced in [4]. In this approach the analogue comparator is implemented by a functional conversion of system OTAs or operational amplifiers (OpAmp) during test mode [5], in which different thresholds can be programmed via the biasing from the digital part. However, all these solutions require careful analogue design, have significant area occupation and, possibly, need critical reference voltages. Finally, digital window comparators have been already outlined in [6].

Unlike the above proposals, the simple solution proposed here, is based on digital gates that require minimal or no additional silicon area and does not require any reference voltage. Such a solution is of particular interest for mixed-signal ICs, where digital gates are already available from standard libraries. On the other hand, the scheme of this work can also be implemented with dedicated logic gates featuring non-standard logical switching thresholds. Such

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gates can then become part of the standard digital library and thus be reused in other designs.

3. DC Transfer Function of Digital Gates

Digital logic gates are designed such that the logic threshold V_{LT}, i.e. the input voltage at which the output is switching, is between ground and supply voltage (V_{DD}). For CMOS gates V_{LT} depends on the W/L ratio of the NMOS and PMOS transistor. In case of a CMOS inverter the input voltage V_{LT} for which the inverter switches is given by [7]:

$$V_{LT} = \frac{V_{DD} + V_{thp} + \sqrt{b} * V_{thn}}{1 + \sqrt{b}} \qquad \text{(Eq. 1)}$$

with V_{thp} and V_{thn} being the threshold voltages for the p and n-transistor, respectively, V_{DD} the supply and β is defined as:

$$b = \frac{K_n * (W_n / L_n)}{K_p * (W_p / L_p)} \qquad \text{(Eq. 2)}$$

In case of V_{thp} = - V_{thn} and β=1 the logical input threshold voltage becomes $V_{DD}/2$ as mentioned above. Depending on β the logic threshold V_{LT} can be moved up and down. Thus, it can be adjusted within some range between ground and the supply V_{DD}. In fig. 1 and fig. 2 this is shown for a CMOS-inverter.
In this example a standard 3.3V CMOS inverter has been used with $L=L_n=L_p$= 0.5µm, W_n=1µm and W_p=2.9µm. To see the impact on the logical threshold, W_n was varied from 0.5µm to 5µm in steps of 0.5µm. The length L was kept constant for both transistors (Fig. 1). As can be seen V_{LT} ranges between 1.3V and 1.8V, i.e. by 500mV. If the W of the PMOS transistor is varied and the W of the NMOS is kept constant the logic threshold V_{LT} varies between 1.15V and 1.6V, i.e. 450mV (Fig. 2).

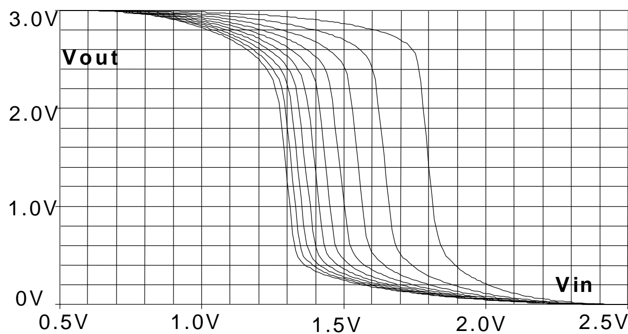

Fig. 1 Variation of W in steps of 0,5µm from W=0.5µm – 5µm and L=0.5µm for the NMOS of an Inverter in 0,5µm Mietec CMOS technology

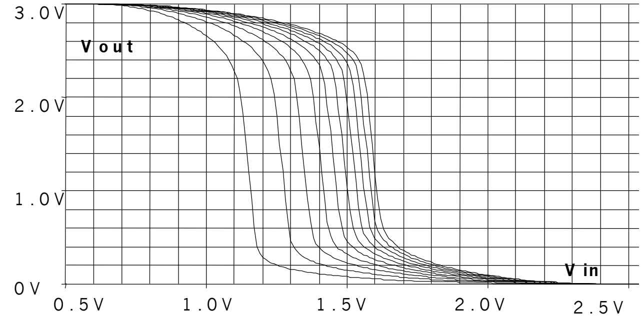

Fig. 2 Variation of W in steps of 0,5µm from W=0.5µm – 5µm and L=0.5µm for the PMOS of an Inverter in 0,5µm Mietec CMOS technology.

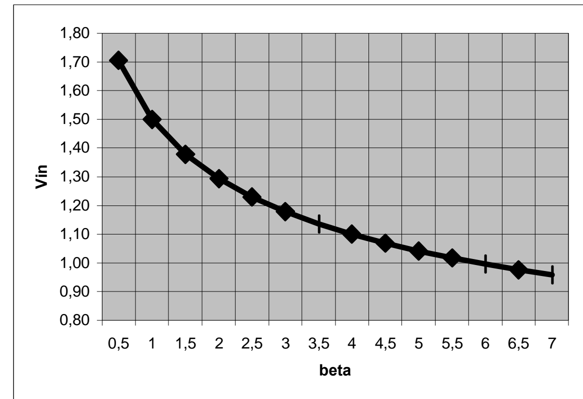

Fig. 3 Logical threshold $V_{in} = V_{LT}$ vs β = 0,5 ..7 according eq. 1

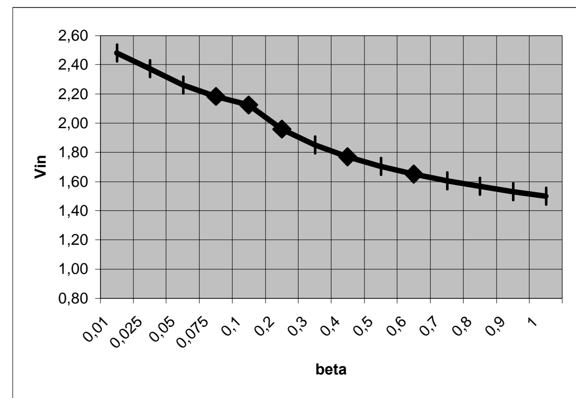

Fig. 4 Logical threshold $V_{in} = V_{LT}$ vs β = 0,01 ...1 according eq. 1

Another way to achieve different V_{LT} with standard gates is the use of more complex logic gates than just simple inverters with special (W/L)-ratios. If both inputs of a 2-input NAND or a 2-input NOR are connected together their transfer function is that of an inverter and, thus, the logical threshold $V_{LT} = V_{DD}/2$ for β=1.
If however one input of the NAND is connected to $V_{DD,}$ the logical threshold is decreased since the β > 1. The

opposite is true for a NOR. If one input of the NOR is connected to GND, the logical threshold is increased due to $\beta < 1$. In tab. 1 the different β values for a x-input NAND and x-input NOR are summarised.

Table 1 gives the β's for NANDs and NORs with two to six inputs. Furthermore, the β's are summarised for different numbers of inputs connected together as signal input whereas the remaining inputs are connected to V_{DD} in case of a NAND and to GND in case of a NOR, respectively. If all inputs are connected together and used as signal input, $\beta = 1$ for either type of gates.

For the NANDs each of the parallel PMOS transistors has the same gate length L_p and gate width W_p'. Thus, a possible "equivalent" inverter can be constructed considering all the pull-up transistors together realizing a single PMOS transistor having as gate width, the total gate width $W_p = n \times W_p$'.

For the NMOS transistors of the NANDs, the gate width W_n is equal and the gate length is L_n'. Thus the gate lenght of the "equivalent" NMOS will be given by the total gate length of the pull-down NMOS transistors which are in series, i.e: $L_n = n \times L_n$'. For the ratio $k_n/k_p = 3$ was assumed (cf. Eq. 2). Accordingly the same is valid for the NOR.

As can be seen from tab. 1 in case of the NAND the β can be increased while for the NOR the β can be decreased. Consequently the V_{LT} for the NANDs is decreased and increased for the NORs. In fig. 3 and fig. 4 the logical threshold voltage $V_{in} = V_{LT}$ are depicted versus different sweeps of β's. While fig. 3 depicts the behaviour for a NAND, fig. 4 shows the curve for a NOR each with different number of signal inputs. Note, that the logical threshold is shown for typical technology parameter.

Tab. 1: Different β for a NANDs and NORs with two to six inputs and different number of inputs connected to V_{DD} or GND.

NAND	Inputs connected together											
beta	1	2	3	4	5	inputs	Wn	Ln	Ln'	Wp	Wp'	Lp
1,00	12,00					2	2	2	1	3	1,5	1
1,00	27,00	6,75				3	3	3	1	3	1	1
1,00	48,00	12,00	5,33			4	4	4	1	3	0,75	1
1,00	75,00	18,75	8,33	4,69		5	5	5	1	3	0,6	1
1,00	108,00	27,00	12,00	6,75	4,32	6	6	6	1	3	0,5	1
NOR							Wn	Wn'	Ln	Wp	Lp'	Lp
1,00	0,25					2	1	0,5	1	6	1	2
1,00	0,11	0,44				3	1,5	0,5	1	13,5	1	3
1,00	0,06	0,25	0,56			4	2	0,5	1	24	1	4
1,00	0,04	0,16	0,36	0,64		5	2,5	0,5	1	37,5	1	5
1,00	0,03	0,11	0,25	0,44	0,69	6	3	0,5	1	54	1	6

Based upon this property of moving the logical threshold V_{LT} a simple digital window comparator can be implemented as described in the following paragraph.

4. Digital Window Comparator

Based on the fact that the logical threshold V_{LT} of NANDs and NORs can be shifted in opposite directions, this allows a simple implementation of a digital window comparator. In its simplest form only one 2-input NAND, an inverter and one EXOR are required as depicted in fig. 5. The output of the inverter and the NAND are connected with the EXOR gate. The output of the EXOR is the output of the digital comparator.

One input of the NAND is connected to the supply V_{DD}, whilst the other one is connected to the signal input together with the input of the inverter. Boolean wise this configuration would always yield a "0" independent whether the input is "1" or "0".

If the input signal however is not a digital, but an analogue input signal, an intermediate state can be observed depending on the input level of the signal. The NAND basically operates as an inverter with a decreased logical threshold. As can be retrieved from tab. 1, β=12 applies for the NAND in this case, whereas the β=1 applies for the inverter.

Using equation 1 and 2 yields a logical threshold of 1,28V for the NAND and 1.5V for the inverter. This results in a diffe-rence between the two logical thresholds of about 220mV. In other words, i.e. if an input signal is slowly ramped up is applied to the signal input (input in fig. 5) of this comparator, the comparator output sequence would be "010".

As long as the signal level is between 1.28V and 1.5V the comparator output is "1", while outside this range or window the comparator is always at "0". Other circuit

The width and centre position of the detection window, i.e. the signal level range where the EXOR output is "1", is the essential design parameter.

It can be adjusted by the choice of gates in terms of number of inputs and type as well as by the number of inputs that are actually connected to the signal input.

In fig. 6 the simulation results for a comparator comprising of a NAND and a NOR are depicted.

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architectures and/or gate combinations could also be used. As can be seen depending on the complexity of the gates a comparator with different sizes for the window can be realised.

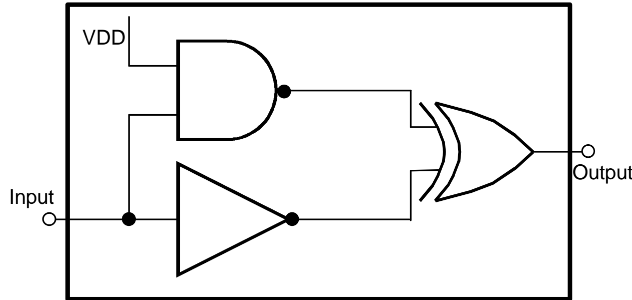

Fig. 5 Digital window comparator using an inverter and a NAND

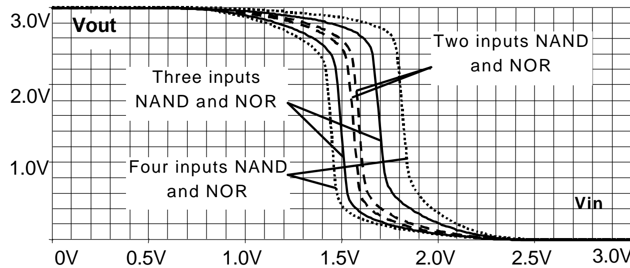

Fig. 6 Comparator realized by a NAND and a NOR with two, three and four inputs.

5. Design-for-Testability Scheme

The previously described digital window comparator can be integrated into an overall Design-for-Testability scheme. Within this scheme it can be used to check whether or not a DC level of a circuit node in the analogue part of a mixed-signal circuit is within a certain range. The width of the window should be chosen such, that a) the typical DC level is centred with this window and that b) it covers e.g. a 6-σ variation of the DC level to be checked. Due to the very low effort to implement such comparators in a mixed-signal circuit, the chip size may be not or only very marginally impacted. However, the comparator must not be completely implemented in the digital part of the mixed-signal circuit as one may assume at the first glance. Since the comparator is logically equal to a constant logical “0”, the synthesis tool for the generation of the digital part would replace the comparator by “0” signal and the comparator function would be lost. Another practical consideration emanates from the current consumption of the chip. If the input signal falls into the window of the comparator, both the PMOS and the NMOS transistors are conducting and a constant DC current would be drawn from the supply. This has to be taken into account and might require to connect the gates to the power down line of the circuit. In particular this will be mandatory if the gates are connected to the digital supply. Otherwise the Iddq test will jeopardised. The node which is checked is only loaded by the low capacity of some gates which is typically in the range of some fF. Since except for the capacitive loading of the gates no current is flowing, the wiring can be at minimal width and no voltage drop is involved. Thus, for the DC level check there is no voltage drop over the metal line from the analogue circuit node to the input of the digital window comparator in the digital part. This allows to use the minimal line width for the wiring and thus causes less area consumption. If a scan path has been implemented in the circuit, the window comparator can be connected with the scan path via an additional flip-flop or via a digital multiplexer to avoid the additional flip-flop.

6. Experimental Results

In this paragraph some experimental investigation results are presented. Up to now it was assumed that no variation occurs in the threshold levels, i.e. all parameters of the transistors are typical. This, however is not true.

Lot-to-lot variations have to be taken into account, as well as the variation due to the temperature for which the circuit has to be operational. The temperature impact is only of importance if the window comparator is also used during the field application. If it is only used during the production test the comparator has to work under ambient temperature regime. In fig. 7 the temperature impact on the characteristic of window comparator was simulated.

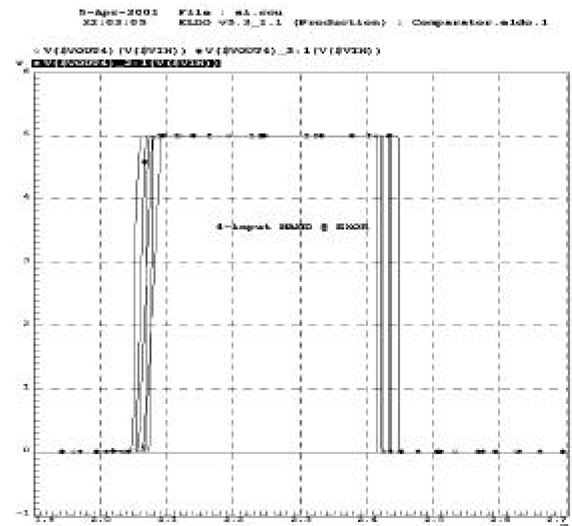

Fig. 7 Four input NAND/NOR window comparator at typical parameters and a temperature variation T: -50 °C – +150 °C

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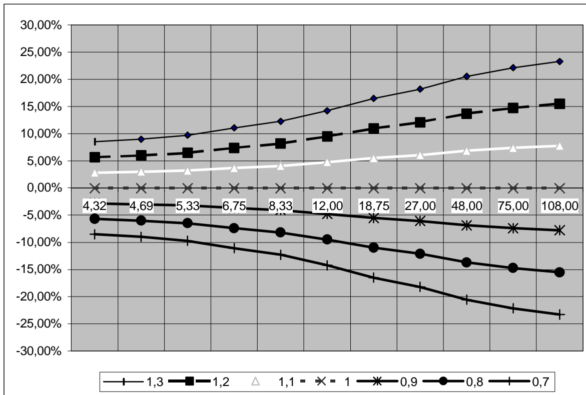

Fig. 8 Relative error of the logical threshold for NANDs as function of their βs for +/- 10%, +/- 20% and +/- 30% deviation of the gate threshold voltage (Note: gate threshold deviations are in opposite directions)

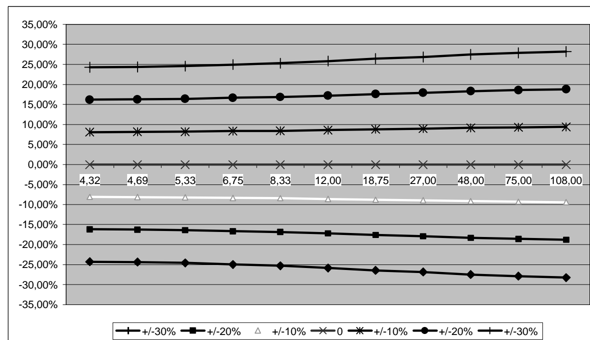

Fig. 9 Relative error of the logical threshold for NANDs as function of their βs for +/- 10%, +/- 20% and +/- 30% deviation of the gate threshold voltage (Note: gate threshold deviations are in same directions)

In this case a 4-input NAND and an inverter in a 0,5µm CMOS technology were used to implement the comparator. The temperature range between –50 °C and +150 °C is the typical temperature span used for the characterisation of automotive applications. In order to obtain a window a triangle signal between zero and supply was applied as input signal. The centre of the window is around 2.25V and the temperature dependent variation of the logical thresholds is about 30mV in both case, ie. When ramping up and ramping down the input signal. The width of the window is about 350mV. As can be seen from this simulation, the temperature impact on the position of the window as well as on the width of the window is not too significant and the switching at cold is just faster than at hot.

Beside the temperature impact, lot-to-lot variation has to be considered. This parameter variation normally does not significantly impact the function of digital logic, but the speed performance. Parameters impacted by lot-to-lot variations are the mobility µ and the gate threshold voltage due to variations in the implant. The variation due to gradiants in the thickness of the gate oxide can be neglected at least across the same die. In fig. 8 the impact of the gate threshold voltage variation for the NANDs from tab. 1 are depicted. In this investigation it was assumed that the gate threshold voltages of the PMOS and the NMOS are moving in opposite directions, i.e. V_{thn} is increased by x% while V_{thp} is decreased by x%.

As can be seen, the lowest relative error is obtained for NANDs where only one input for 2-input NANDs or maximum two inputs are connected to the supply for NANDs with more than two inputs. In this case the error for a 10% variation of the gate threshold is between 2,5% - 5%. Of course the larger the gate threshold variation the larger is the error. As a general rule it can be stated, that too large βs should be avoided if possible.

A different result is obtained if the lot-to-lot variation of the gate thresold of the P- and NMOS transistors are assumed to be in the same direction, i.e. V_{thn} and V_{thp} are either increased by x%.

In fig. 9 the relative errors for the same amount of variations for the gate thresholds are depicted. In this case the relative error is almost constant and always higher than under the previous condition. However, also here lower βs are yielding slightly better results. Unlike in the previous case the variation of β has a much more significant impact. Of course one may question whether or not this assumption is realistic for a well controlled technology.

The same investigations were performed for the NORs again from as summarised in tab. 1.

The results are depicted in fig. 10 and fig. 11. Also here the previous statement is valid: The lowest relative errors are achieved for NORs with only one input connected to ground or for not more than two inputs in case of NORs with more than two inputs. Again this investigation was performed under the assumption that the gate threshold voltages move in opposite directions for the PMOS and NMOS, respectively.

Like in the case of the NAND also for the NOR gates the case of gate threshold variation in the same direction have been investigated. Again the relative error curves are flat and higher than in case of opposite directions of gate threshold variations.

As can be seen in fig. 11 the relative error observed are slightly higher than in case of the NAND gates but show the same trend.

Beside the gate threshold variation also the mobility of the PMOS and NMOS can change. As long as this variation impacts the mobility in the same direction, i.e. both mobilities are increased or decreased by the same amount, the β is constant and not effect on the logical threshold is observed. If, however, the mobilities are opposite, i.e. one increased while the other decreases, than the β either

increases or decreases and the effect can be directly seen from the graphs in fig. 3 and 4.

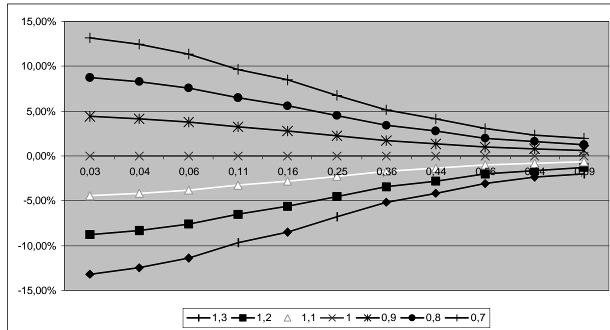

Fig. 10 Relative error of the logical threshold for NORs as function of their βs for +/- 10%, +/- 20% and +/- 30% deviation of the gate threshold voltage (Note: gate threshold deviations are in opposite directions)

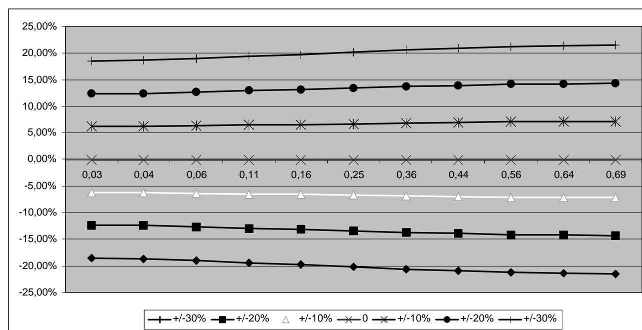

Fig. 11 Relative error of the logical threshold for NORs as function of their βs for +/- 10%, +/- 20% and +/- 30% deviation of the gate threshold voltage (Note: gate threshold deviations are in same directions)

As described before, several parameters impact the position and width of the comparator window. In the following a window comparator comprising of a 2-input NAND with one input connected to the supply and a 2-input NOR with one input connected to ground and the EXOR. This comparator was characterised over temperature and parameters variations using the four different corners:

- NMOS fast PMOS fast
- NMOS fast PMOS slow
- NMOS slow PMOS fast
- NMOS slow PMOS slow
- NMOS typical PMOS typical

Two temperatures were simulated: -50 °C and +150 °C. The characterisation result is depicted in fig, 12 in the above mentioned order. As can be seen from this simulation the impact of the temperature is of less importance and narrows the window. The impact of the parameters variations however, is of much more importance. The most critical parameters constellations are the fast-fast and slow-slow combinations. Here the windows exhibit a common overlap range of 300mV ranging from 2,2V – 2,5V. The combination fast-slow and slow-fast are in general considered to be too pessimistic. However, it is important to note, that in those cases the window position is moved out of the common overlap region. Note, that the width of the window itself, however, is not significantly effected. Wether or not this causes a problem for the particular application, can only be decided after the characterisation of the whole circuit, including the circuit under test (CUT). Another way of solving this problem is the use of another combination of gates and number of inputs as mentioned above or the modification of the comparator circuit constellation. Though the fast-slow and slow-fast combination appear to be less significant this case is currently under further investigation.

It should also be mentioned that supply level shifts have also to be considered (power-supply rejection). Furthermore, this approach is limited by the supply for the digital gates which can be typically 5V or 3.3V if the digital supply is used. This might be lower than the actual analogue signal level. If the level is outside the adjustable threshold range the digital can be supplied by the higher analogue supply. Since the digital gates are anyway not placed inside the digital part of the mixed-signal circuit, this can resolve this limitation. Otherwise additional level shifters could be used. However, this solution should not be of primarily preference.

In order to investigate the performance of the proposed solution, a test circuit configuration has been used as described in [5]. It comprised of a simple Miller OpAmp [8] used as CUT. The window comparator was formed by an inverter and a 2-input NAND. For this configuration fault simulations have been performed, assuming only faults in the CUT, i.e. in the OpAmp.

For the selection of the assumed faults, the layout-based fault extraction technique (L^2RFM) [9] has been applied to derive layout-realistic faults. Those included poly- and metal-shorts, cracks (opens) in the metal and poly structures as well as pin-holes in the thin (gate and capacitor) oxides. Also variations of the absolute value of the Miller capacitance were considered. Due to those assumed defects different failure modes are caused which can either be described by catastrophic and parametric faults. The following layout-realistic faults have been considered: shorts between gate-drain, gate-source, drain-source, gate-channel, pin-holes and poly-poly shorts on the compensation capacitance (Miller OpAmp), as well as drain, source and gate opens.

The simulations have been performed with SPICE. For the modeling of the faults the so-called "Resistor Fault Simulation Model" (R-fsm) has been used. For a short

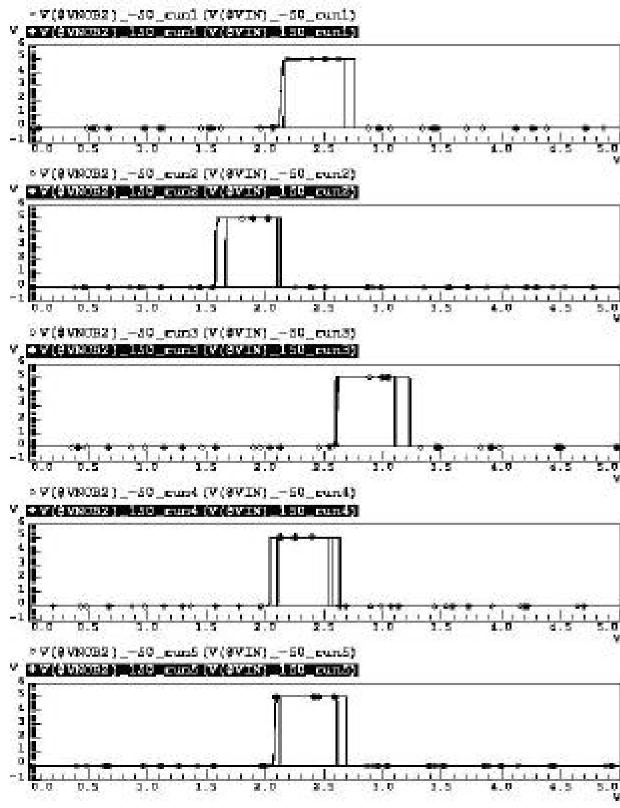

Fig. 12 Characterization of a 2-input NAND/NOR window comparator a) NMOS fast, PMOS fast, b) NMOS fast, PMOS slow, c) NMOS slow PMOS fast, d) NMOS slow PMOS slow and e) NMOS typical PMOS typical

fault a resistor value of .01Ω has been applied whilst for the open fault a resistor value of 10 GΩ was used. For the pin-hole, a simple resistor model between the gate and substrate was used with the resistance changing between of 1MΩ and 10kΩ. For the compensation capacitance a possible pin-hole was considered and the fault was modeled using a capacitor of 1pF (Miller capacitance) in parallel with a resistor with values changing between 1MΩ until 10kΩ.

Within the course of L^2RFM the layout implementation of wide transistors was taken in account for the fault simulation. Figure 13 shows an example (M5). In layout this transistor is implemented as five parallel transistors (M5/1 – M5/5) of the same size. This results in the same channel length and width, however, each equal to only 1/5 of the width of the original transistor width M5. For the fault assumption the common gate is of particular importance, as in layout it is a single straight poly-line. Moreover, the “gates” are only connected on one side (e.g. the left side) to the circuit. Figure 13 depicts where the open faults were considered. In fact the gate opens are considered as a poly-line crack moving along from the left to the right. Only one gate open at a time was assumed as this is the more difficult fault situation. For shorts, no fault were assumed realistic between gate-drain and gate-source for transistors with a width larger than 15µm. As test stimulus the so-called complementary signal (COMPSIG) has been used to drive the CUT to the quiescent state after a defined time [10] at which the test response is then evaluated by the window comparator. Of course also any other test stimulus can be applied, as long as the circuit is in a stationary or quasi-stationary state during test evaluation. In this case the observation window of the comparator was centered around the output offset of the fault-free CUT i.e. at -419mV. The chosen width of the observation window was ± 100 mV. This was sufficient for the fault-free response of the OpAmp assuming a σ = 8.33mV.

From the fault simulations, which are described in more detail in [5], it turned out, that the pin-hole on the Miller compensation capacitance was easily detected. The

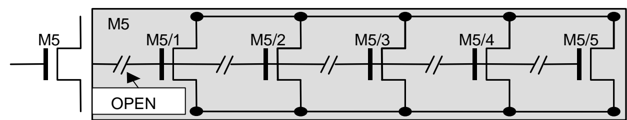

Fig. 13 The fault assumption for the open gate on the transistor M5.

different gate-open constellations on wide transistors resulting in partially floating gate configurations appear like parametric faults. However, all faults could be detected by the digital window comparator. This is an important result since parametric failure behaviors are in general difficult to detect.

7.Conclusion

A simple DfT-technique for mixed-signal ICs is described that uses a window comparator to observe the DC level on analogue circuit nodes. For the implementation of the comparator only a few additional digital standard or dedicated logic gates are required. No references or clock signals are required. Due to this techniques a very low overhead in terms of gates and wiring is caused. Due to the low number of gates, in practice no increase in the silicon area can be assumed. Investigations showed that the impact of the temperature can be neglected, but the lot-to-lot variations have to be considered. If considered realistic in particular the fast-slow and slow-fast combination have to be simulated as the window may move out of the common overlap region. Fault simulations showed, that a good fault coverages.

8. References

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