HAS FPGA TECHNOLOGY PEAKED IN WIDEBAND WIRELESS APPLICATIONS?

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I think it is reasonable to say that field programmable gate arrays (FPGAs) have become a dominant technology for first-stage intermediate frequency (IF) and modem processing in a variety of wideband wireless applications. This is especially true in markets such as military and commercial satellite communications where "reprogrammability" and time-to-market concerns outweigh the costs benefits associated with application-specific integrated circuits (ASICs) in mass production.

The reason for this market dominance is strongly tied to the performance of these devices. For the past several years, both Xilinx® and Altera® have invested heavily in differentiating themselves in the signal processing space through FPGA product families that incorporate hundreds of dedicated digital signal processor (DSP) coprocessing elements, each capable of supporting hundreds of megasamples per second [1, 2]. Conversely, while traditional DSPs and general-purpose processors (GPPs) have always been able to support narrowband signal processing at some level, their ability to support wideband signal processing has been fairly limited to date. For example, a high-end signal processing device capable of two DSP operations per clock provides only 100 operations per sample on a 20 Msample/s baseband signal when operating at 1 GHz. This number of operations per sample is far too low for the complex waveforms and air interface standards associated with the majority of wideband applications.

Looking forward, a key question is whether the dominant position of FPGAs in wideband wireless applications is sustainable. To explore this question, it is first necessary to examine the technology roadmaps for other device families in the context of wideband wireless applications. With this in mind, consider the following:

- Numerous "non-FPGA"-based reconfigurable computing devices have entered the market specifically targeting wideband wireless applications. These devices include the FastMath® processor from Intrinsity®, the PicoArray® from PicoChip®, and the Ivy Cluster™ array from Cogent ChipWare. They typically incorporate multiple signal processing elements in a massively parallel array to provide the processing performance necessary for wideband applications [3–5]. While these technologies are relatively new, and as such have not as yet entered the mainstream, the cost/performance trade-offs associated with them has garnered considerable interest in the wireless community.
- The data rates associated with wideband wireless applications tend to advance at a slower pace than Moore's Law [6]. This effect is illustrated in Fig. 1, which shows typical data rates for narrowband and lower-rate wideband applications mapped against the data rates supported by typical GPP and DSP processing engines. The curves for the latter have been extrapolated based on announced technology roadmaps and assume that market leaders such as Intel® and Texas Instruments® (TI) will continue to follow a Moore's Law curve in the advancement of their processing technology for the foreseeable future. While these curves represent numerous dependencies associated with the complexity of the target wideband application and are therefore somewhat subjective, the overall trend is clear. Over time it is reasonable to assume that GPPs and DSPs will be able to address more and more of the signal processing associated with wideband wireless applications that has been traditionally supported only through reconfigurable computing and ASIC devices.

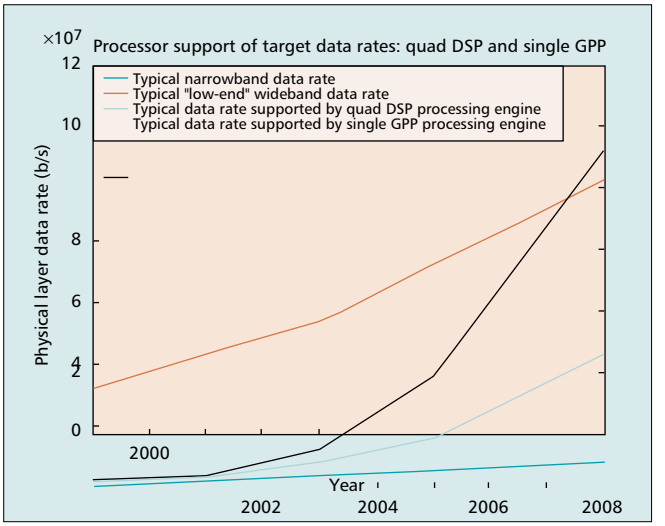

Figure 1. *Applicability of GPP and DSP technology to lower-rate wideband IF and modem processing.*

- GPP devices incorporating wideband vector processors, such as Intel's Xeon® processor, have begun to gain acceptance in the wireless community as mainstream signal processing devices. This is evidenced through the acceptance of the Vanu® software-defined Global System for Mobile Communications (GSM) base station, which utilizes a dual Xeon processing engine as its signal processing subsystem, for interoperability with Nortel Network's® mobile switching centers [7].
- Over the past several years leading DSP chip manufacturers have begun producing chipsets specifically targeting wireless applications based on their core DSP technology. TI, for example, has produced chipsets for wireless terminals and wireless infrastructure targeting an array of commercial cellular waveforms [8, 9]. The signal processing devices associated with these chipsets integrate multiple peripheral elements

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such as RISC processors, analog and digital I/O, and ASIC coprocessors in with the DSP core to provide a cost optimized application-specific solution. For example, TI's TMS320TCI100 device targets Universal Mobile Telecommunications System (UMTS) infrastructure applications with an embedded Viterbi coprocessor capable of supporting 350 voice channels and a turbo coprocessor capable of supporting 28 high-data-rate users [10]. TI is already involved in the definition of ultra-wideband (UWB) standards, and as such, it is reasonable to assume that they will advance their portfolio offering with a UWB application-specific DSP solution in a similar manner [11].

These trends indicate a potential for FPGAs to be replaced as the dominant technology in wideband wireless applications if the selection of FPGA technology were based solely on raw performance. Defining the technology trends for these applications beyond raw performance requires an evaluation of additional selection criteria for each candidate signal processing device [12].

Level of integration: The ability to integrate multiple functional components and peripheral devices into a single package can significantly reduce the size and hardware complexity of the digital transceiver, and will often lead to a lower cost per channel for the overall radio system. For example, both Xilinx and Altera offer soft processing cores for system control and integrated high-speed multigigabit transceivers for interfacing to other elements of the radio architecture. These technologies coupled with the DSP coprocessing elements embedded in these devices allow a single FPGA to act as a complete wideband modem processor, supporting chip rate processing, modulation, demodulation, interleaving, framing, and forward error correction.

Programmability: Programmability defines the ability to reconfigure a device or part of a device to perform a desired set of functions for each of the target air interface standards. ASIC devices, as their name states, are application-specific, and therefore offer only limited programmable features. As such, while an ASIC device may offer the best performance at the lowest cost for a given function, it may not support the flexibility necessary in the wideband radio platform. Furthermore, support for reconfigurability in FPGA devices to date typically requires that the entire FPGA be reprogrammed, whereas partial reconfigurability is natively supported on DSP and GPP devices. Support for partial reconfiguration of FPGAs is achievable, however, and it can be anticipated that this capability will be widely available in the foreseeable future [13].

Development cycle: As devices become more specialized, the development cycle and skill set associated with implementing an algorithm on those devices increases significantly. Thus, in general, it takes less time to implement an algorithm on a GPP than on a DSP, and it takes less time to implement an algorithm on a DSP than on an FPGA. As such, device selection directly impacts time to market and the nonrecurring engineering costs associated with the creation of a wideband radio platform. FPGA and DSP vendors have been working to mitigate this issue through the use of predefined standard processing blocks supporting common wireless application functions, and tools such as System Generator for rapid application development [14].

Power: The power utilization of the device when performing the required function must also be assessed in the devices selection process. ASIC devices are generally optimized to provide outstanding power performance. The power requirements of most programmable devices, however, increase substantially with device utilization and clock rate, and this must be taken into account when evaluating the power budget for the overall design.

A subjective evaluation of these criteria against the roadmaps of FPGA, DSP, and GPP vendors leads me to believe that FPGAs will retain their dominant position for the foreseeable future in IF and modem processing *for the highest-rate wideband applications*, where DSPs and GPPs cannot provide the required level of processing performance. Other reconfigurable computing technologies may gain a leadership position in select market spaces supporting these highest-performance applications based on specific values they bring to those markets. For *lower-rate wideband applications*, however, GPP- and DSP-based solutions will become attractive alternatives to FPGAs, with the cost advantages of GPP-based architectures leading where size, weight, and power do not drive the overall requirements. These devices will typically be supplemented by FPGA processing in the very front end of the radio architecture, providing a synchronous interface between the GPP or DSP and mixed signal processing.

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Biography

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