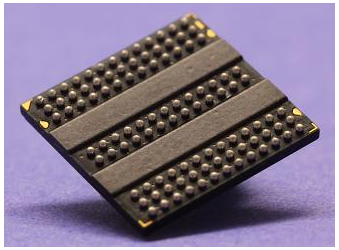
Cost-Minimized Double Die DRAM Packaging for Ultra-High Performance DDR3 and DDR4 Multi-Rank Server DIMMs

R. Crisp[1], B. Gervasi[2], W. Zohni[1], B. Haba[3]



Richard Crisp
Vice President and Chief Technologist
Invensas Corp.
rcrisp@invensas.com
14 March 2012
rcrisp@invensas.com

[1] Invensas Corp.
[2] Discobolus Designs
[3] Tessera Intellectual Properties Corp.

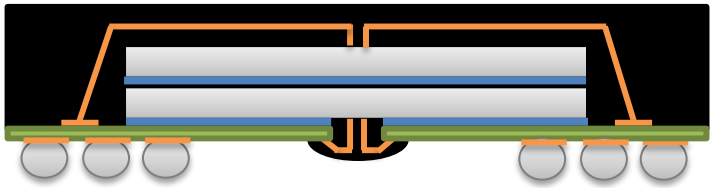
Outline

- Key difficulties with current multi-die DRAM packages
- Newly developed structure
- Comparison of manufacturing process flows
- Device-level measured results
- DIMM PCB Design Comparison
- DIMM in system measured results
- Conclusion

invensas™

Key Difficulties with Dual Die DRAM Package Structures

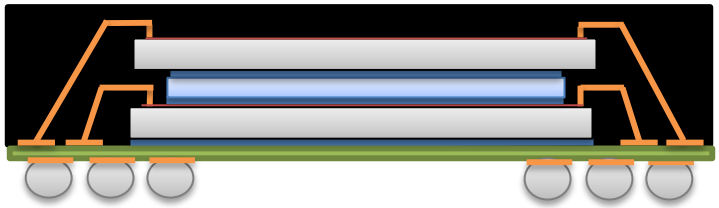
Dominated by Gold Cost



Opposing-Face DDP

Asymmetric signal and power delivery
Thermal
Thickness
Cost

Dominated by RDL Cost



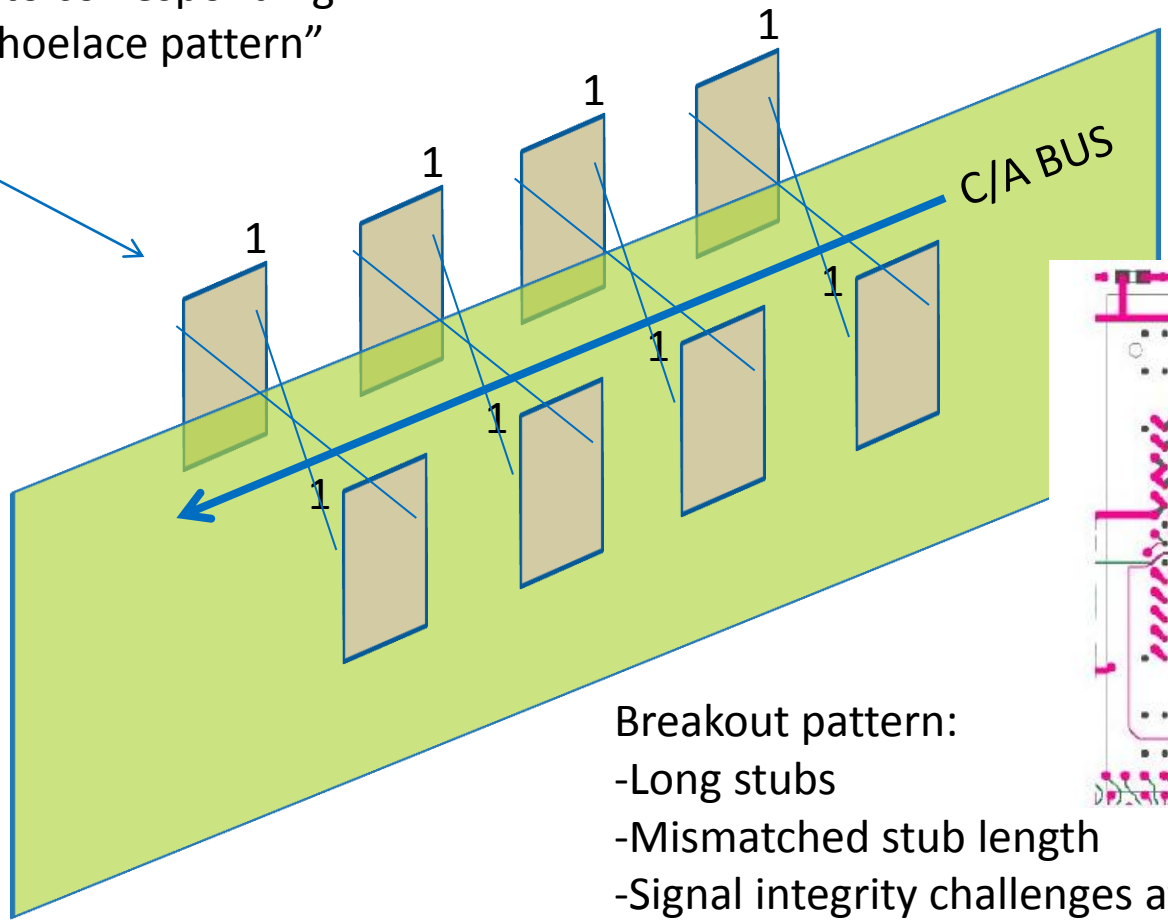
Face-Up DDP with RDL

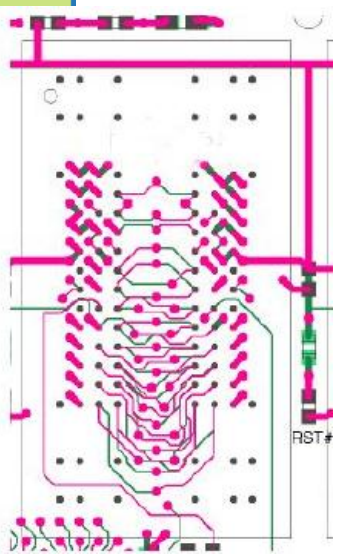
Power and Signal Delivery via RDL
Thermal
Thickness
Cost

invensas™

PCB Layout difficulties with standard DDPs

Must interconnect same-named bussed signal to corresponding leads using “shoelace pattern”

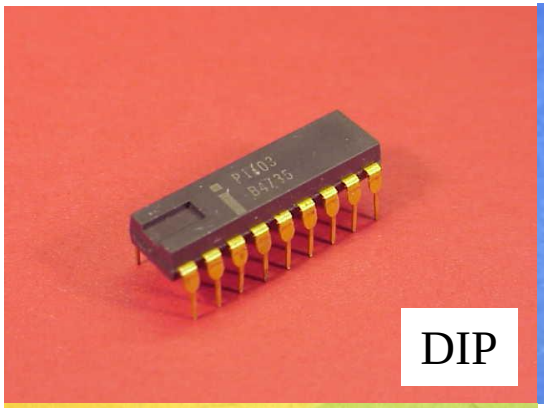




Breakout pattern:
-Long stubs
-Mismatched stub length
-Signal integrity challenges at high frequency

Why do we have the long stubs in the breakout?

- Package evolution / legacy is the best answer


DIP

SOJ

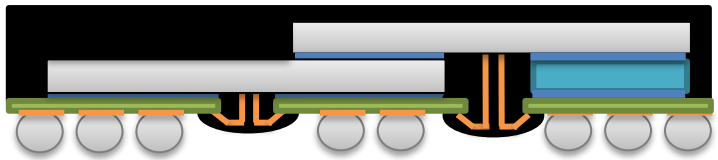
TSOP

BGA

- Mass-Market DRAM have always had laterally displaced Address/Command signals
- Never created much of a timing issue until >1600MT/s operation became the target

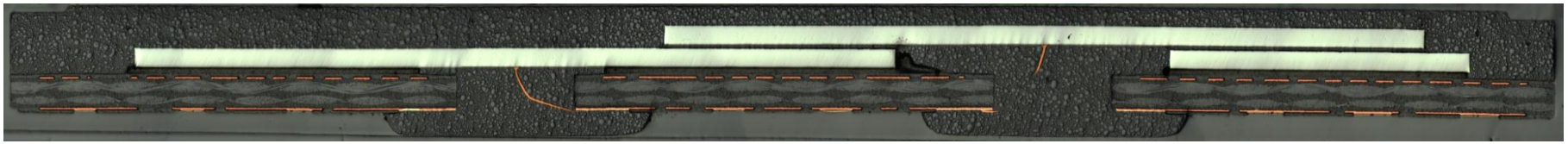
invensas

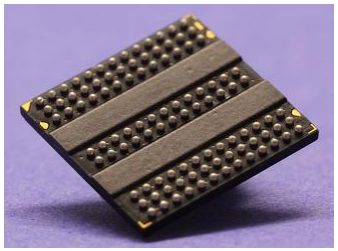
Newly Developed Package: Invensas Dual Face Down: DFD™



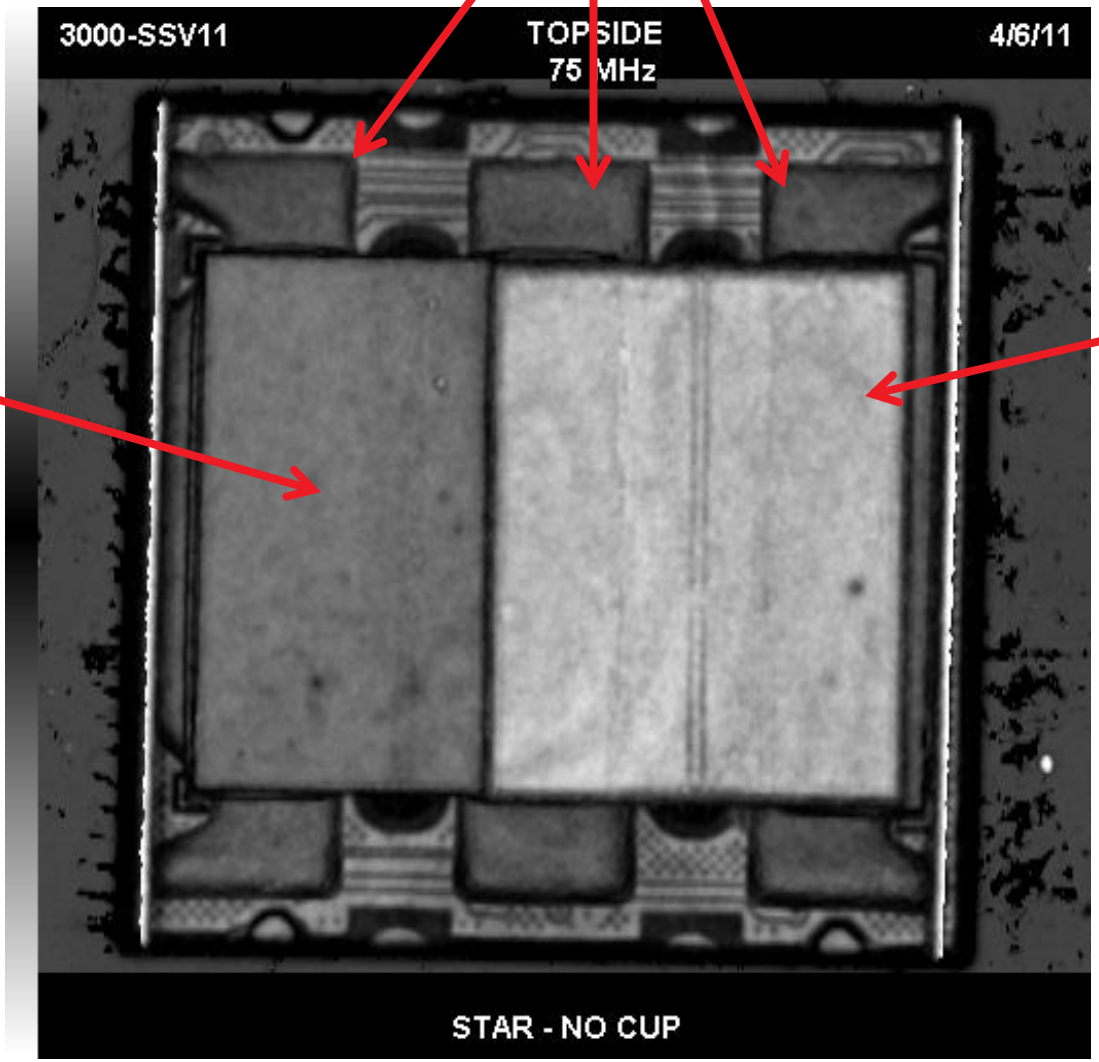
Invensas Dual Face Down

Symmetric performance: similar to Single Die Package
Best thermals
Thinnest structure (no topside wire loops)
Lowest manufacturing cost





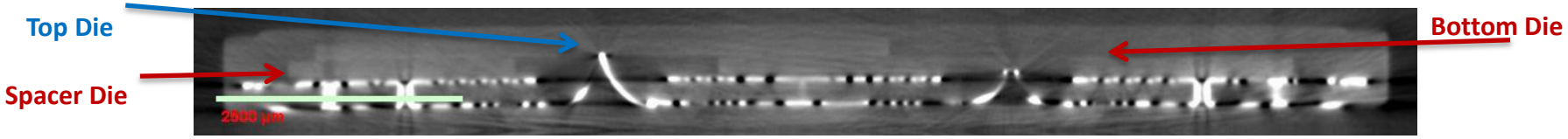
Acoustic Microscope Image: Invensas DFD



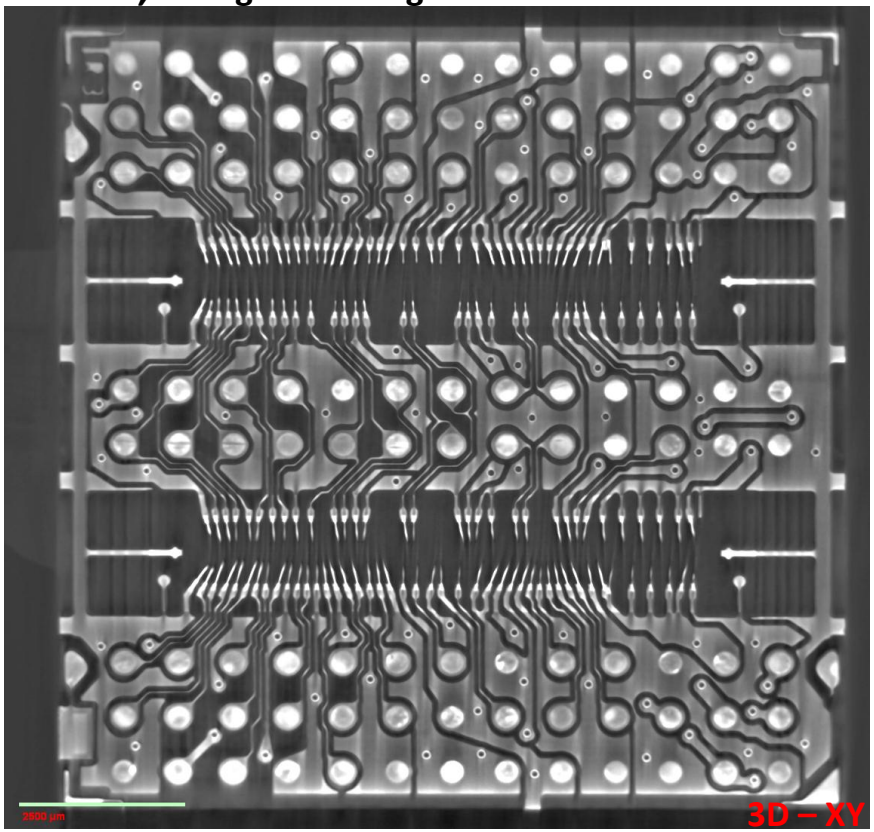
Invensas DFD: XRAY 2D CT Scan

Invensas Dual Face Down package: High Resolution Computerized Tomography – 2D Slices

YZ Slice



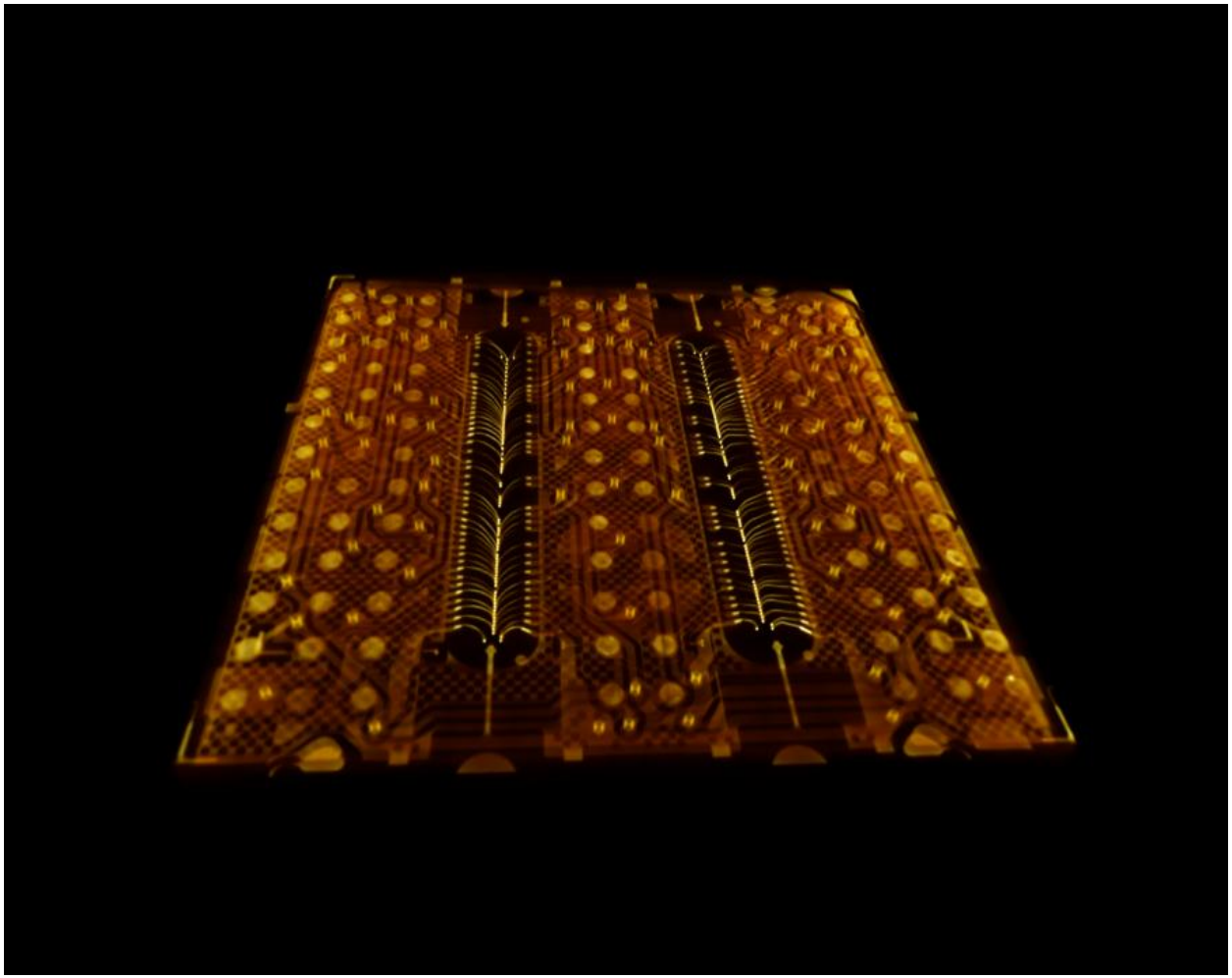
XYSlice; Z height showing bond wires



XYSlice; Z height showing substrate routing

3D – XY Slice

Invensas DFD: XRAY 3D CT Scan



DFD Solves the C/A Stub issue elegantly

	1	2	3				7	8				12	13	14
A	VDD	DM_1	VSS				VDD	VDD				VSS	DM_0	VDD
B	VSS	DQ0_1	DQ2_1				CK	CKB				DQ0_0	DQ2_0	VSS
C	VDD	DQ1_1	DQ3_1				RASB	CASB				DQ1_0	DQ3_0	VDD
D	VSS	DQSB_1	DQS_1				A10	WEB				DQS_0	DQSB_0	VSS
E	ZQ_1	VDD	VSS				A15	BA2				VSS	VDD	ZQ_0
F	VDD	VSS	VDD				BA0	A12				VDD	VSS	VDD
G	VSS	ODT_1	VSS				BA1	A0				VSS	ODT_0	VSS
H	VREFDQ_1	CKE_1	VDD				A3	A1				VDD	CKE_0	VREFDQ_0
J	VDD	CSB_1	VSS				A4	A2				VSS	CSB_0	VDD
K	VREFCA_1	VSS	VDD				A5	A11				VDD	VSS	VREFCA_0
L	VSS	VDD	VSS				A6	A9				VSS	VDD	VSS
M	VDD	VSS	VDD				A7	A14				VDD	VSS	VDD
N	VSS	VDD	RSTB_1				A8	A13				RSTB_0	VDD	VSS

C/A signals in dead center of package in the traditional “No Man’s Land”

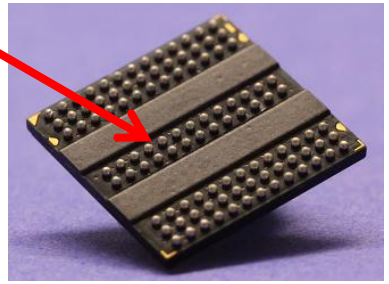
C/A region has simple breakout

C/A Bus Signal ordering matches DDR3 register perfectly

DQs and DQS signals close to package edge

Most other signals only need simple through-hole connections to backside components

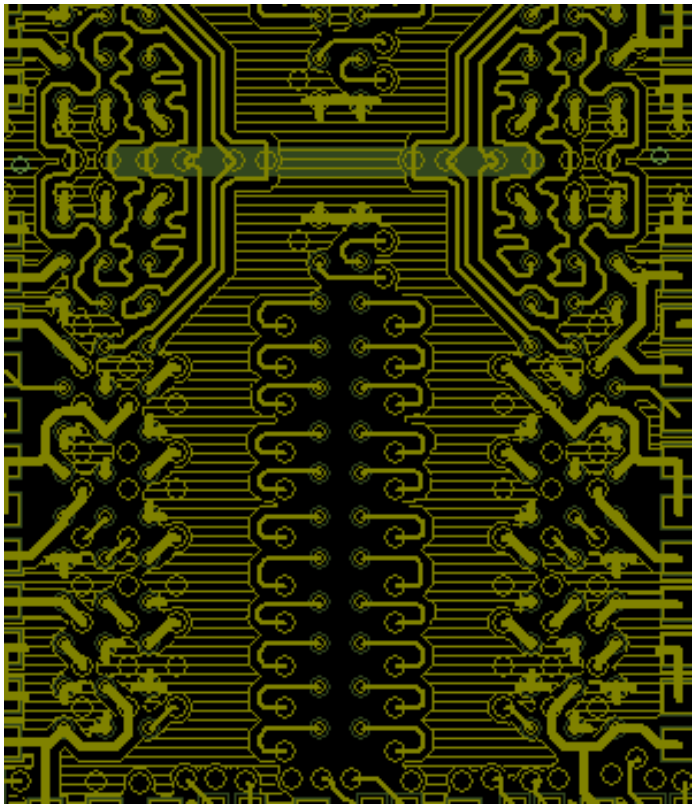
Additional signals will be added to support DDR4



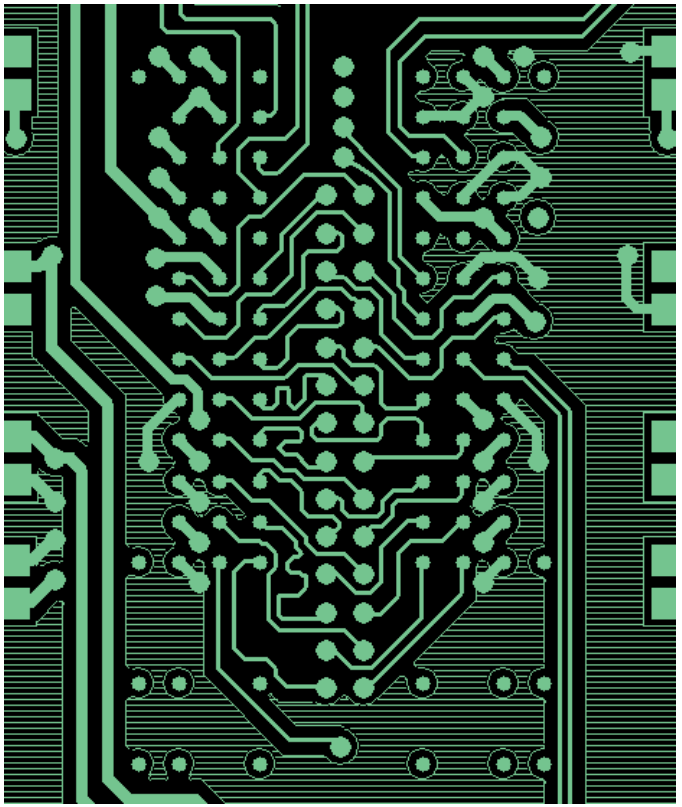
invensas™

Simplified Breakout Using DFD

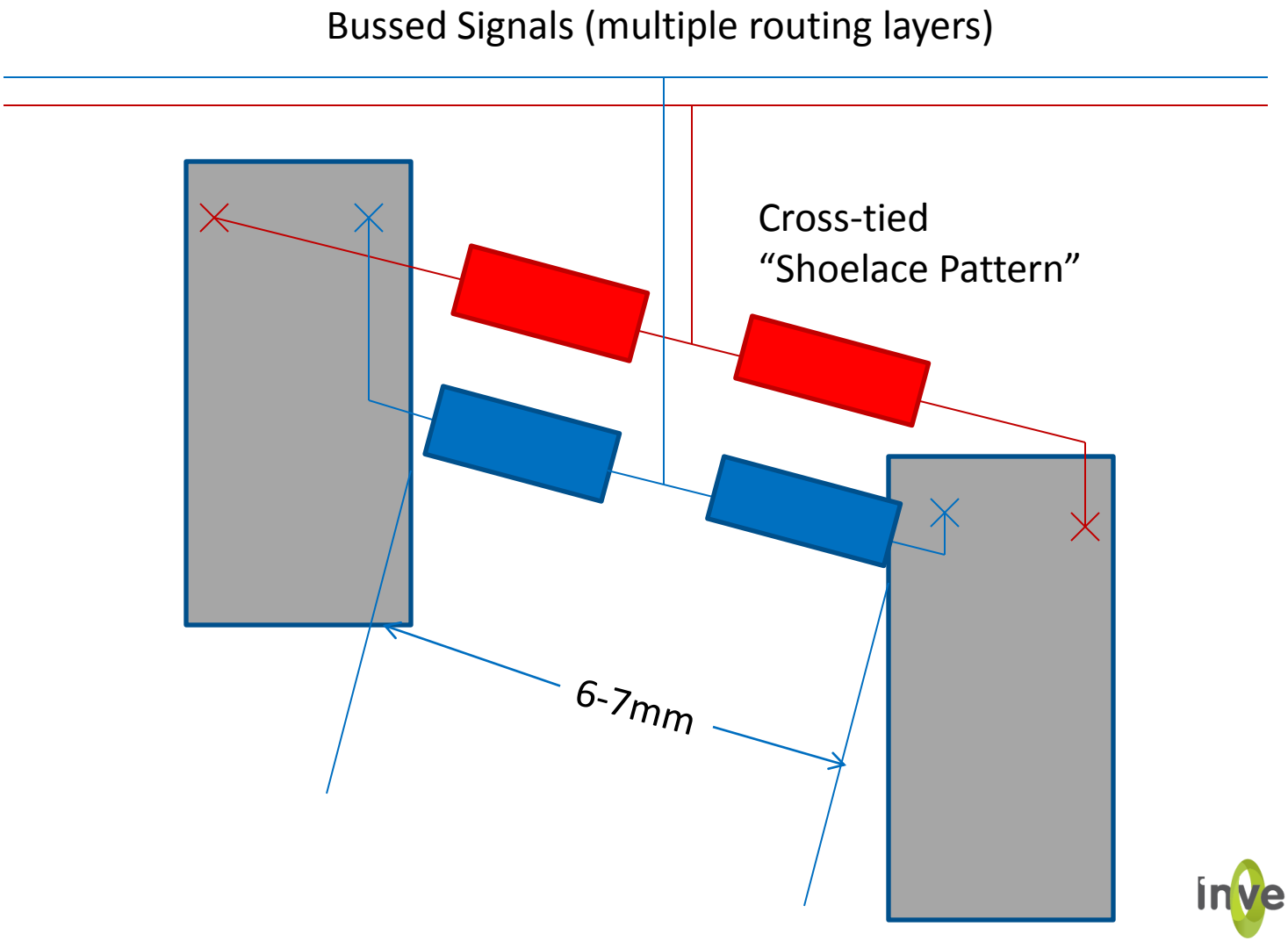
Invensas DFD



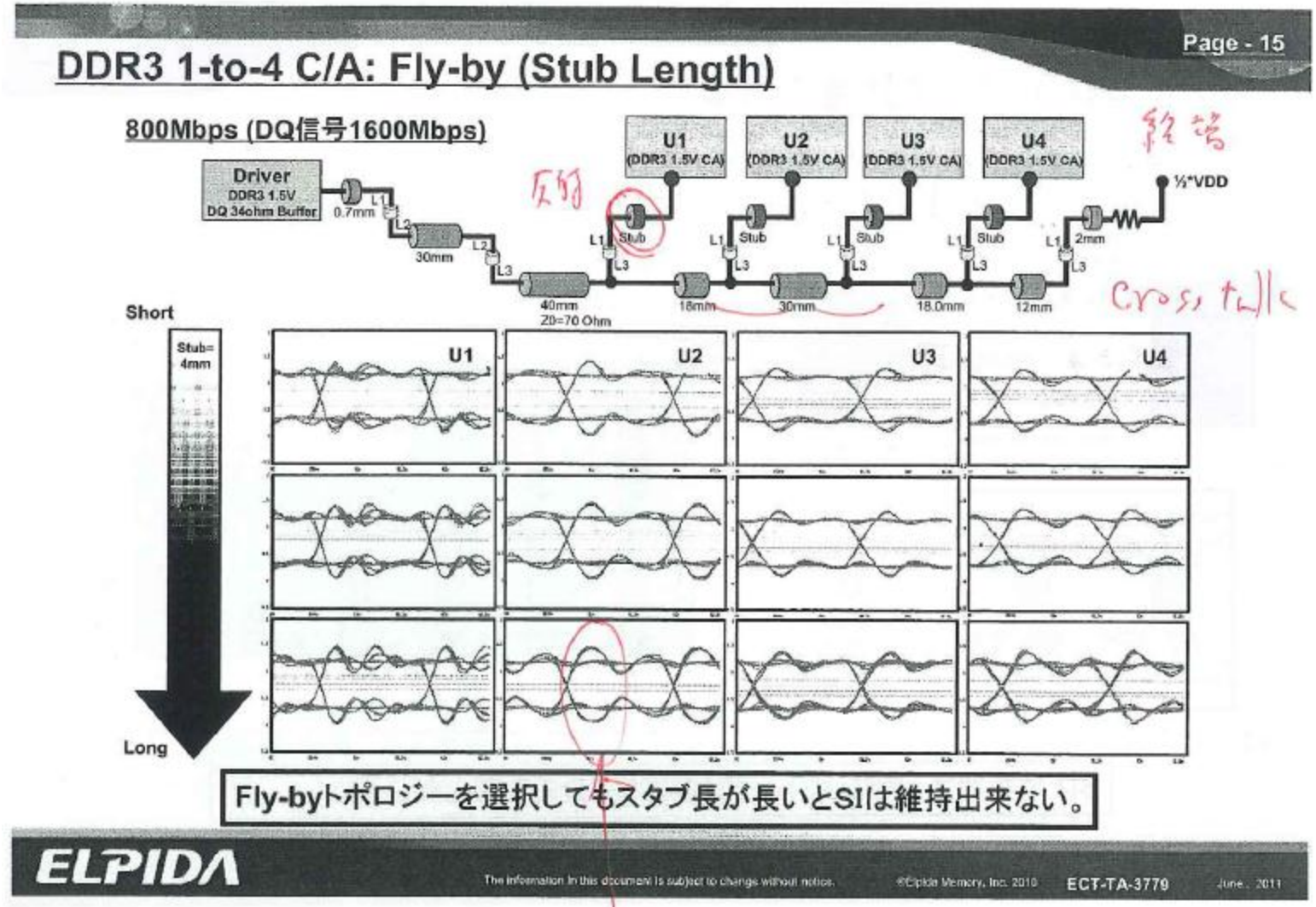
Standard BGA



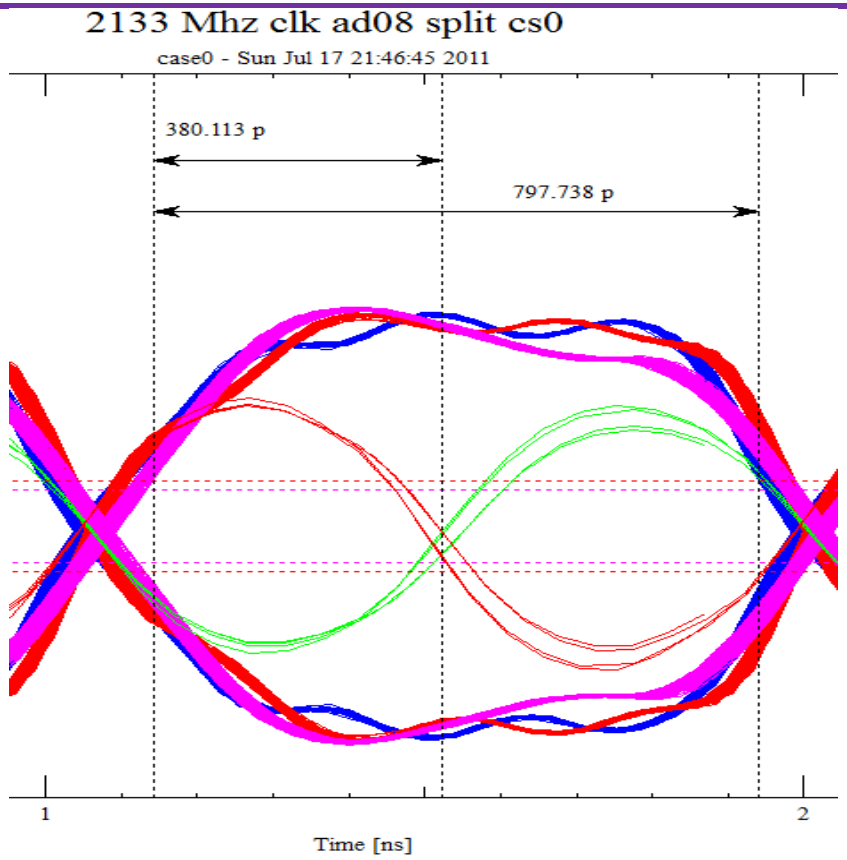
Electrical View: Standard BGA Package Breakout Stubs

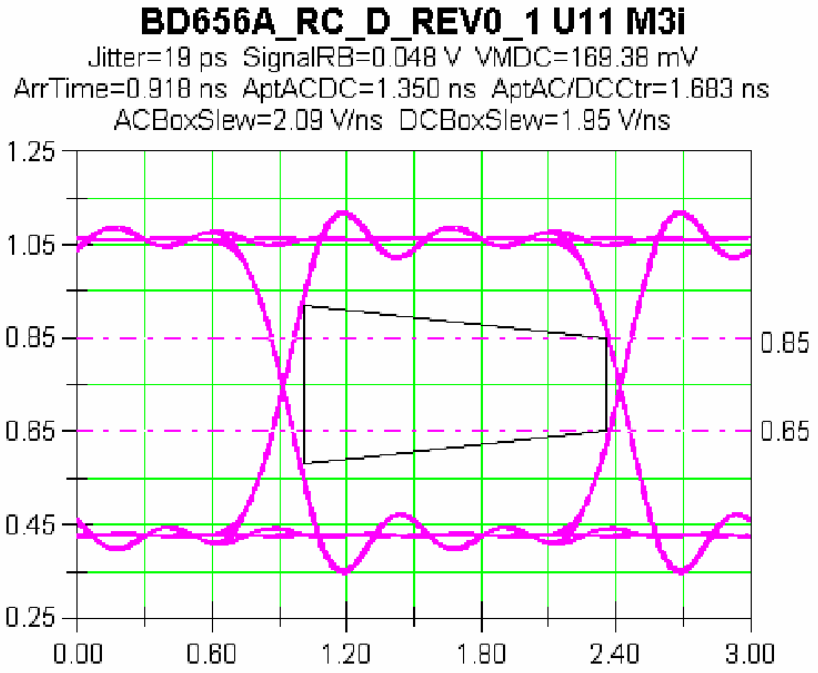


C/A Bus: Stub Issue



A/Clk Simulation at DDR3-2133: 16% more margin at 75% faster operation





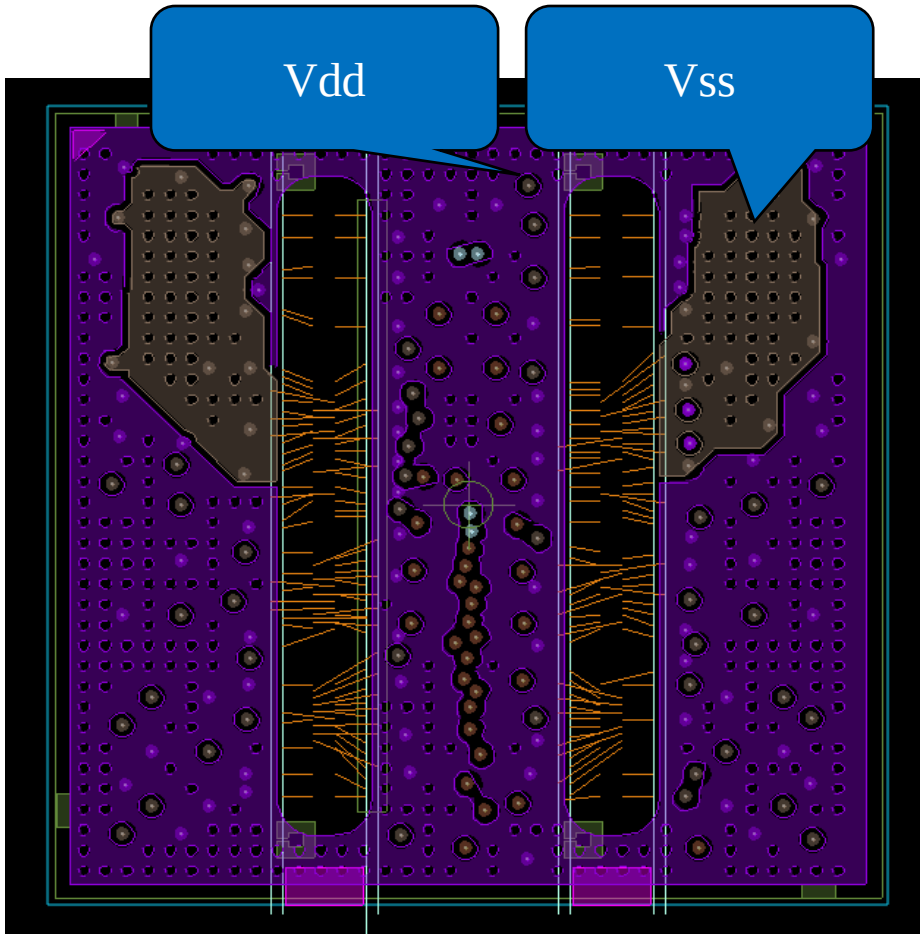
DFD @ 2133

- Window = 798 ps
- Ideal tCK = 938 ps
- 85% of a tCK

JEDEC r/c D @ 1333

- Window = 1093 ps
- Ideal tCK = 1500 ps
- 73% of a tCK

Electrical Considerations: Reference Planes for signals



All C/A signals referenced to Vdd in JEDEC DIMM Specs

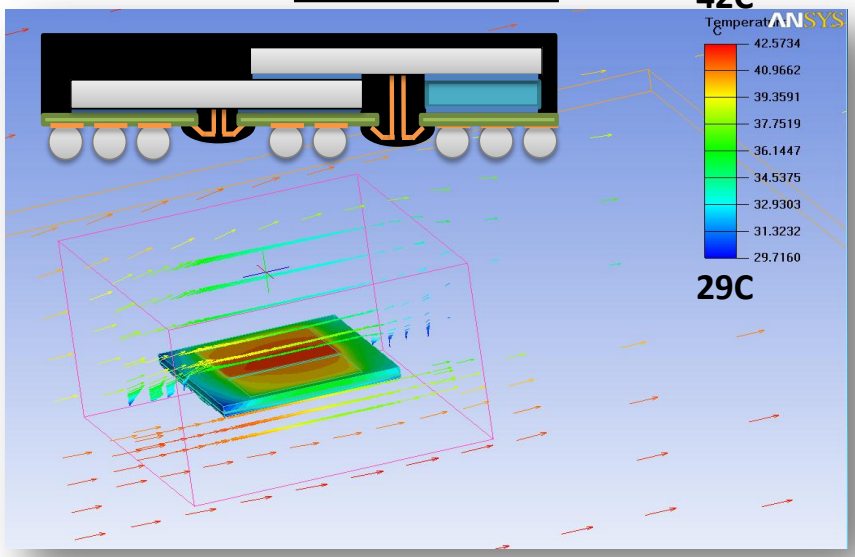
DFD references C/A signals to Vdd in package providing consistent image current path: controller to memory die

DFD also references all non C/A signals to Vss for consistent image current path: controller to memory die

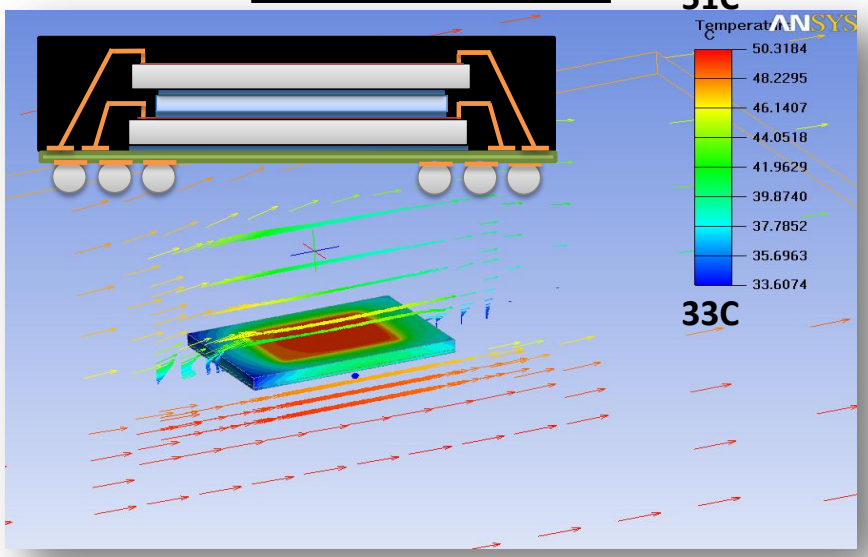
invensas™

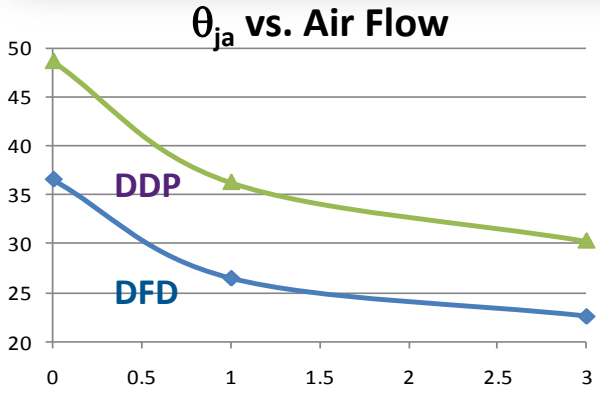
Forced Air Convection Heat Transfer Advantage

Invensas DFD



Conventional DDP





Configuration	DFD (°C/W)	DDP (°C/W)	Delta from DDP
θ_{ja} still air	36.6	48.7	-25%
θ_{ja} @ 1m/s	26.5	36.3	-27%
θ_{ja} @ 3m/s	22.6	30.3	-25%

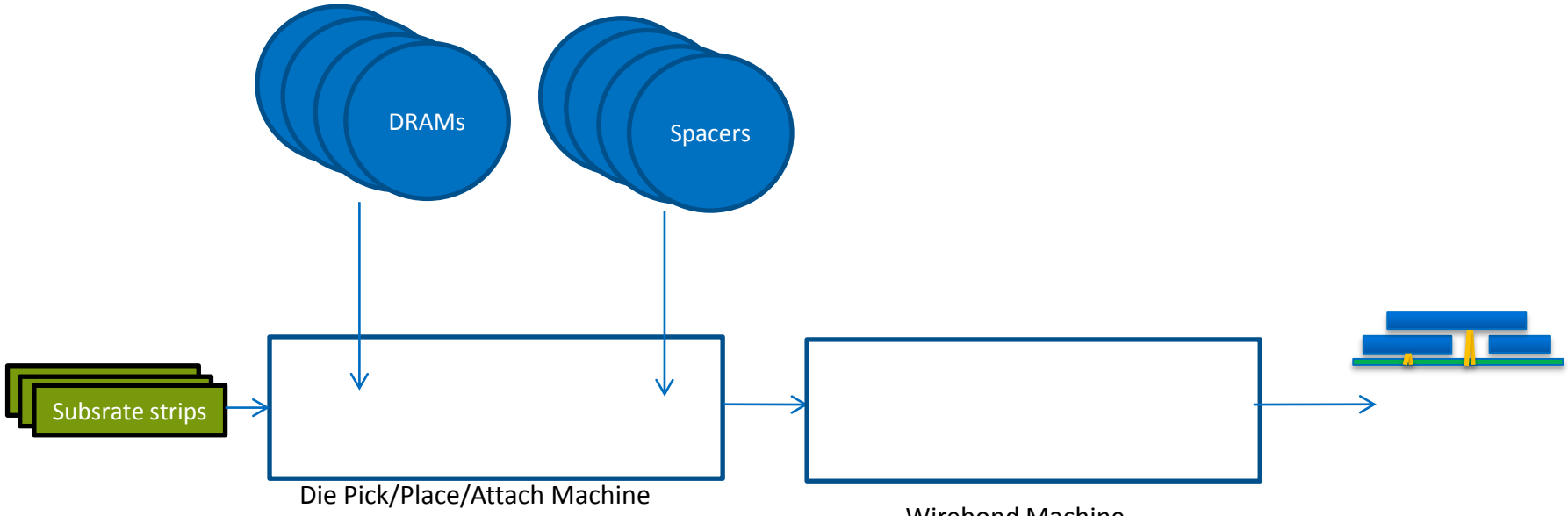
~25% lower θ_{ja} for DFD vs. conventional DDP package

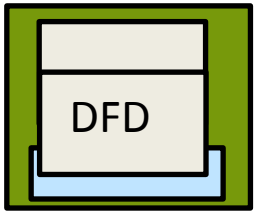
invensas™

Manufacturing cost: process flows

invensas™

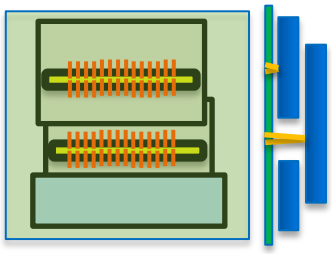
Line flow example: DFD die attach and wirebond





All die + spacers placed
on substrate in one machine pass
All live die sourced from same
wafer

DFD

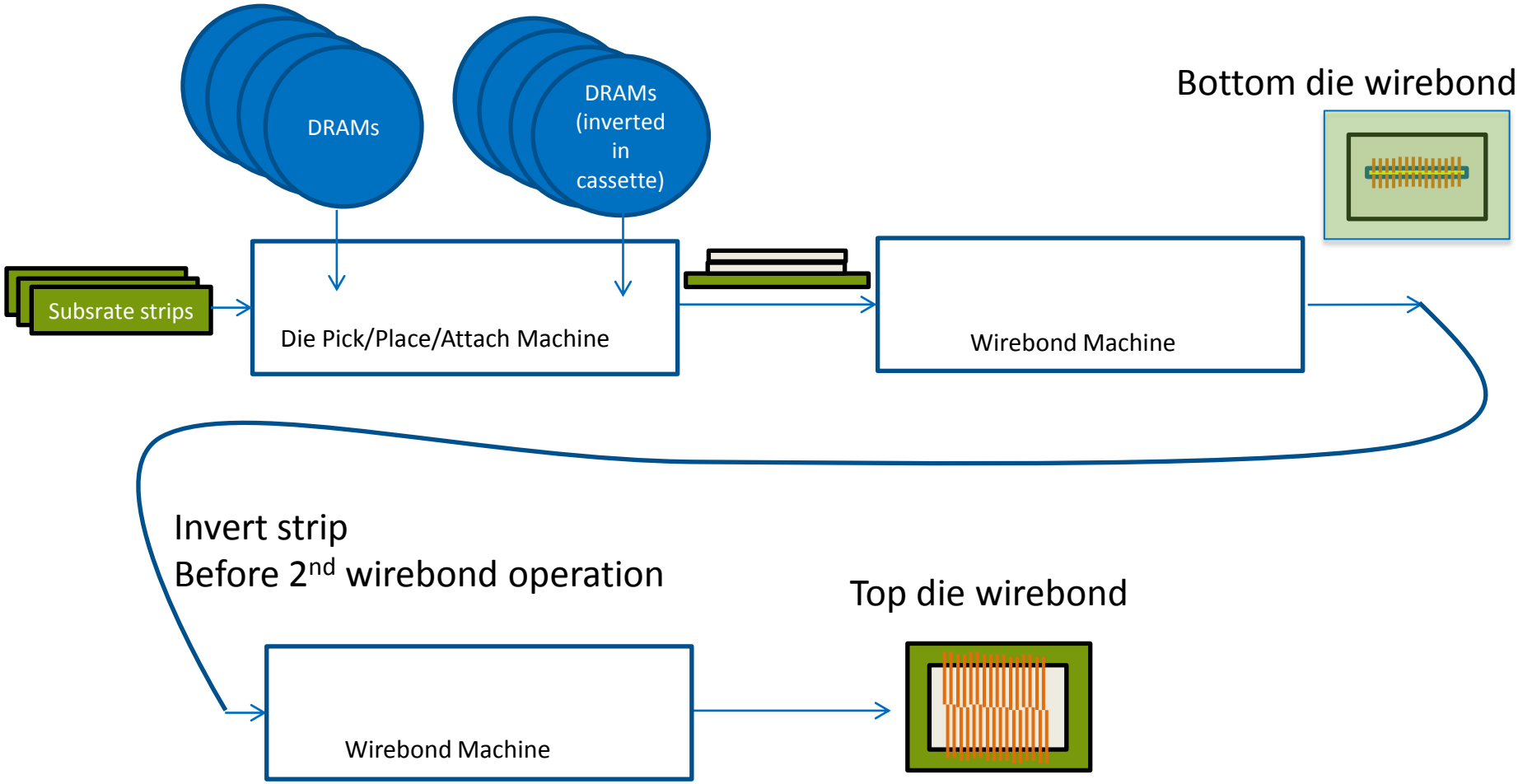


All die wirebonded in a single pass

Two Machine Insertions: die attach and wirebond all die for a dual die package

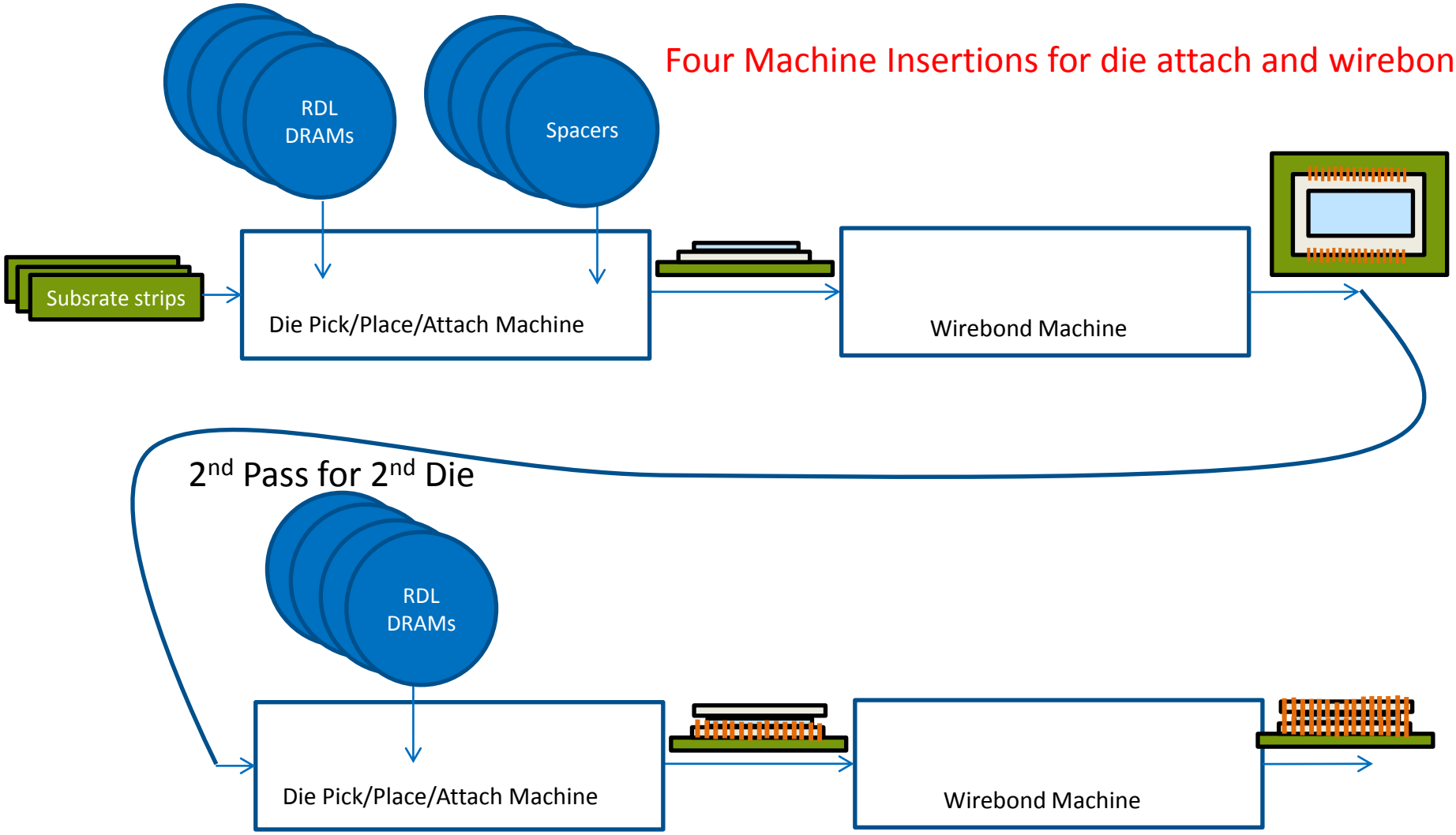
invensas

Line flow example: Opposing Face DDP die attach/wirebond

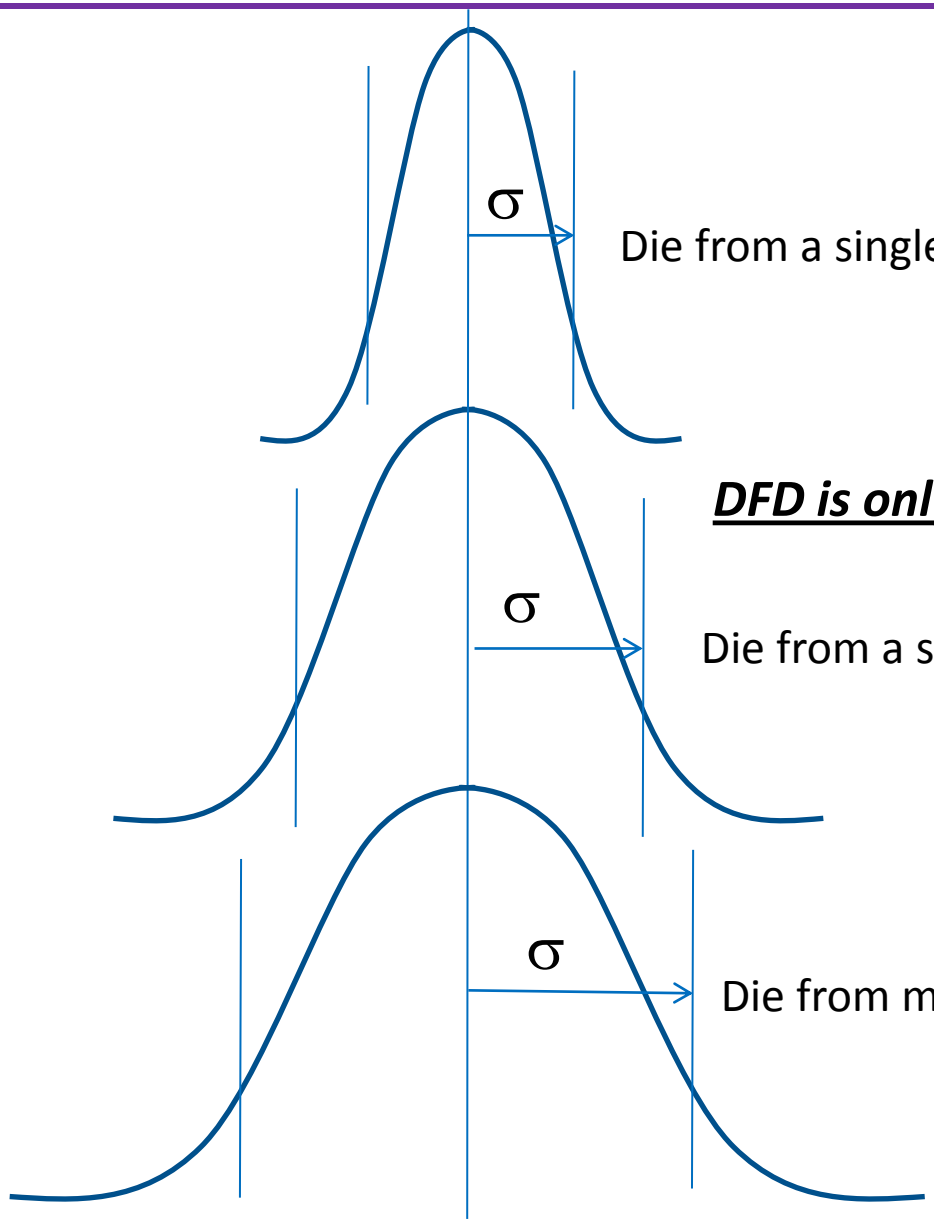


Three Machine Insertions for die attach and wirebond

Line flow example: RDL DDP die attach/wirebond



Wafer/Die Speed binning statistics

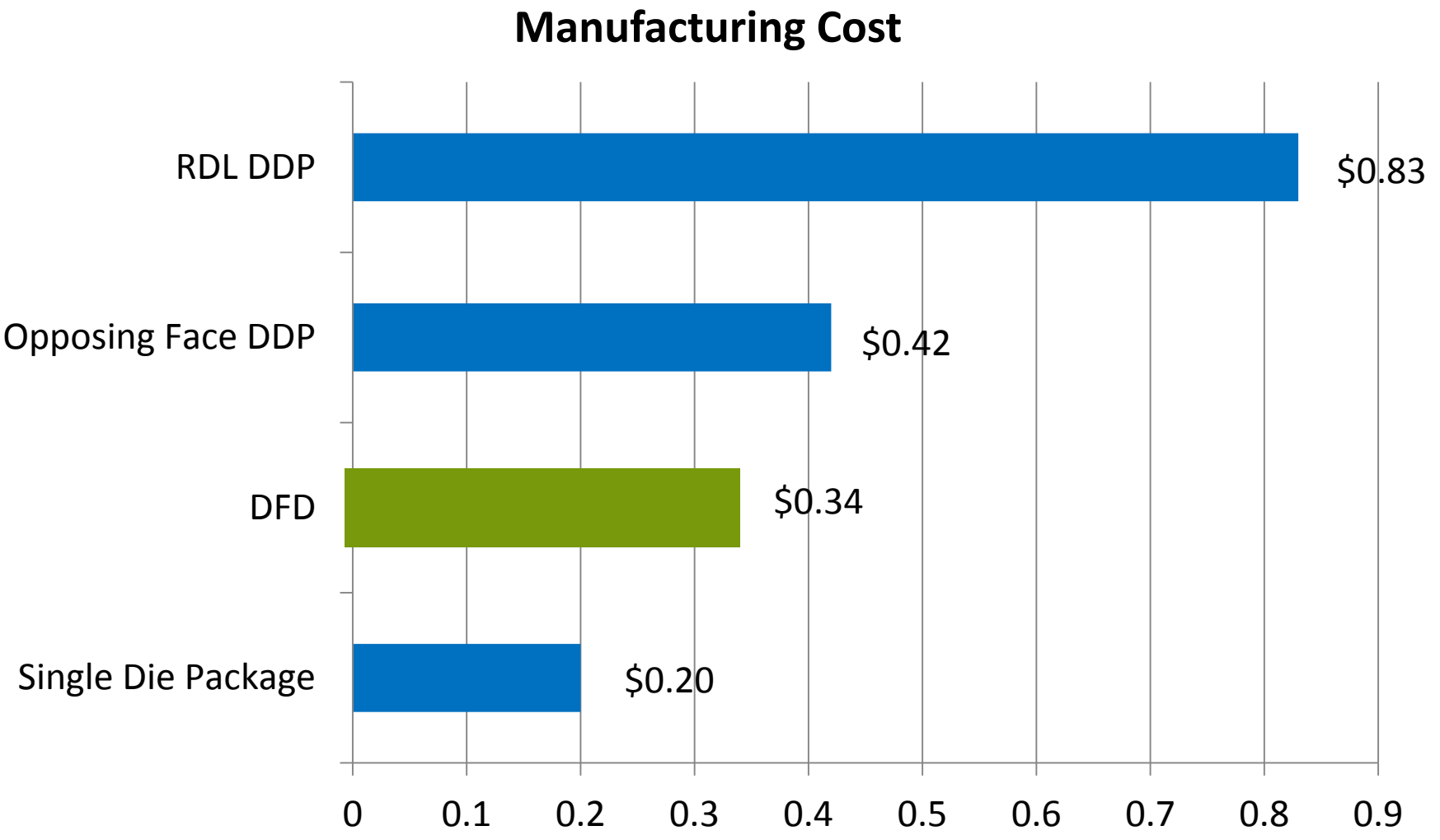


Die from a single wafer show tighter speed distribution vs multiple wafers/wafer lots

DFD is only DDP that picks all die from same wafer

invensas™

Cost Comparison

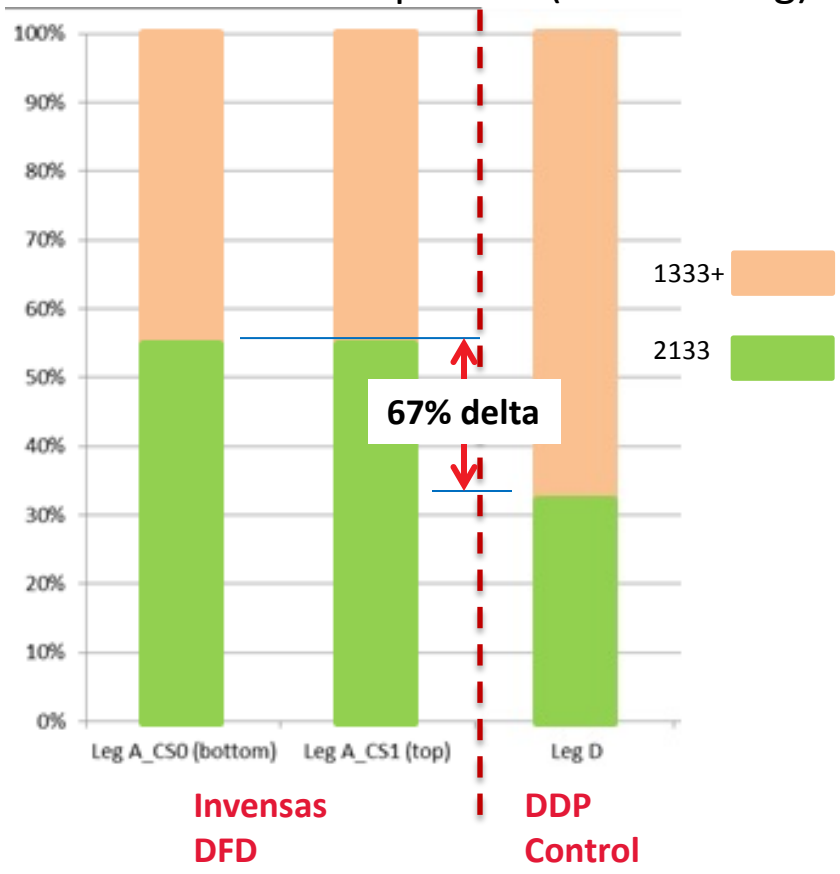


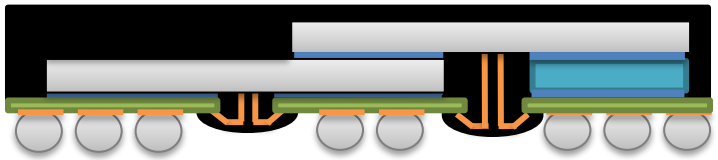
Sort Yield Advantage: Invensas DFD vs Conventional DDP

Bin splits of yielded goods improved significantly

Speed Bin Yield vs. Control

1000 unit sample size (95°C testing)





Leg A bottom, Leg B top

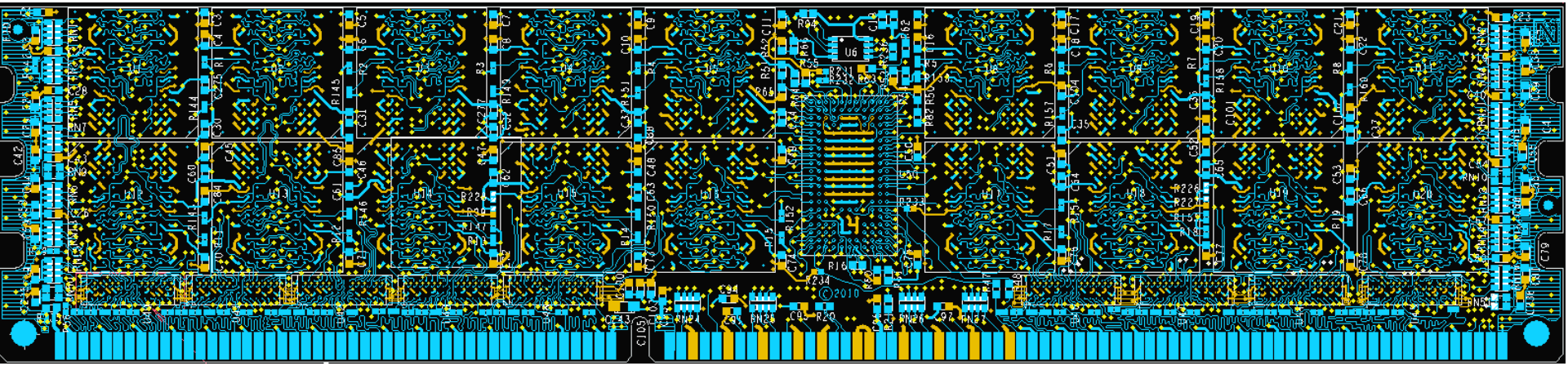
Leg D (top die only w/o substrate routing for lower die: performance is therefore optimistic)

- 67% Improvement in 2133MT/s Yield vs Control using same wafer lot

DIMM Design Example:
Multi-Rank Buffered DIMM PCB

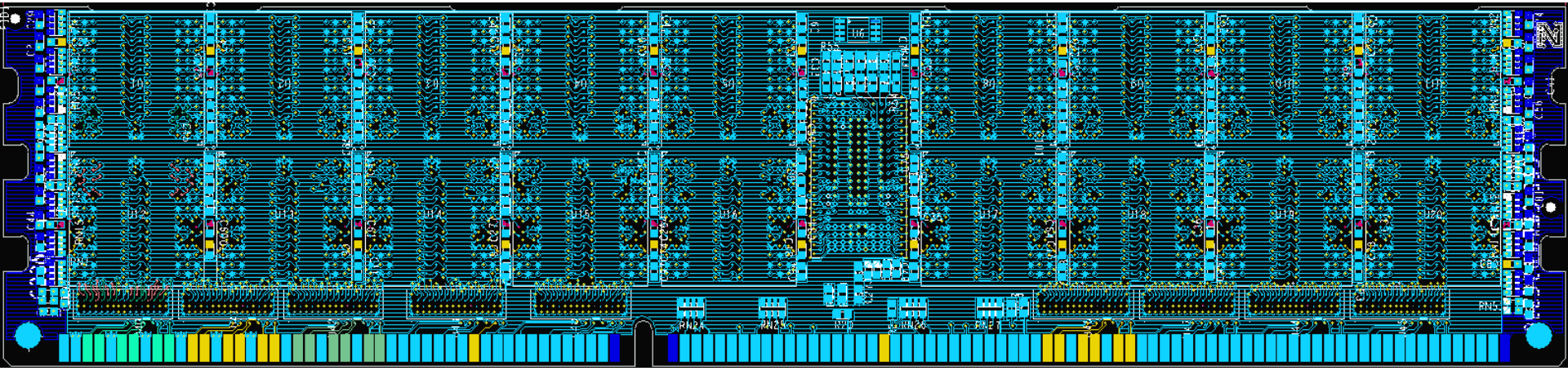
invensas™

Comparison: DDP vs DFD (Breakout layer)



DDP

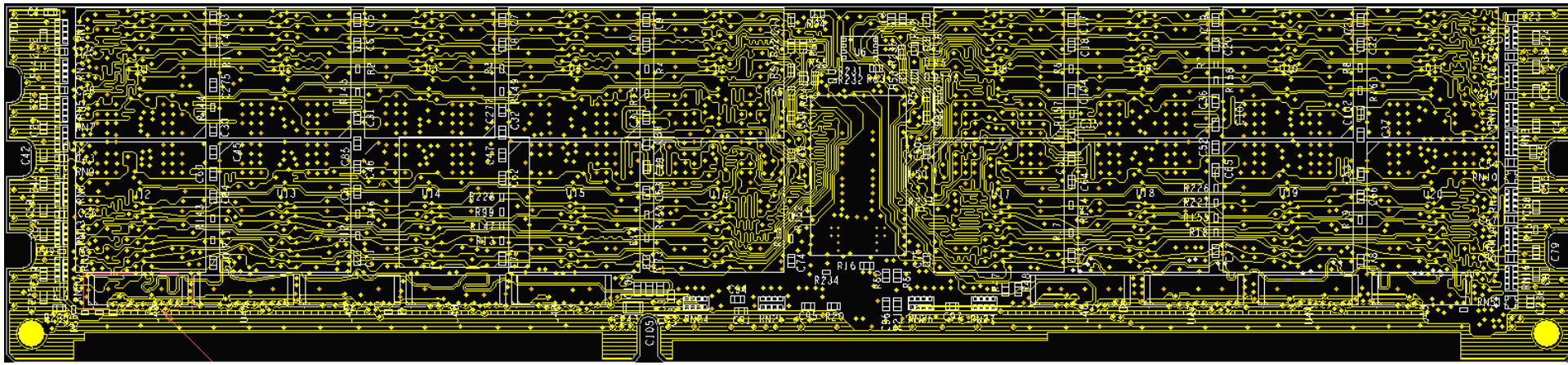
Layer 1: Breakout, Isolation Devices, Register, TSE SPD



DFD

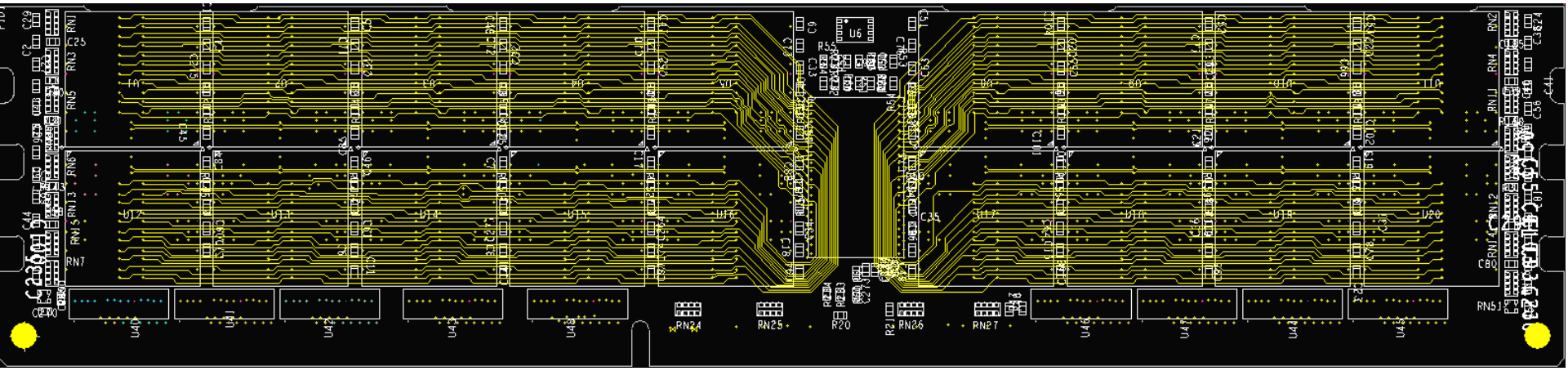
invensas™

Comparison: DDP vs DFD (Address/Command)



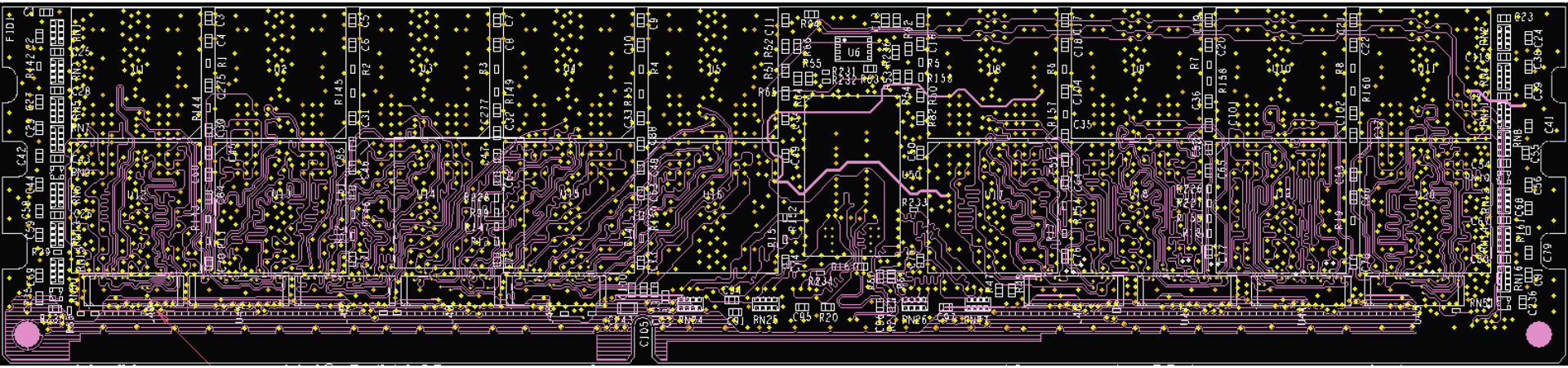
DDP

Layer 4: Post-Register Device Address, Command



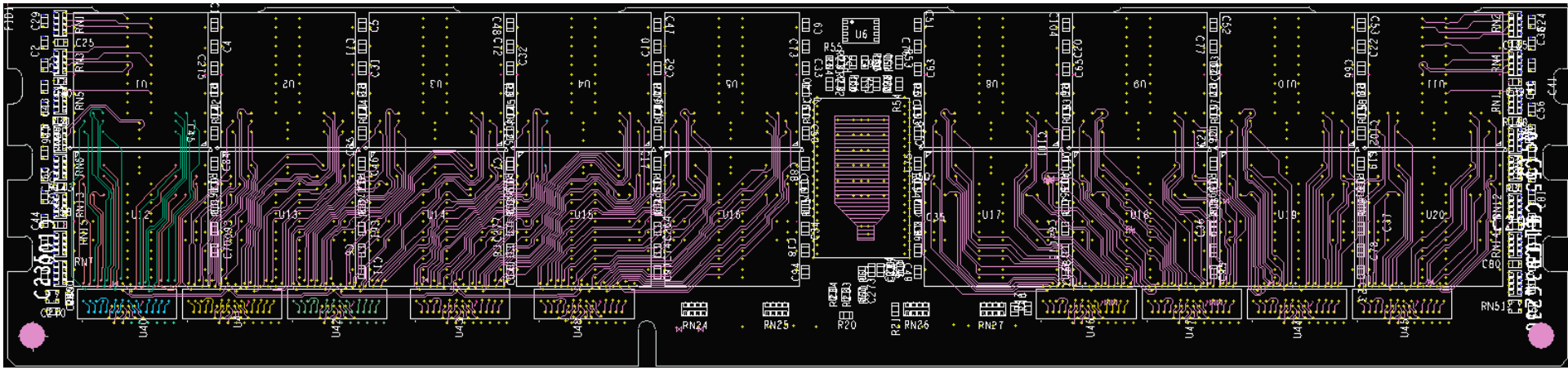
DFD

Comparison: DDP vs DFD (Data/Data Strobes)



DDP

Layer 3: Data routing



DFD

Measured RDIMM Results

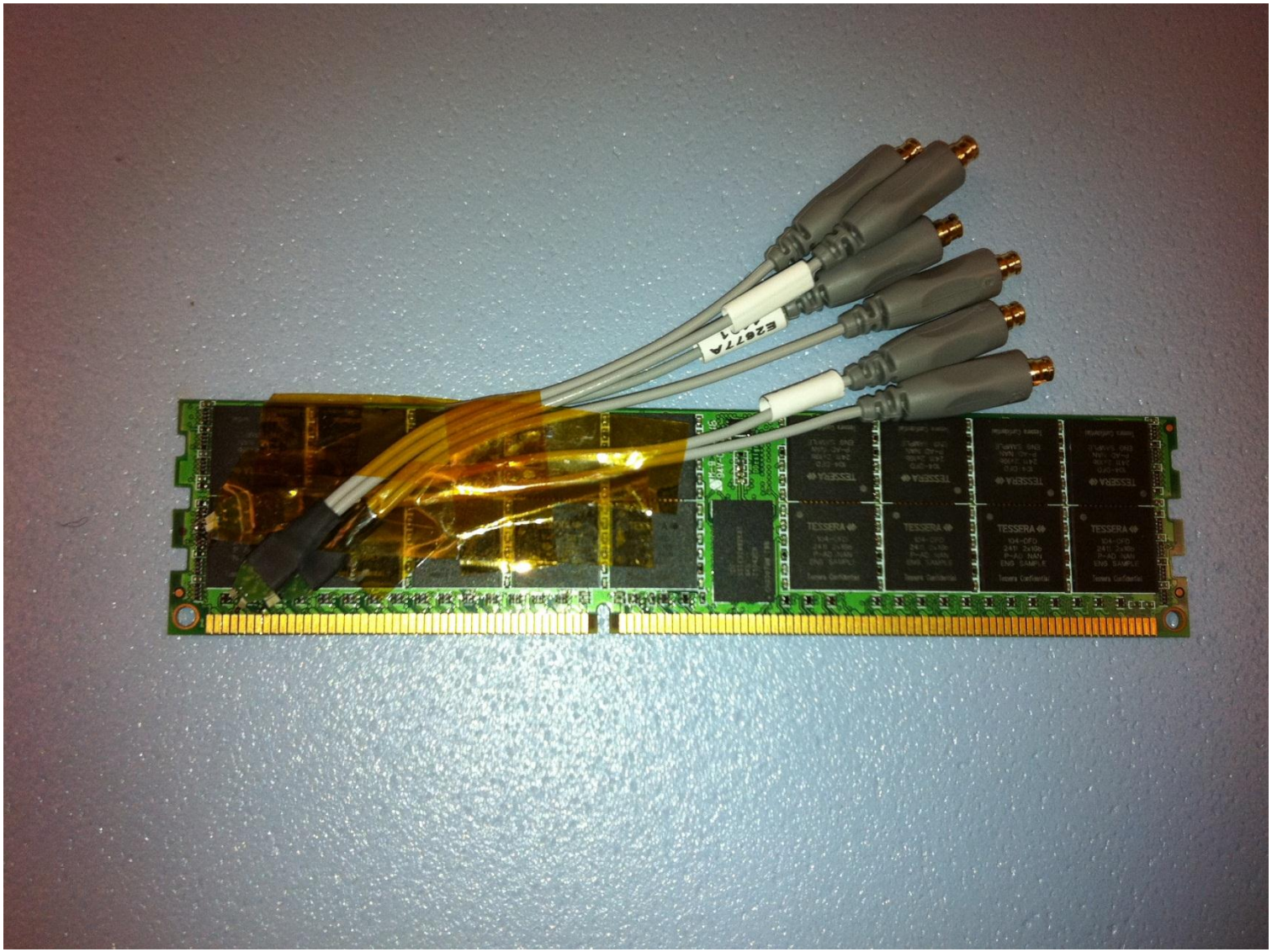
invensas™

Overview of RDIMM Evaluation Vehicle

- Invensas developed an 8GByte Quadrank x72 ECC RDIMM using the DFD package technology (dual 1 Gbit die/package)
- Each module contains 72 die of 1Gbit capacity (x4 die organization)
- Standard RDIMM edge connector/module form factor
- Initial testing: full speed in-system with Memtest 86
- Additional at-speed probing of signals in-system with 12GHz DSA

invensas

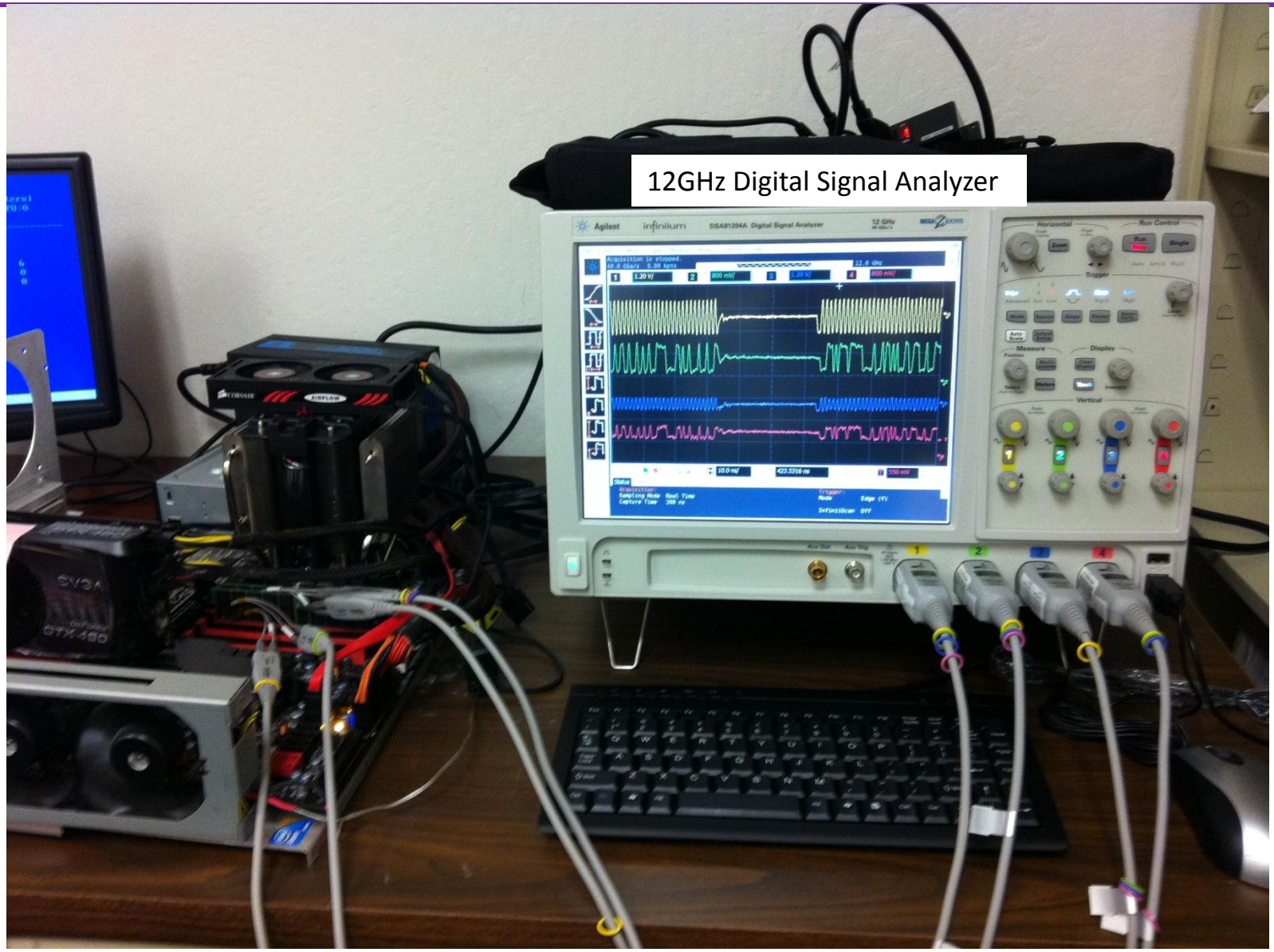
Instrumented DIMM With Probes Solder-Attached



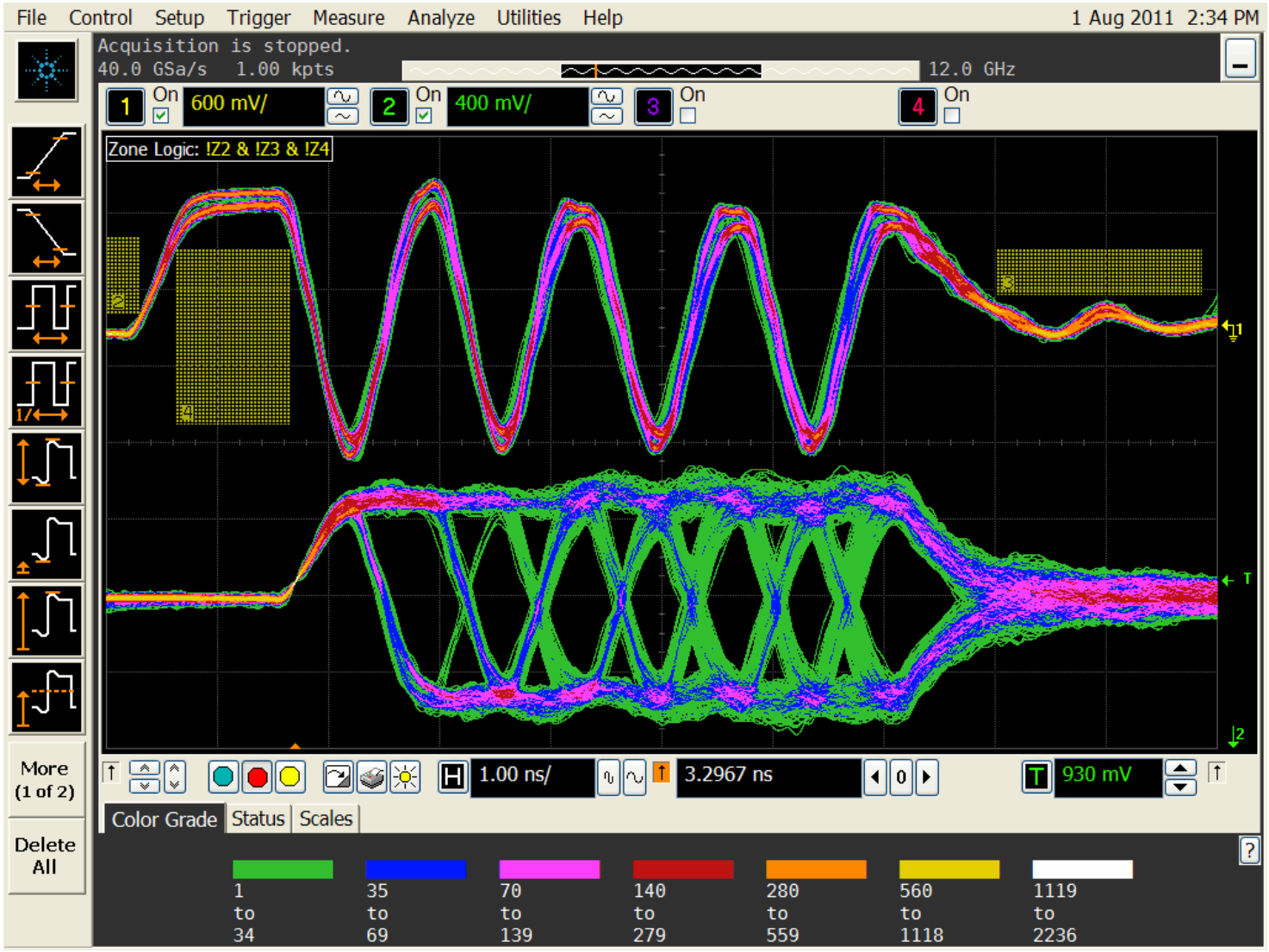
For full-speed in-system probing of DQ, DQS

invensas™

In-System Test Setup

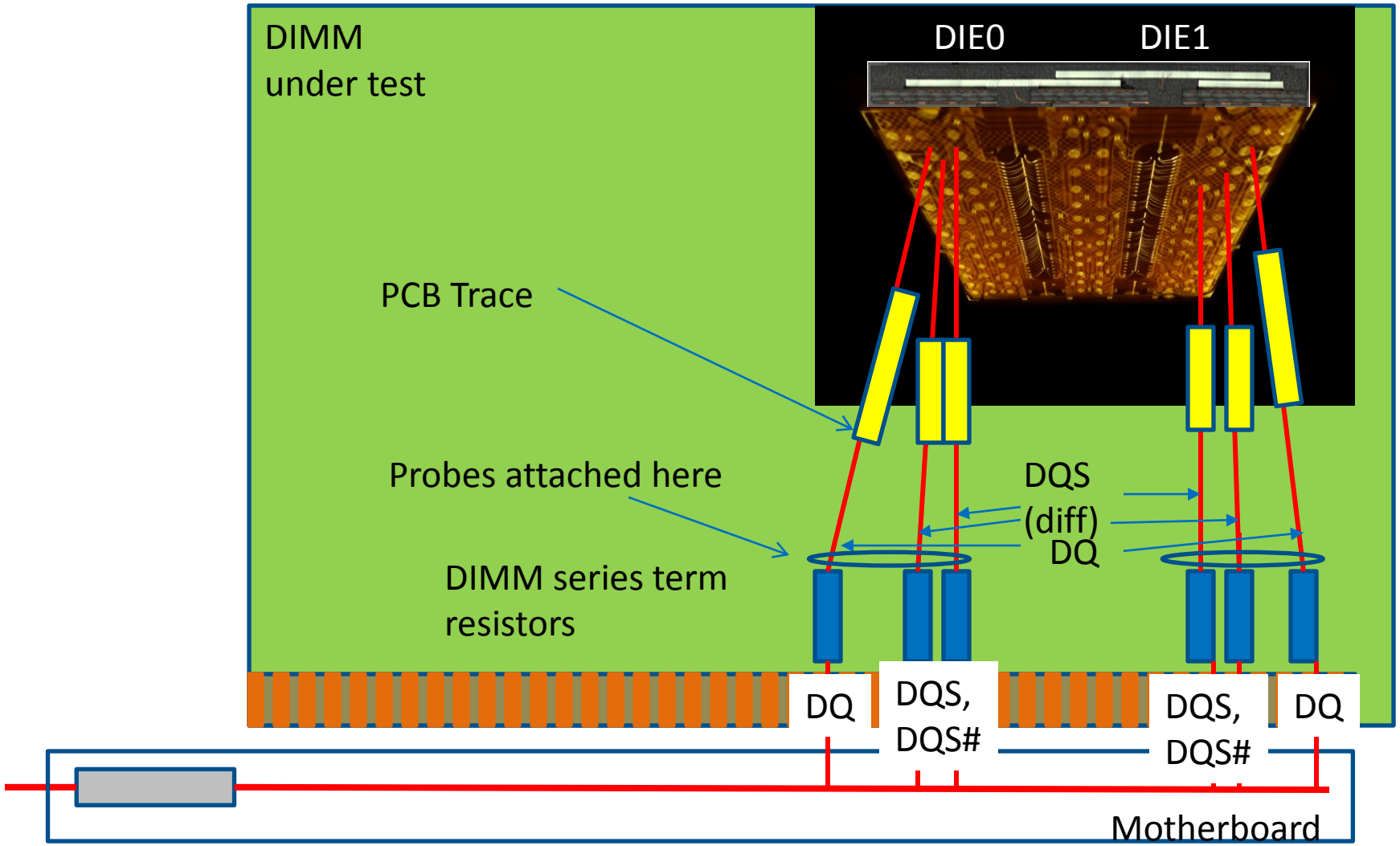


Read Eye Diagram (Quadrank RDIMMs, 2DPC @1600MT/s)



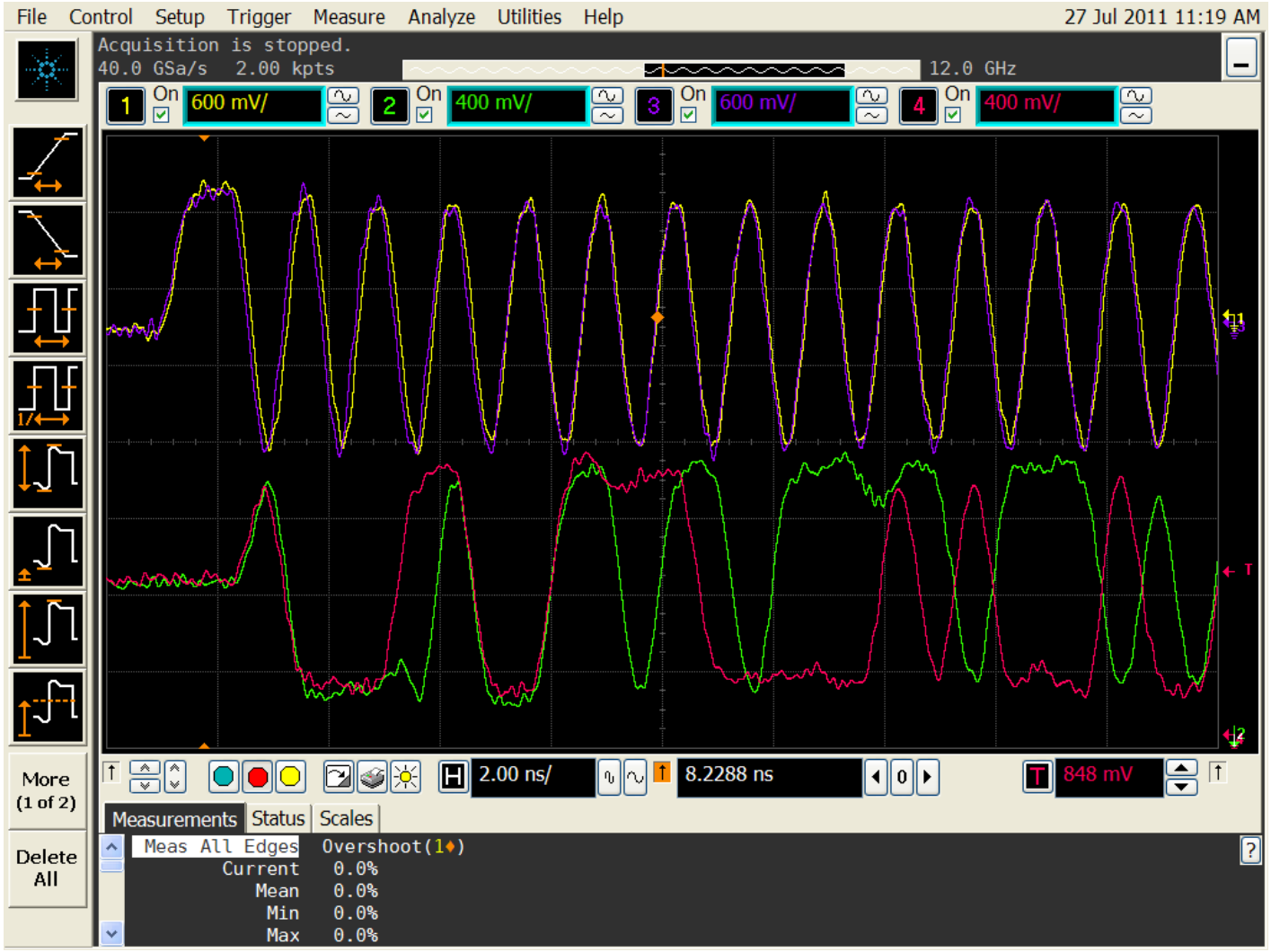
Symmetric Performance

(DQx, DQS from die in same package)



invensas

DFD Reads Same Package, Both Die



DQS (DIE0)

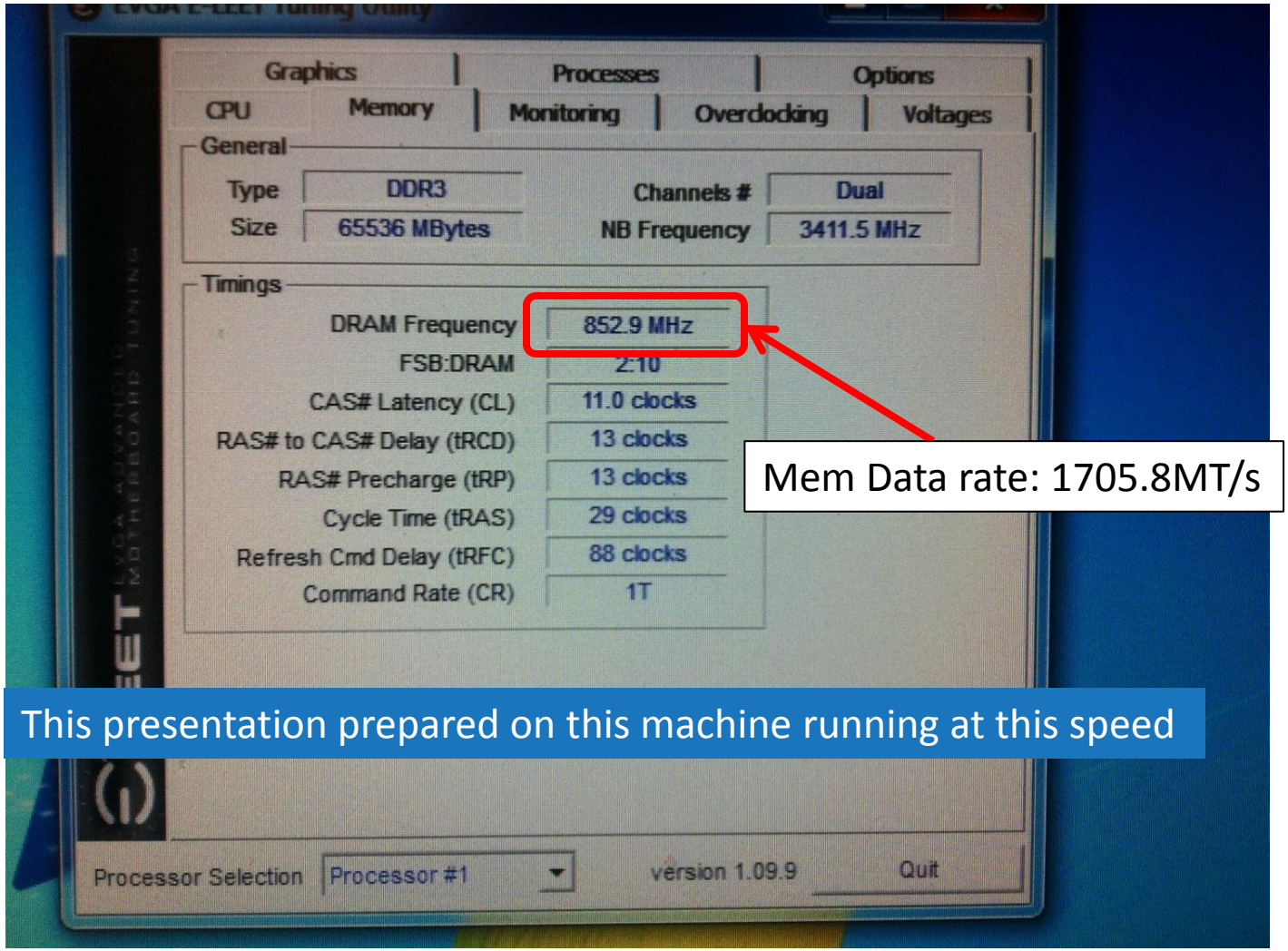
DQS (DIE1)

DQ (DIE1)

DQ (DIE0)

invensas

Running Windows: Two DIMMs/Channel at 1700MT/s



invensas

Conclusion

- A performance-enhanced cost-reduced double die DRAM package was developed
- The package features a streamlined manufacturing flow and is the lowest cost way to assemble a given number of DRAM die
- The ballout is very easy to use on a DIMM PCB: simple routing with minimal length stubs contribute to enhanced electrical performance
- Thermal characteristics are more than 25% better than standard DDP
- Significant simplification of DIMM PCB routing demonstrated
- A quadrank RDIMM was developed and measured; with 2DIMMs/Channel reliable operation beyond 1700MT/s was observed
- This talk was prepared using the test machine using 8 pieces of 8Gbyte Quadrank DFD RDIMMs in 2DPC configuration at 1700MT/s

invensas™