Mismatch Compensation of CMOS Current Mirrors Using Floating-Gate Transistors

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Abstract— The simple CMOS current mirror is a fundamental compositional element which is employed in a wide variety of analog and digital circuit designs. The use of CMOS current mirrors is appealing to circuit designers given the low cost associated with CMOS fabrication and the inherent simplicity of operation. Unfortunately, the simplicity of the CMOS current mirror makes it particularly susceptible to device mismatch due to process variations. In recent years the use of floating gate transistors for mismatch compensation has become increasingly popular. We report on our observations regarding the efficacy of this technique in both weak and strong inversion and present analytical and simulated results quantifying these observations. The central result is that although compensation using floating gates works well for correcting mismatch for subthreshold operation, similar compensation in above threshold operation results in the introduction of previously unseen mismatch effects.

I. INTRODUCTION

The proper operation of many types of circuits relies on the precision and accurate operation of the current mirror. Previous work has shown that current mirrors employing MOSFETs have a much greater degree of mismatch than those constructed with BJTs [1], with a likely cause being the great effect that surface charge anomalies have on the MOS current flow mechanism. However, the use of CMOS processes remains very popular given their widespread availability and the low cost associated with fabrication. Although modern commercial CMOS processes are very mature, and advancing rapidly, it is generally accepted that as feature sizes decrease, the effects of process variation become even more significant than in the past.

The simple CMOS current mirror is a two transistor circuit. For the purposes of this discussion we will focus on the NMOS version since it has been shown that PMOS based circuits suffer from a greater degree of mismatch due to higher mobility variations and poorer gate oxide capacitance matching [2]. The results discussed here are directly relevant to the operation of both NMOS and PMOS current mirrors. The NMOS current mirror is shown in Fig(1), and in the case of ideal operation (neglecting the effects of mismatch and channel length modulation), \( I_{out} = I_{in} \).

In section II we discuss the typical sources of mismatch and the techniques which are commonly used for compensation. Section III outlines important mismatch parameters, develops the SPICE models used for simulation, and presents the results of our analysis and simulation of mismatch in both strong and weak inversion. Section IV introduces the floating gate current mirror, discusses the tuning capabilities afforded by such a structure, and shows the results of our analysis and simulation of the mismatch compensated current mirror for both regimes of operation. Finally, Section V summarizes our findings.

II. SOURCES OF MISMATCH

Mismatch amongst transistors of equivalent geometry arises primarily from localized process variations such as fluctuations in doping intensity and device dimensions, impurities in the silicon, surface states, and defect traps. A number of circuit layout techniques have been suggested to mitigate the occurrence of mismatch. These include the use of large geometries, multiple finger elements, and common centroid layout methods [3], [4]. All of these methods are effective to some degree, but still depend heavily on the quality of the fabrication process.

There are also circuit design techniques which can be used to increase the accuracy of current mirror operation [5], [1], but these methods generally result in significantly increased complexity. Here we have chosen to focus on mismatch compensation for the principal sources of mismatch in the MOS device using the floating gate current mirror.

III. MODELING THE EFFECTS OF MISMATCH

The three parameters best suited for modeling mismatch are the threshold voltage \( V_{th} \), subthreshold slope \( \kappa \) and the transconductance \( \beta \) [1]. Another factor which can be a source of mismatch is the channel length modulation parameter \( \lambda \), but the effect of variations in \( \lambda \) only come into play at high drain voltages, and more importantly when the drain voltages of the two transistors differ. In this paper we will neglect the effect...
of variations in \( \lambda \), since it will allow us to look at some of the more fundamental causes of mismatch which are present when all other operating conditions are equivalent.

To show the effects of mismatch using simulation, we have developed two sets of 100 different BSIM3v3 SPICE models. The first of which represents uniform distributions of \( V_{th} \) mismatch and \( \beta \) mismatch, using the parameters \( V_{th0} \) and \( \mu_0 \) respectively. Ten values of \( \Delta V_{th} \) are used, ranging from \(-100 mV\) to \(+100 mV\). Correspondingly, ten values of \( \Delta \mu_0 \) are also used, ranging from \(-100 \frac{cm^2}{V_s}\) to \(+100 \frac{cm^2}{V_s}\). The second set of models were developed in a similar manner to represent uniform distributions of \( I_0 \) mismatch (using \( \mu_0 \) ranging from \(-100 \frac{cm^2}{V_s}\) to \(+100 \frac{cm^2}{V_s}\)) and \( \kappa \) mismatch (using the \( N_{factor} \) parameter, ranging from -20% to +20%). The \( I_D - V_G \) characteristic of a MOS transistor was simulated for all possible combinations of these parameters within each model set.

A. Mismatch in Strong Inversion

Neglecting channel length modulation, the drain current of an NMOS operating in the above threshold saturation regime is given by

\[
I_D = A(V_{GS} - V_{th})^2
\]

where \( A = \frac{\kappa W}{2L} \) is the transconductance parameter and \( V_{th} \) is the threshold voltage. The input characteristic for the current mirror becomes

\[
I_{in} = A(V_{in} - V_{th})^2
\]

The output characteristic including the effects of mismatch is given by

\[
I_{out} = (A + \Delta A)(V_{in} - V_{th} - \Delta V_{th})^2
\]

Ignoring second order terms, the transfer function for \( I_{out}/I_{in} \) can be approximated by

\[
\frac{I_{out}}{I_{in}} \approx 1 + \frac{\Delta A}{A} - 2\sqrt{\frac{A}{I_{in}}} \Delta V_{th}
\]

The effects of mismatch for above threshold operation in the saturation regime are shown in Fig (2), which is a \( \log I \) vs \( V \) plot. Whereas the voltage offsets arising from \( \Delta V_{th} \) are easily observed in Fig (3a), the errors introduced by \( \Delta I_0 \) are not as apparent as in the above threshold case. The horizontal shift is much smaller for the case of \( \Delta V_{th} \) mismatch in Fig (3b), but the variation in gain becomes significant.

B. Mismatch in Weak Inversion

Neglecting channel length modulation and body effect, the drain current for subthreshold operation in the saturation regime is given by

\[
I_D = I_0 e^{\frac{\kappa (V_{GS} - V_{th})}{V_T}}
\]

where \( I_0 \) is the pre-exponential scaling factor, \( \kappa \) is the subthreshold slope factor, \( V_{th} \) is the threshold voltage, and \( V_T \) is the thermal voltage. The input characteristic becomes

\[
I_{in} = I_0 e^{\frac{\kappa (V_{in} - V_{th})}{V_T}}
\]

The output characteristic including the effects of mismatch is given by

\[
I_{out} = (I_0 + \Delta I_0) e^{\frac{\kappa (V_{in} - V_{th} - \Delta V_{th})}{V_T}}
\]

The transfer function for \( I_{out}/I_{in} \) is given by

\[
\frac{I_{out}}{I_{in}} = \left(1 + \frac{\Delta I_0}{I_0}\right) e^{\frac{\kappa \alpha (V_{in} - V_{th})}{V_T}}
\]

The effects of mismatch for subthreshold operation in the saturation regime are shown in Fig (3), which is a \( \log I \) vs \( V \) plot. Whereas the voltage offsets arising from \( \Delta V_{th} \) are easily observed in Fig (3a), the errors introduced by \( \Delta I_0 \) are not as apparent as in the above threshold case. The horizontal shift is much smaller for the case of \( \Delta V_{th} \) and \( \Delta \kappa \) mismatch in Fig (3b), but the variation in gain becomes significant.

IV. MISMATCH COMPENSATION USING FLOATING GATES

A. Floating Gate Current Mirror

Floating gate transistors can be fabricated in any standard CMOS process. The gate of the transistor is isolated by an
electrically insulating oxide layer, and thus charge may be stored on the gate in a non-volatile manner. Any stored charge produces a voltage offset $V_{Corr}$ which adds in series with the externally applied control voltage $V_{in}$. The charge stored on the floating gate can be modulated using either impact-ionized hot electron injection to decrease the potential [6], [7], or Fowler-Nordheim tunneling to increase the potential [8]. Inputs may be applied through capacitive coupling to this floating node. The capacitive inputs may be implemented using any capacitor, including MOSCAPs, poly-poly capacitors, or other dielectric capacitors available in a particular technology. The only requirement is that there be minimal leakage current onto the floating node. It is sometimes convenient to implement the input coupling capacitor using a linear poly-poly capacitor which is available in many CMOS technologies. The floating gate current mirror is shown in Fig (4), where $V_x = V_{in} - V_{Corr}$.

![Fig. 4. Floating gate NMOS current mirror](image)

**B. Tuning for Mismatch Compensation**

Since mismatch is present in several parameters, ideally one must introduce corrections for each of these parameters. However, the use of floating gates allows for the tuning of only one parameter ($\Delta V_{th})$. We have found empirically that although this works well for weak inversion, in the case of strong inversion compensation results in the introduction of unanticipated gain variations. This is further explored in the following sections.

**C. Compensation in Strong Inversion**

When compensated, the output characteristic of the floating gate current mirror for above threshold becomes

$$I_{out} = (A + \Delta A)(V_{in} - V_{th} - \Delta V_{th} - V_{Corr})^2$$

(9)

where $V_{Corr}$ is the voltage stored across the capacitor. Setting $I_{out} - I_{in} = 0$ and solving for $V_{Corr}$ gives an expression for the required correction factor as a function of $A$, $\Delta A$, $I_{in}$, and $\Delta V_{th}$.

$$V_{Corr} = -\Delta V_{th} + \sqrt{I_{in}} \left( \frac{1}{\sqrt{A}} - \frac{1}{\sqrt{A + \Delta A}} \right)$$

(10)

Using a first order Taylor series expansion this can be approximated as

$$V_{Corr} \approx -\Delta V_{th} + \sqrt{I_{in}} \left( 1 + \frac{\Delta A}{2A} \right)$$

(11)

Once the correct value of $V_{Corr}$ is introduced for a particular operating point, the resultant $\sqrt{I}$ vs $V$ plots all pass though the bias point at which the correction factor was computed. This is shown in Fig (5) for curves that have been corrected at $V_{in} = 1.75$.

![Fig. 5. Mismatch correction for strong inversion](image)

Here we find that although floating gate MOSFETs allow for corrections to $\Delta V_{th}$ mismatch, the $\Delta A$ mismatch cannot be compensated in a similar manner by simply introducing an offset to the gate voltage. Furthermore, looking at Fig (5) it can be observed that although the characteristics all pass through the same bias point, there is a variation in slopes that causes them to diverge away from that bias point. Thus, compensation is best at a particular operating point and decreases in efficacy away from that point. What is not as obvious is that correcting for transconductance mismatch leads to an increase in gain variations.

This effect is quantified below in Fig (6). Here it can be seen that for a given value of $\Delta A$, correction of the threshold mismatch reduces gain variation (i.e., the standard deviation of the corrected gain is lower than the uncorrected gain). However, for a given value of $\Delta V_{th}$, correction of the transconductance mismatch increases the gain variations.

![Fig. 6. Standard deviation of gain for strong inversion](image)
D. Compensation in Weak Inversion

For subthreshold operation, the introduction of a floating gate at the output transistor gives the following output characteristic.

\[ I_{out} = (I_0 + \Delta I) \left( \frac{(\kappa + \Delta \kappa) V_{in} - V_{th} - \Delta V_{th} - V_{Corr}}{V_T} \right) \]  

(12)

Setting \( I_{out} - I_{in} = 0 \) and solving for \( V_{Corr} \) gives an expression for the required correction factor.

\[ V_{Corr} = \Delta \kappa V_{in} - \Delta V_{th} - U_T \ln \left( \frac{1}{1 + \frac{\Delta I_0}{I_0}} \right) \]  

(13)

Once the correct value of \( V_{Corr} \) is introduced for a particular operating point the resultant \( \log I \) vs \( V \) plot is shown in Fig (7). It can be observed from Fig (7a) that compensation nearly eliminates variations due only to \( \Delta I_0 \) and \( \Delta V_{th} \) mismatch. However, when \( \Delta \kappa \) mismatch occurs compensation only allows for matching at the operating point. Fig (7b) shows that since the floating gate compensation results in a shifted curve the effective gain at the operating point is altered. Fig (8) quantifies this result, where it can be seen that compensation in the presence of \( \Delta \kappa \) mismatch has significant effect on gain.

Fig. 7. Mismatch correction for weak inversion  
A: \( \Delta V_{th} \) and \( \Delta I_0 \) mismatch, B: \( \Delta \kappa \) and \( \Delta I_0 \) mismatch

Thus we find that \( I_0 \) and \( V_{th} \) mismatch are well compensated by the use of a floating gate, but that \( \kappa \) mismatch is poorly compensated and leads to gain variations.

V. Conclusion

Using analysis and simulation, we have shown that the use of floating gate transistors in CMOS current mirrors allows for adequate mismatch compensation in both weak and strong inversion for signals about a particular operating point. If the current mirrors are exercised over a wide dynamic range, this method compensates well for \( V_{th} \) mismatch and for \( I_0 \) mismatch in weak inversion, but fails to compensate for transconductance mismatch in strong inversion and for \( \kappa \) mismatch in weak inversion. We conclude that this technique overcomes the dominant sources of mismatch in weak inversion, and that its use in strong inversion suppresses mismatch but results in the introduction of gain errors.

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References