RAZAN: A High-Performance Switch Architecture For ATM Networks

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Summary

In this paper a high-performance packet switch architecture based on the improved logical neighbourhood (ILN) interconnection network, called RAZAN, is presented. RAZAN is an NxN multistage interconnection network (MIN) which consists of n stages, where n = log(2)N, of switching elements. Each stage consists of a column of N switching elements and (n + 1) x N links. Each switch has n + 1 inputs and n + 1 outputs. Every switching element j is connected to those n + 1 neighbouring switches in the next stage whose binary addresses differ by at most 1 bit from the binary address of switch j. The performance of RAZAN is evaluated both analytically and via simulation under uniform traffic load. The analytical and simulation performance evaluation results are compared. The performance of RAZAN is compared with a number of existing ATM switch architectures such as Benes, parallel banyan and Tagle networks. It is shown that RAZAN exhibits better performance in terms of both the rate of cell loss and throughput. This advantage of RAZAN over existing ATM switch architectures has been achieved at the expense of a moderate increase in switch complexity. In addition, an important characteristic which RAZAN possesses and which distinguishes it further from most existing ATM switch architectures is its ability to achieve very high throughput (higher than 80 per cent) in the presence of faulty switches and/or links. In this paper the fault tolerance characteristics of RAZAN are presented. However, space constraints do not allow us to present a detailed analysis of the fault tolerance and reliability features of RAZAN. These aspects are elaborated in a separate publication. (C) 1998 John Wiley & Sons, Ltd.
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