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A NOVEL MASH-KIND THIRD-ORDER ΣΔ CONVERTER STRUCTURE

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ABSTRACT

This paper presents a novel sigma-delta modulator architecture dedicated to very low-power applications wherein third-order noise shaping is achieved with very modest constraints on the analog part. The architecture is based on an enhanced MASH structure where the feedback of every loop is the sum of its output and of the output of the following loops.

The analytical model of the architecture is introduced and it is shown that the proposed architecture offers performance comparable to other third order cascaded sigma-delta modulator topologies with an analog part that is two times smaller than the one of a conventional MASH structure. Computer simulations confirm the theoretical calculations made with this structure.

The chip layout of a ultra low-power 16-bit audio D–A converter using this modulator is presented. The expected power consumption of the converter is only 125µW with a power supply of 1.8V.

1. INTRODUCTION

To realize high-resolution digital-to-analog conversion, sigma-delta converters using oversampling and quantization noise shaping techniques have demonstrated their suitability for integrated circuit technologies by balancing analog and digital complexity [1], [2]. The future reductions of feature geometry and power supply voltage in CMOS technology make possible the realization of very low power digital circuits. However this reduction offers little advantage for analog circuits regarding power consumption. Thus to obtain low-power high-resolution in future D-A converters, it is essential to minimize the analog part.

In sigma-delta modulators, oversampling and negative feedback are used to shape the spectrum of the quantization noise, moving most of the noise energy to frequencies above the signal baseband.

The dynamic range of sigma-delta modulators can be expanded by increasing the oversampling ratio and/or the order of the modulator. For low-power applications the clock frequency is limited to a few MHz, so the order has to be increased to achieve high resolution.

But these topologies are subject to stability problems for orders of modulation higher than 2. An alternative that overcomes this difficulty is the use of cascaded or MASH architectures [3]. The output signal of these modulators is composed from the outputs of different cascaded low-order modulators. As each stage is realized with a stable loop, the whole structure is inherently stable. But, as the output is a sum of the different branches, it is no longer single-bit, so the complexity of the analog part is increased.

The structure presented in this paper reduces the number of output levels of the sigma-delta modulator by keeping the same noise shaping characteristics and stability behavior as the MASH structure.

This paper is organized as follows. Section 2 describes the MASH topology. Section 3 introduces and analyzes the new ΣΔ structure with reduced number of output levels. Some results are presented in section 4. Section 5, finally, contains some concluding remarks and presents the chip layout of a 16-bit D–A converter using this modulator.

2. MASH STRUCTURE

The MASH structure uses cascaded first- and second-order sigma-delta modulators to achieve high-order noise shaping with at the same time avoiding any stability problems.

2.1 Basic MASH technology

The signal flowchart of a two-stage MASH 2-1 sigma-delta modulator with third-order noise shaping is shown in Fig. 1. The first stage is a second-order modulator and the quantization error noise of the first quantizer is shaped by a first-order modulator.

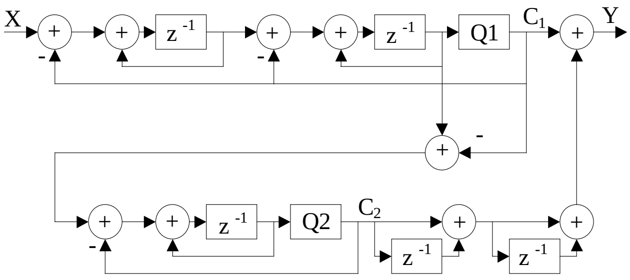

Fig. 1. Basic MASH 2-1 architecture.

The outputs of the first and second stages are given by

$$C_1 = X z^{-2} + (1 - z^{-1})^2 e_1 \qquad (1)$$

$$C_2 = - e_1 + (1 - z^{-1}) e_2 \qquad (2)$$

Where X is the input and e_1 and e_2 are the quantization error noises of the quantizer Q_1 and Q_2 respectively. Y, which is the two-stage MASH output, is obtained by summation of C_1 and the second-order differentiation of C_2.

$$Y = X z^{-2} + (1 - z^{-1})^3 e_2 \qquad (3)$$

Which is the same transfer function as for a conventional triple-integration sigma-delta modulator. The quantization error noise of the first quantizer is cancelled and the second one is shaped by a third-order function.

2.2 Number of output levels

The final output of the sigma-delta modulator is a combination of C_1 and C_2, which both oscillates between two levels (-1, +1). The second-order differentiation of C_2 gives an oscillation with 5 levels (-4, -2, 0, +2, +4).

So the final output of the sigma-delta modulator oscillates between 6 levels (-5, -3, -1, +1, +3, +5).

This shows a significant disadvantage of the MASH structure compared to the conventional modulators. Even with single-bit quantization in both branches of the modulator, the following DAC needs to have six levels, which demands much more constraints to the realization of the analog part as a sigma-delta modulator with single-bit output (whose DAC is always linear).

A main objective of developing a new MASH-kind structure was to reduce the number of output levels and in turn to continue minimizing the analog circuit complexity. All this by keeping the noise and stability characteristics of the MASH structure.

3. NOVEL ΣΔ STRUCTURE

This section presents a method to reduce the number of output levels in a MASH structure. This reduction is made by elimination of the differentiation on the second stage output. If this cancellation function is suppressed, the output of the second stage has to be subtracted from the input, so that the mean value of the output still tracks the input signal.

Hereafter, this structure will be referred to as TFM (Total Feedback MASH).

3.1 TFM 2-1 structure

This structure is derived from the MASH 2-1. The only difference is that the sum of C_1 and C_2 in negatively fed back and that there is no differentiation on the second stage, as shown in Fig. 2.

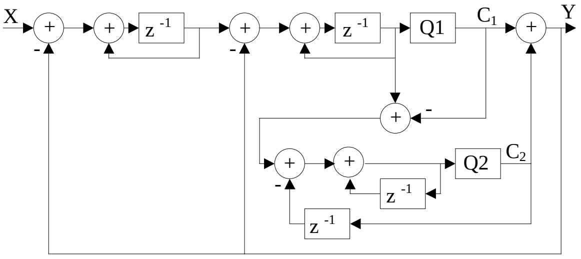

Fig. 2. TFM 2-1 ΣΔ structure.

The output of the first stage is given by

$$C_1 = X z^{-2} + e_1 - e_2 (1 - z^{-1})(2z^{-1} - z^{-2}) \qquad (4)$$

While the output of the second stage is the same as for the conventional MASH.

$$C_2 = - e_1 + (1 - z^{-1}) e_2 \qquad (5)$$

In this structure, the modulator output Y is obtained by simple summation of C_1 and C_2.

$$Y = X z^{-2} + (1 - z^{-1})^3 e_2 \qquad (6)$$

Which shows that the noise shaping is identically to the one of the MASH or the conventional structure.

3.2 TFM 1-1-1 structure

The third-order noise shaping can also be achieved by cascading three first-order modulators. The advantage of this structure compared to the 2-1 structure is the better behavior for full-scale amplitude signals.

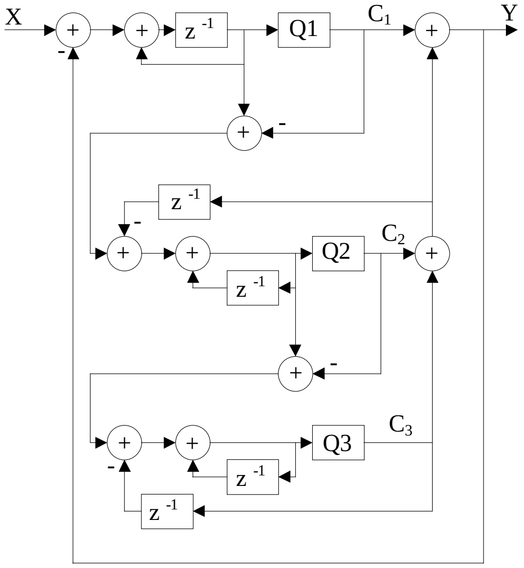

Fig. 3. TFM 1-1-1 ΣΔ structure.

The outputs of the three stages are given by

$$C_1 = z^{-1} X + e_1 - z^{-1} (1 - z^{-1})^2 e_3 \tag{7}$$

$$C_2 = - e_1 + e_2 - z^{-1} (1 - z^{-1}) e_3 \tag{8}$$

$$C_3 = - e_2 + (1 - z^{-1}) e_3 \tag{9}$$

So the sum of C_1, C_2 and C_3 is

$$Y = z^{-1} X + (1 - z^{-1})^3 e_3 \tag{10}$$

Again the quantization error noise is shaped by a third-order function and the error of the first two quantizers is cancelled.

3.3 Number of output levels

In the TFM 2-1 structure, the outputs of the first and second stage oscillate between two levels (-1, +1). So that the final output of the modulator has three levels (-2, 0, +2). Compared to the conventional MASH 2-1 structure, the number of levels and with this the complexity of the DAC has been reduced by a factor of two. The in-band quantization noise stayed the same because there is still a single-bit quantization with equally-amplitude input shaped with a third-order function.

For the TFM 1-1-1 structure, the output oscillates between 4 levels (-3, -1, +1, +3). Again the number of output levels was reduced by a factor of two compared to the MASH 1-1-1 structure whose output has eight levels.

3.4 Low-power considerations

The TFM structure is well suited for high-resolution low-power converters. All multiplying coefficients in the feedback loops can be taken as power of two. So there is no multiplication at high frequency with large signal word length.

The analog part is much smaller than with a conventional MASH structure.

4. RESULTS

The following simulation results have been generated using Matlab. The frequency of the input sine wave was 4 kHz sampled with a Nyquist rate of 50 kHz and an oversampling ratio of 64, so the modulator working frequency was 3.2 MHz.

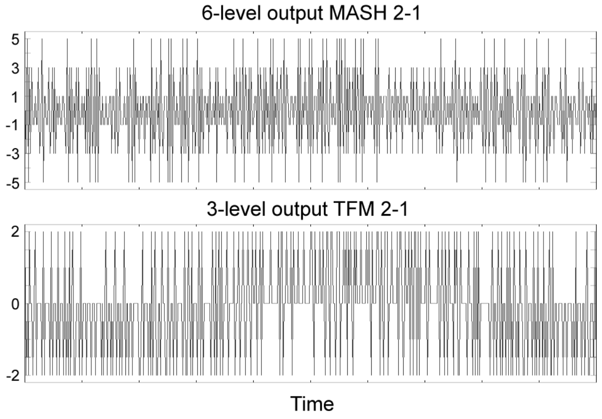

Fig. 4. Output signals of the MASH 2-1 and of the TFM 2-1 structure for a 4kHz sine wave input with -6dB amplitude.

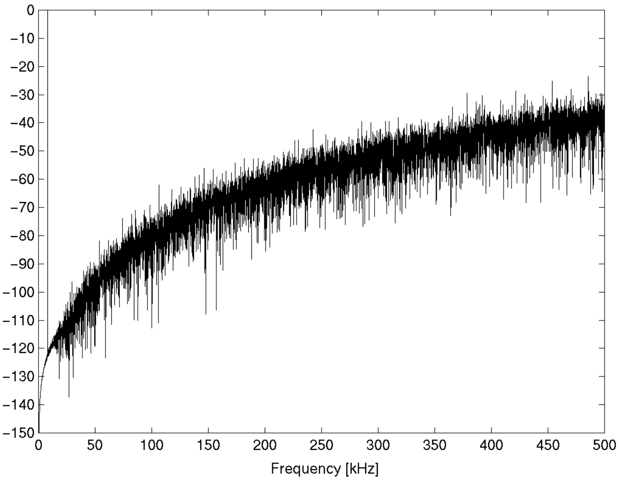

Fig. 5. Normalized power spectral density for a –6dB 8kHz sine wave.

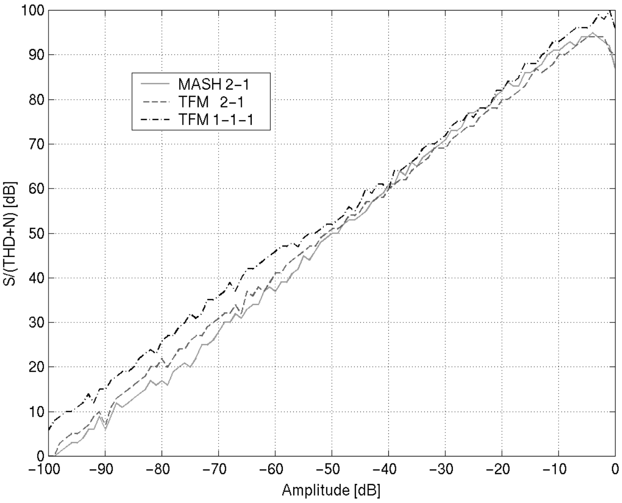

Fig. 6. S/(THD+N) versus amplitude for the TFM and for the conventional MASH.

The TFM 1-1-1 and TFM 2-1 modulator achieved a dynamic range of 104dB and 98dB respectively and a peak SNR of 100dB and 95dB.

These results show that this structure, working with an OSR of 64, can be used for a D-A converter with at least 16 bit of resolution.

Despite the TFM 1-1-1 structure has the better S/(THD+N) ratio than the TFM 2-1 modulator, the TFM 2-1 structure is preferable because it has less levels than the first structure. For the realization of a converter, the 3-level D-A converter can comfortably be obtained using only one differential amplifier and two switches.

To convert the high and low values the positive or the negative input of the amplifier is connected to V_{ref} and the other to ground. To convert a “0” the two inputs are shorted.

With this converter it is possible to achieve almost perfect linearity.

5. CONCLUSIONS

A new MASH-kind sigma-delta modulator structure using third-order noise shaping has been presented. This architecture has the same transfer function and stability behavior as a conventional MASH structure.

The advantage is the number of output levels, which is reduced by a factor of two by keeping almost the same signal-to-noise ratio. This structure continues to simplify the analog part.

This TFM sigma-delta modulator has been used to design a 16-bit digital-to-analog audio converter operating at a supply voltage of 1.8V. The layout has been realized in a 0.25µm CMOS technology with one polysilicon and six metal layers. The modulator occupies a chip area of 0.21mm^2 and the expected power consumption is less than 75µW for 25kHz bandwidth using an OSR of 64.

Fig. 7 shows the layout of this converter using the TFM 2-1 structure. For a further reduction of the clock frequency, this realization uses multi-bit quantizers. A major part of the digital chip area is occupied by the interpolation filter and test structures.

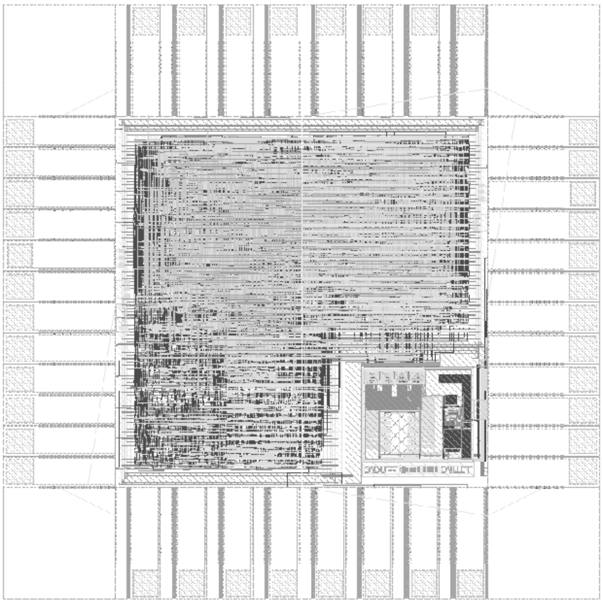

Fig. 7. Chip layout

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