A Fast-Locked Bang-Bang All-Digital Phased-Locked Loop Using Successive-Approximation Frequency-Search Algorithm

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Digital system such as system-on-chip microprocessor generally requires Phased-Locked Loop (PLL) for clock generation. However, traditional analog PLL typically contains several important components not included in a standard cell library, such as resistor and low leakage capacitor, which makes it difficult to integrate into a digital system. In addition, its performance is limited by process, voltage, and temperature variation.

In recent years, the benefits from technology scaling have enabled the implementation of all-digital phase-locked loop (ADPLL). Many different approaches on ADPLL have been proposed for clock generation. In [1], high-resolution time-to-digital converters (TDC) have been integrated in ADPLL to replace the analog charge pump; however, the resolution is limited by the delay of single inverter. Although Vernier delay line [2] time-to-digital converter has been proposed and the resolution is reduced to around several picoseconds, such design is challenged by its complexity and power consumption.

In order to alleviate the resolution requirement of conventional TDC-based ADPLL, bang-bang ADPLLs have become popular. However, such architecture suffers from long settling time and may cause stability problem if the output frequency is far from the center frequency [3]. Therefore, conventional bang-bang ADPLL generally has both proportional path and a low-gain integral path, such as [4]; whereas, the integral path adjusts the frequency and phase error when the system is far from lock, similar to a charge pump in analog PLL. When these errors are small, the change due to proportional path is much larger than that of integral path, and the system behaves as first-order bang-bang PLL. However, the low integral gain limits the bandwidth and results in a long settling time.

Thus, several techniques have been proposed to reduce the locked time of bang-bang ADPLL. In [5], the bandwidth of the system is adaptively self-adjusted. A large proportional gain is used initially to settle the phase and frequency error to a smaller value and then a small gain is used for fine resolution. In [6], when the phase error is larger than a certain amount, the integral path dominates to achieve fast lock. However, in all above techniques, the PLL settling time strongly relies on the bandwidth of the system and still needs thousands of cycles to settle.

Thus, this work proposes a novel successive approximation frequency-search algorithm to not only center the starting frequency of digitally controlled oscillator (DCO) on the desired frequency but also align the phase of the output clock to that of the reference clock. In this algorithm, the settling mainly depends on the DCO control bits instead of the bandwidth of the system. Therefore, fast-lock can be achieved despite of a low bandwidth system. Moreover, in this work, a novel binary-encoded DCO is also proposed to reduce its power consumption.

References


