Physical degradation of GaN HEMT devices under high drain bias reliability testing

S.Y. Park, Carlo Floresca, Utiya Chowdhury, Jose L. Jimenez, Cathy Lee, Edward Beam, Paul Saunier, Tony Balistreri, Moon J. Kim

Abstract

The AlGaN/GaN heterostructure HEMTs were epitaxially grown using MOCVD on semi-insulating SiC substrates. Standard III-V commercial production processing technology was used to fabricate the devices, which were then subjected to stress under accelerated DC life-tests with base-plate temperatures of 82, 112, and 142 °C. Drain bias of 40 V and time-zero drain current of 250 mA/mm were applied. TEM samples were prepared via the lift-out technique using a focused ion beam (FIB). TEM analysis revealed that electrically degraded devices always contain a pit-like defect next to the drain in the top AlGaN layer. It has been found that the degree of the defect formation strongly correlates to drain current (I_Dmax) degradation.

1. Introduction

The AlGaN/GaN heterostructure is a promising candidate as a High-Electron Mobility Transistor (HEMT) device material system due to its wide band gap, superior carrier saturation velocity, thermal conductivity, and high breakdown field all of which are required for high temperature and high speed applications such as cell phone base stations and RADAR [1–4]. Most research for HEMTs have focused on understanding and improving the performance, structure, and fabrication processes of the devices. Recently, an extremely high output power of 900 W and high power added efficiency (PAE) of 75% has been reported [3]. By aid of improved material design and process control, the operation voltage has increased from 12 to 24 V to approximately 48 V. These improved properties of AlGaN/GaN devices put them at the forefront of commercial market acceptance.

Excellent performance of GaN devices can be obtained routinely. However, achieving acceptable reliability and stability under continuous performance operations is still needed for the commercialization. While several researchers have reported a stable operation life of more than 10^5 h, these results are limited to high drain biases and high frequency conditions should be ensured for use in applications of high performance devices and monolithic microwave integrated circuits (MMICs). Improvement in reliability requires a better understanding of the failure features and mechanisms. Physical changes, which can explain electrical degradation, have not been clearly revealed. In this study, AlGaN/GaN HEMT devices were life-tested under high drain bias of 40 V and high resolution transmission electron microscope (HRTEM) analysis was conducted to find microstructural changes after the reliability tests. This results in the elucidation of the correlation between those changes and the degradation of electrical properties.

2. Experimental

The HEMTs' heterostructure, a 3 nm GaN cap/16 nm Al_{0.28}Ga_{0.72}N/1 nm AlN barrier/thick GaN buffer layer, was epitaxially grown on semi-insulating SiC substrates using MOCVD. A Pt/Au metal gate 0.25 μm in length was deposited via evaporation. Standard III-V commercial production processing technology by TriQuint Semiconductor was used to fabricate the devices. A SiN passivation and air-bridge was used to connect the source pads. A total gate width of 400 μm periphery was assembled into package.

For the accelerated DC life-tests, the devices were subjected to stress under base-plate temperatures of 82, 112, and 142 °C, which corresponds to channel temperatures of 250, 285, and 320 °C, respectively, as estimated by device modeling. A drain bias of 40 V and a time-zero drain current of 250 mA/mm was applied for a duration time of 1000 h. Variations of drain current (I_D) and gate current (I_G) was recorded during tests. Every hour the stress was turned off and the drain and gate current, I_Dmax and I_Gmax respectively, were measured under a 5 V drain bias and 1 V gate bias. Failure was defined as I_Dmax drop more than 10%.

Cross sectional transmission electron microscope (TEM) samples from over 65 devices were prepared via the lift-out technique using a focused ion beam (FIB, FEI Nova200). All the samples were fabricated from the center of the gate finger (Fig. 1). In an effort to...
ensure that the samples being analyzed represented the device defects in whole, 10 TEM lamina were made along a single gate. In the same device, another gate was sampled in the center which confirmed that the gates in the same device degraded similarly with respective pit sizes of similar size as shown in Fig. 1c. Cross sectional HRTEM and high angle annual dark field (HAADF) image observations were conducted and correlated with the electrical degradation by using a field emission TEM and scanning TEM (STEM). A nano beam energy dispersive X-ray (EDX) technique was also used for the chemical analysis of the degraded area.

3. Results and discussion

The fabricated devices have flat interfaces between the Pt/Au gate and the AlGaN layer as shown in Fig. 2. It is confirmed that the AlGaN and GaN cap layers were well epitaxially grown without any defects. Fig. 3 shows the typical degradation of electrical properties during the tests where drain current ($I_{DQ}$) decreases continuously. We found that prominently degraded properties were $I_{D\text{max}}$ drop up to 70% and threshold voltage shift of 0.6 V in the positive direction, while this amount is significantly varying depending on specimens. The decrease of $I_{D\text{max}}$ was used as a barometer to describe the degree of electrical degradation.

TEM analysis revealed that electrically degraded devices always contain a pit/crack shaped defect at the gate edge in the top AlGaN layer, as shown in Fig. 4. In the cases where devices showed little

![Fig. 1. Micrographs showing the FIB sample preparation method; (a) typical sample preparation at the center of gate finger, (b) thinned TEM sample attached on a grid, and (c) 10 TEM lamina made along the gate finger.](image)

![Fig. 2. Cross sectional TEM images of the as-fabricated device.](image)

![Fig. 3. Evolution of drain current ($I_{DQ}$) during the reliability test under a 40 V drain bias and maximum drain current ($I_{D\text{max}}$) recorded every hour under a 5 V drain bias and 1 V gate bias.](image)
degradation, a shallow pit is observed only in the drain side. On the other hand, severely degraded devices always have a large pit in the drain side and occasionally a small pit in source side. The fact that the defects mainly form under the drain next to the gate was expected since all the phenomena, such as temperature increases, strain development, and carrier traps are concentrated on the drain side [6–8].

It is observed that the degree of physical damage strongly correlates to the drain current ($I_{D_{\text{max}}}$) degradation. The device which was stressed for 45 h shows a pit 3 nm deep and 11 nm wide (Fig. 4a). The $I_{D_{\text{max}}}$ value of this device dropped 19% during the life-test. The device stressed for 240 h (Fig. 4b) contains a larger pit, 6 nm deep and 13 nm wide, as well as a crack propagating from the bottom of the pit to the interface between the AlGaN/GaN. The $I_{D_{\text{max}}}$ in this device dropped 58%. It is confirmed through imaging and electrical results of over 65 stressed devices that the electrical degradation is mainly due to the formation of physical defects.

One drawback of TEM analysis is that the extremely localized observation area hardly represents the overall features of the devices. In order to compensate for this drawback, multiple along the gate finger were observed in selected devices (Fig. 1). Through observation, it is confirmed that the center of the gate finger represents the whole device. The small pit observed at the center of the gate finger was also seen in all the sections along the gate finger (Fig. 5). The sections prepared from the next finger in the same device showed very similar pit sizes. Although some of the more abruptly degrading devices have different defect sizes, defects formed at the finger center are always larger than those created at the edge of the gate finger as shown in Fig. 5. The center of the gate finger is the area that suffers the highest joule heating temperature since it has the lowest cooling efficiency geometrically. It is thought that the small pit shaped defect forms uniformly throughout the device showing stable operation and gradual degradation, while abrupt defects form first at the center of the gate finger and expands to the other gate regions. It is concluded that TEM observation at the center of the gate finger can represent the physical features of the device. In order to quantify the amount of physical degradation, observation at the center was used.

Fig. 4. TEM images of defects formed in the drain side after the reliability tests; $I_{D_{\text{max}}}$ drops of (a) and (b) was 19% and 58%, respectively.

Fig. 5. TEM images showing the variation of defect sizes at the center and near the edge along the gate finger; (a) and (b) are images from the same finger, but in different positions. (c) and (d) are images from the same positions as (a) and (b), but on a finger from a different device.
The physical degradations based on the TEM images of 20 devices were classified into six grades using the double blind method, the persons grading physical degradation have not given any electrical data, as described in our previous report [9]. We used the term ‘disfiguration factor’ to describe the physical degradation. Fig. 6 shows how these devices were classified. Factor 0 was marked by little to no damage while Factor 6 classification described damage over the entire AlGaN layer. The sample that contained a crack only reaching the GaN interface was classified as Factor 4. The results were plotted with the $I_{\text{Dmax}}$ percentage drop. A monotonic dependence between the electrical degradation and amount of physical damage was clearly demonstrated. In the regime of high power and high drain bias (40 V), the physical degradation is regarded as the reason for degrading electrical performance of AlGaN/GaN HEMT devices.

The defect types observed in stressed devices were single pits, cracks, or a combination of both. It is not clear which defect forms first in the samples where they are both observed since pits and the cracks have been observed without the presence of the other. It is noted that all of the devices that contained a crack showed significant $I_{\text{Dmax}}$ drops. It is believed that the pit formation induces gradual performance degradation while the crack formation is responsible for abrupt failures of the HEMT devices.

We found that the life time of the device is very divergent. In order to see this tendency clearly we tested 10 devices that were fabricated by the same process on the same wafer. After 6 h of testing, the most degraded and the least degraded samples were taken out of the test box to have their cross sectional microstructure observed. In the same way, two samples were removed from the test at 18 h, 45 h, 4 days, and 12 days. Fig. 7 shows the defects formed in the most degraded device after 6 h and the least degraded device after 12 days. The degree of physical defect formation was not proportional to the test time. Although these devices were fabricated at the same time by identical processes on the same wafer, the life time of each device revealed an extremely high deviation. Considering the fact that this test was an accelerated one, the divergence tendency was very prominent. The cause for these divergent life times is still under investigation.

In order to understand defect formation, nano beam EDX technique was applied at and away from the defect area (Fig. 8). The Cu peak in the figure is from the surrounding Cu TEM grid. The corrosive element, which can remain from etching and expedite degradation during device operation, was not detected. It is noteworthy that more Si, O, and C are detected in the defect area than on the pristine AlGaN layer. The cavity formed during degradation was filled with SiN$_x$ passivation material. The fact that the passivation layer flowed into the cavity and oxidation occurred implies that high temperature by joule heating is involved in this failure.

Several degradation mechanisms for HEMT devices have been reported. Those mechanisms explain electrical degradation in the relatively low drain bias regime. However, the physical damage observed in this experiment such as pits and/or cracks cannot be sufficiently supported by these mechanisms. Only the presence of a vertical crack can be supported by the inverse piezoelectric

Fig. 6. TEM images showing how disfiguration factors 0–6 were determined, and a plot showing correlation between disfiguration factor and $I_{\text{Dmax}}$. Scale bar in the images is 10 nm.

Please cite this article in press as: Park SY et al. Physical degradation of GaN HEMT devices under high drain bias reliability testing. Microelectron Reliab (2009), doi:10.1016/j.microrel.2009.02.015
effect [10]. It is known that AlGaN layer grown on GaN has a
tensile in-plane misfit strain [11]. In addition, applied voltage in
the AlGaN/GaN HEMTs causes the greatest amount of inverse
piezoelectric strain/stress near the gate edge on the device [8]. It
is thought that accumulated in-plane stress by the combination
of the misfit strain and the inverse piezoelectric effect is partly
responsible for physical degradation of devices. On the other hand,
the formation of pits is hardly explained by any of these mecha-
nisms. Therefore better understanding of the physical degradation
is required to improve the reliability of GaN HEMT under high bias
voltages.

4. Conclusions

Microstructures of production-quality AlGaN/GaN HEMT de-
vices have been investigated after accelerated life-tests under high
drain bias of 40 V. Physical defects, such as pits and cracks, under
the drain next to the gate were observed in the electrically
degraded devices. The degree of these defects formation strongly
correlates to drain current (I_Dmax) degradation. It was found that
the life time of devices fabricated via identical processes showed
sample-to-sample variation in a given wafer. Although the forma-
tion of physical defects is not fully understood, the observation
indicates that mechanical stress is involved in this failure.

Acknowledgements

This work was supported in part by the US Defense Advanced
Research Project Agency and Army Research Laboratory, ARL Con-
tract No. W911QX-05-C-0087.

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Microelectron Reliab 2003;43:1705.
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