International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020

A Single PV Source based 17 Levels Module for Multilevel Inverter

Jayalekshmi O B
PG Scholar
Government Engineering College, Barton Hill
Thiruvananthapuram, Kerala, India

Prof. Raji Krishna
Assistant Professor
Dept. of EEE
Government Engineering College Barton Hill
Thiruvananthapuram, Kerala, India

Abstract:- **Multilevel inverter plays an important role in the field of modern power electronics and is widely being used for many high voltage and high power industrial and commercial applications. It has many advantages compared to conventional two-level inverters such as high dc-link voltages, reduced harmonic distortion, fewer voltage stresses, and low electromagnetic interferences. However, for higher-level operation, it has some major disadvantages such as the use of higher number of voltage sources and power switches, voltage balancing issues, and complex pulse width modulation control. Implementing asymmetrical multilevel inverter topology uses minimum switching components to generate higher levels as compared with other conventional topologies. 17 level multilevel inverter using reduced switching components is proposed in this paper. A single DC source with a front end flyback converter is proposed to facilitate the reduction of required dc sources to a single source and thereby it can be developed as a single PV source-based multilevel inverter. The front end flyback converter is used to provide the input for asymmetrical multilevel inverter(which requires unequal DC sources). The simulation results are presented to validate the approach.**

Keywords: 17 level, Flyback converter, Asymmetrical sources, Switched capacitors

1. INTRODUCTION

DC to AC power conversion is a prime factor in the modern authoring of generation, transmission, distribution and utilization of electric power. DC to AC power converters plays a very important role in variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, static var compensators, active filters, flexible AC transmission systems and DC power source utilization (such as electricity obtained from batteries, solar panels or fuel cells) [1,2]. The different

advantages of multilevel inverters include lower switching frequency, lower switching losses, lower peak inverse voltage, smaller common mode voltage, lower harmonic distortion, less electromagnetic interference and high voltage capability. The three main conventional multilevel inverter topologies are diode clamped or neutral point clamped, flying capacitor and cascaded H-bridge with independent DC sources. A high power rating can be achieved by the multilevel inverter. Various resources such as photovoltaic, battery and fuel cells can be used as a DC source, which can be easily interfaced for high power and medium voltage application. In diode clamped inverter, large numbers of clamping diodes are required and regulating the capacitor voltages makes the control method more complex. In a flying capacitor inverter, the size of the inverter is increased because of the requirement of more capacitors to achieve higher levels. Small output filters are used at the output of multilevel inverters for high power applications. Bulky transformers and complex peripheral reset circuits make the solution non-feasible for applications such as electric vehicles. As a solution to this problem high-frequency links with a single input or multiple outputs are used to feed the inverter as proposed in [12-14].

To achieve higher output voltage levels, it requires a greater number of individual DC voltage sources for each module and semiconductor devices which increase the number gate drive circuit [6]. To overcome these drawbacks, different topologies of multilevel inverters and modified pulse width modulation (PWM) methods have been developed in recent years [2]. The PWM methods for multilevel inverters help to achieve the following objectives: easy implementation, reduced switching loss and minimum total harmonic distortion. The most widely used PWM techniques for multilevel inverters are the carrier-based PWM techniques, selective harmonic elimination PWM (SHE-PWM) techniques and the space vector based PWM techniques [4]. Different topologies of a transformer with fewer inverters are proposed to improve efficiency and reduce current leakage. Lately, different topologies of multilevel inverters with reduced components have been developed [1].

These inverter topologies may be symmetric or asymmetric. However, these topologies do not considerably reduce power switches. Hence, a new topology with a reduced number of switching devices and voltage sources is proposed in this paper. Unlike the previously mentioned topologies, the proposed inverter topology reduces the total number of switches in the conduction path, which in turn minimizes the switching losses.

In this paper, a modified multilevel asymmetric inverter topology with a reduced number of power switches is proposed. The proposed inverter uses only a single DC voltage source and eleven switches to generate 17-level

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020

output voltage during asymmetric mode of operation. An asymmetric multilevel module is introduced to produces 8 positive levels, 8 negative levels and zero level (totally 17 levels) without any additional circuit to create negative voltage levels [5,6]. The module can be connected in series as cascade connection easily to produce more and higher output voltage levels [15]. The different modes of operation of the proposed 17-level inverter are explained in Section 2. Section 3 includes the comparative study of the proposed topology and other existing topology which is closer in configuration with the proposed system. Section 3 also discusses the different methods of calculating the simulation results obtained using MATLAB/Simulink.

2. OPERATING PRINCIPLE OF PROPOSED MULTILEVEL INVERTER

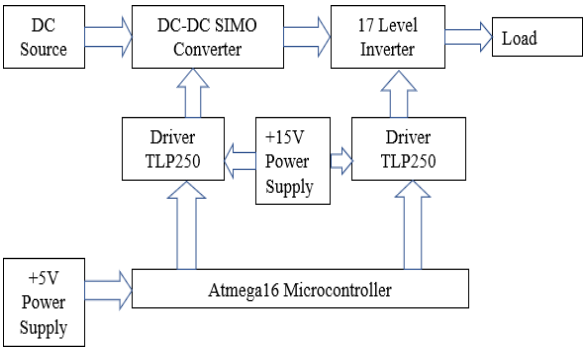


Figure 1: Block Diagram

The first block in Figure 1 shows a dc source (PV) to supply the converter. The output dc voltage of the cell is then fed to the DC-DC front end flyback converter to boost the DC output. The boosted output is then fed to the proposed converter whose output is stepped voltage (near sinusoidal) and it is then fed to the utility grid.

But for the DC-DC flyback converter, a driver circuit is required which requires a power supply of +12V. Similarly, the converter also requires a driver circuit that needs a +12V power supply. Hence a +12V power supply is required and it is placed in between the 2 driver circuits.

Atmega16 microcontroller is also required in order to control the power electronic switches, which is provided with the power supply of +5V.

A. Circuit Diagram

The dc output from the PV cell is fed to the flyback converter. When the switch is closed, it induces a voltage on the secondary windings. V2 voltage is induced in the first secondary windings while 3V2 is induced in the next two secondary windings Figure 2. The voltage induced is of negative polarity. Hence the diode becomes negatively biased. Here since the capacitor is pre-charged, it supplies power to the load. Since the power is supplied by the capacitor, charge on the capacitor decreases. When the switch is kept open, the voltage of positive polarity is induced in the windings. Hence the diode becomes forward biased and power to the load is supplied by it.

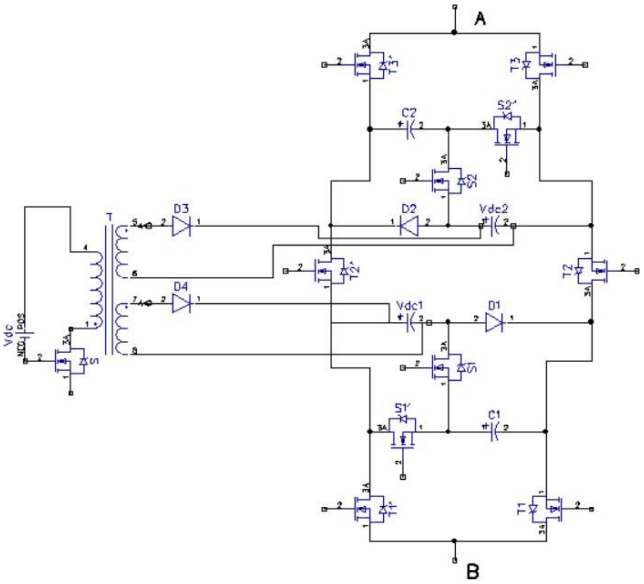


Figure 2: Circuit diagram of the proposed 17 level inverter

B. MODES OF OPERATION

The proposed MLI uses a single input multiple output front end flyback converter. The flyback converter is operated by using a single dc source. The duty ratio of the switch Q is selected according to the output voltages

Needed. The transformer windings also depend on the load voltages. The operation of the proposed MLI is illustrated in the Table 1. The logic 1 is considered as the ON state and logic 0 is considered as the OFF state of the switch.

The basic units can be connected in series to form cascade structure so as to generate more levels of output voltage and the output of each basic unit can be added together to obtain a greater output voltage [6].

Table 1: Modes of operation

Switching States	T1	T1'	T2	T2'	T3	T3'	S1	S1'	S2	S2'	OUTPUT VOLTAGE
1	0	1	1	0	0	1	1	0	1	0	4Vdc + VC1 +VC2 = 8Vdc
2	0	1	1	0	0	1	0	1	1	0	4Vdc +VC2 = 7Vdc
3	1	0	1	0	0	1	0	1	1	0	3Vdc +VC2 = 6Vdc
4	0	1	1	0	0	1	1	0	0	1	4Vdc +VC1 = 5dc
5	0	1	1	0	0	1	1	0	0	1	4Vdc
6	1	0	1	0	0	1	0	1	0	1	3Vdc
7	0	1	1	0	1	0	1	0	0	1	Vdc +VC1 = 2Vdc

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020

8	0	1	1	0	1	0	0	1	0	1	Vdc
9	1	0	1	0	1	0	0	1	0	1	0
10	1	0	0	1	0	1	0	1	0	1	-Vdc
11	1	0	0	1	0	1	1	0	0	1	-Vdc -Vdc = -2Vdc
12	0	1	0	1	1	0	0	1	0	1	-3Vdc
13	1	0	0	1	1	0	0	1	0	1	-4Vdc
14	1	0	0	1	1	0	1	0	0	1	-4Vdc -VC1 = -5Vdc
15	0	1	0	1	1	0	0	1	1	0	-3Vdc -VC2 = -6Vdc
16	1	0	0	1	1	0	0	1	1	0	-4Vdc -VC2 = -7Vdc
17	1	0	0	1	1	0	1	0	1	0	4Vdc - VC1 -VC2 = -8Vdc

3. SIMULATION USING MATLAB : RESULTS AND DISCUSSION

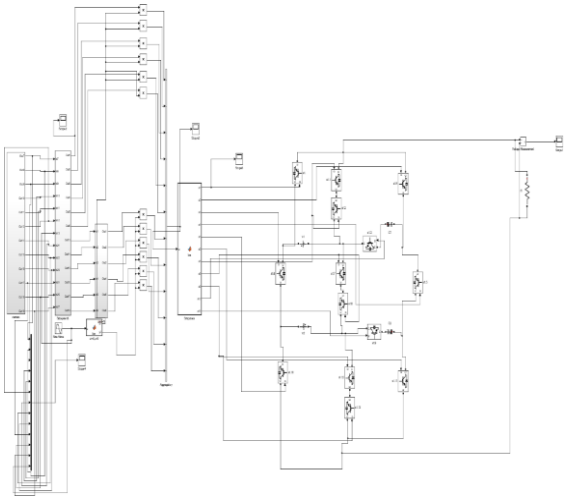


Fig 3: Simulink diagram of proposed 17 level inverter

Simulation results of the proposed inverter for 17 levels are presented using MATLAB / Simulink. Since the MOSFET switches have the fastest switching capability, it is used here. The load used for the multilevel inverter is R load. The MATLAB simulation circuit for the proposed MLI is shown in Fig 3. It takes only eleven MOSFET switches for producing I7 level output voltage. The R load is used for the simulation purpose. The simulation results show that the circuit is functioning properly. The output waveform has 8 levels in the positive section, 8 levels in the negative section and a zero level, in total 17 levels. Thus the proposed multilevel inverter is successfully simulated.

A. Modulation technique

The multilevel converters can be controlled by using different modulation schemes. For this topology, a multi-carrier PWM technique is adopted [6,7]. The carrier-based PWM technique was used to generate the switching pulses for the MLI. In this technique, the sinusoidal reference signal is compared with the triangular carrier waveform. In this topology phase, opposition disposition sinusoidal PWM (PODSPWM) is adopted for its simplicity and all the carrier waveforms were in phase with each other. The pulses obtained are used for switching the MLI corresponding to the respective voltage levels. Figure 4 shows the switching signals generated by PODSPWM technique. Atmega16microcontroller is used here to control the inverter switches.

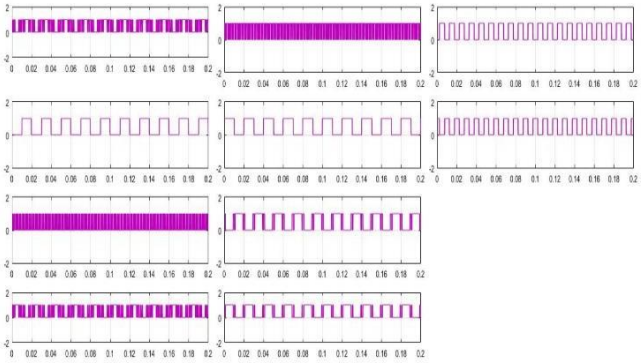


Fig 4: Switching signals for switches

In this modulation technique sinusoidal waveform is compared with all the 17 carrier waveform. For all the carrier waveforms above the time-axis, the results of comparison with the reference sine wave are 1 or 0. For all the carrier waves below the time-axis, the results of comparison with the reference sine wave are 0 or -1. The aggregated signal has the same number of output levels as desired in the output waveform. The switching signals are derived from this and by comparing the signal with the desired level using the lookup table and the output is fed to the switches of MLI. The lookup table is generated by using the switching states of the 17-level inverter.

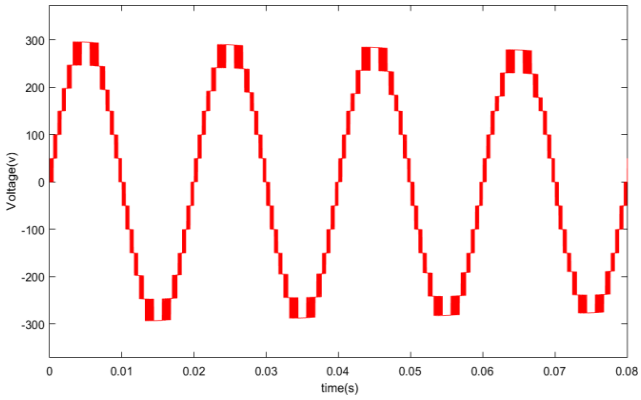


Figure 5:13 level output from[3]

Figure 5 shows the inverter output of [3] where the output voltage is 300V and the number of levels actually obtained in their work was 13.

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020

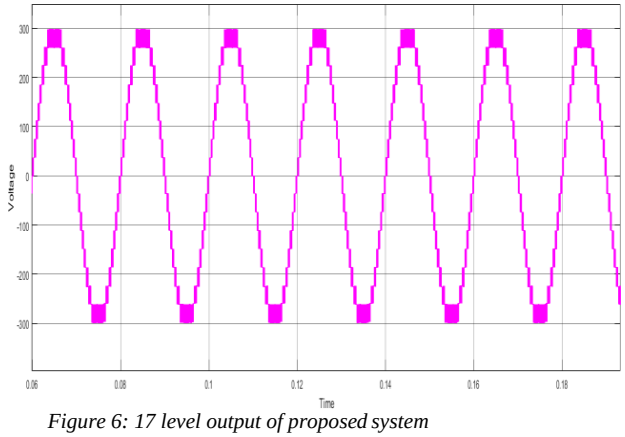


Figure 6: 17 level output of proposed system

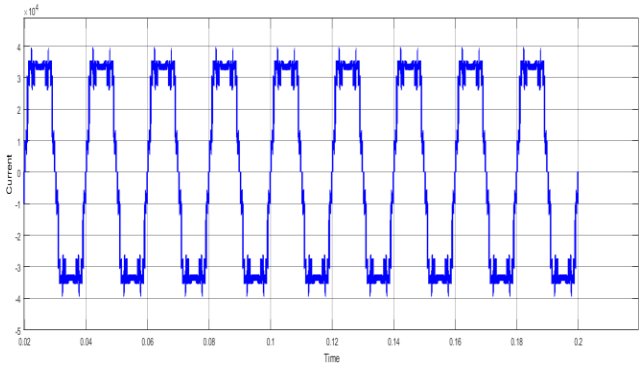


Figure 7: Output current from proposed topology

The 17 level output voltage and the output current obtained in the proposed system is shown in Figure 6 and 7. The maximum output voltage obtained in this structure is the sum of the load voltages of the multi-output flyback converter (input voltage to the inverter section). Figure 8 shows the output voltages from the flyback converter to the two bridges where V_{aux2} : V_{aux1} are in the ratio 1:3.

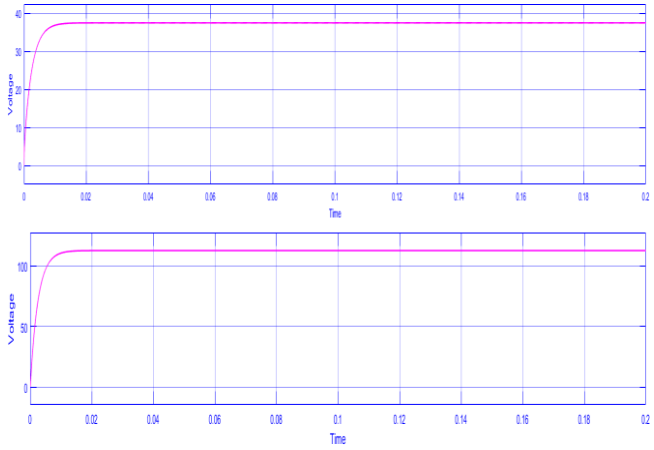
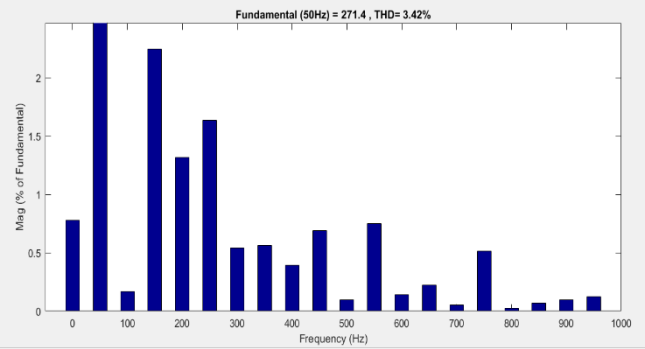


Figure 8: Output voltages obtained from flyback converter

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020



The resulting total harmonic distortion of the proposed structure is shown in Figure 16. The THD of this structure is 3.42%. The total harmonic distortion is very less compared to conventional type multilevel inverters.

B. Comparative study

The proposed multilevel inverter module aims to get maximum levels from a minimum number of DC sources and other power electronic components. Regarding this issue, there are few configurations with minimum switching components to compare, rarely. The proposed system is got compared with one such configuration [3]. The proposed system uses only a single DC source and 11 switches to generate 17 level output voltage while the other configuration used two DC sources and 14 switches to generate 13 level output voltage. The Total Harmonic Distortion obtained in the proposed inverter is far better when compared with the considered configuration. Table II shows the result comparison of the proposed system and [3].

Table II: Result comparison of proposed system and [3]

	[3]	**PROPOSED**
Number of switches	14	11
Number of dc sources	2	1
THD	7.75%	3.42%
Input Voltage	V_1=50V V_2=100V	V_1=37.5V V_2=112.5V
Inverter Output	300 V	300V
Number of levels of output voltage	13	17

4. CONCLUSION

An asymmetrical single DC source-based multilevel inverter has been proposed in this paper. The proposal involves the least number of switches and a 17 level voltage waveform is obtained. The main advantage of this inverter topology is that it uses only a single DC source and eleven main switches to achieve 17 level output voltage during the asymmetric mode of operation. Overall THD is very low when compared to previous topologies and thus the quality of output waveform is of improved quality. Due to the use of a fewer number of switches, optimized circuit layout and packaging is possible, less cost is required to implement the proposed inverter. A comparative analysis is done and it is found that the proposed topology is more efficient. This topology can be successfully installed for solar-based AC applications, SMPS and for any industrial applications.

REFERENCES

[1] E. Samadaei, S. A. Gholamian, A. Sheikholeslami and J. Adabi, "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7148-7156, Nov. 2016.

[2] V Thyagarajan,Somasundaram P, "Simulation of New Symmetric and Asymmetric Multilevel Inverter Topology with Reduced Number of Switches," in *IEEE Transactions On Industrial Electronics*,Vol. 62, No.1,Jan 2018, p.256-269.

[3] E. Samadaei, M. Kaviani, K. Bertilsson , "A 13-levels Module (K-Type) with two DC sources for Multilevel Inverters," in *IEEE Transactions on Industrial Electronics*,Vol. 34, No.1, March 2018, p. 211-220.

[4] Elyas Zamiri, Naser Vosoughi, Seyed Hossein Hosseini, Member, IEEE, Reza Barzegarkhoo and Mehran Sabahi, "A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series-Parallel Conversion with Less Number of Components"in *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 324–341, Jun. 2012

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 06, June-2020

[5] M. D.Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, Jun. 2000.

[6] S. K. Chattopadhyay and C. Chakraborty, "Performance of three-phase asymmetric cascaded bridge (16 : 4 : 1) multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 5983–5992, Oct. 2015.

[7] A. Taghvaie, J. Adabi and M. Rezanejad, "A Multilevel Inverter Structure Based on a Combination of Switched-Capacitors and DC Sources," in *IEEE Transactions on Industrial Informatics*, vol. 13, no. 5, pp. 2162-2171, Oct. 2017.

[8] P. Flores, J. Dixon, M. Ortuzar, R. Carmi, P. Barriuso, and L. Moran, "Static VAR compensator and active power filter with power injection capability, using 27- level inverters and photovoltaic cells," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 130–138, Jan. 2009.

[9] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "An effective control method for three-phase quasi-z-source cascaded multilevel inverter based grid-tied photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6794–6802, Dec. 2014.

[10] K.K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," in *IET Power Electronics*, Volume 5, Issue 4,pp. 435-446,April 2012.

[11] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655-664, Mar./Apr. 2005.

[12] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one dc source in asymmetric cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3884–3892, Sep. 2011.

[13] P. Roshankumar, R. S. Kaarthic, K. Gupakumar, J. I. Leon and L. G. Franquelo, " A seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridge, " *IEEE Trans. Power Electron*, vol. 30, no. 7, pp. 3471-3478. Jan. 2015.

[14] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply," *IEEE Transactions on Vehicular Technology*., vol. 59, no. 8, pp. 3736–3743, Oct. 2010.

[15] Ashraf Ahmed, Mohana Sundar Manoharan, and Joung-Hu Park, "An efficient single-sourced asymmetrical cascaded multilevel Inverter with reduced leakage current suitable for single-stage PV systems" in *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, March 2019, pp.211-220.

[16] Wei-Fu Lai, Shih-Ming Chen, Tsorng-Juu Liang, Kuan-Wen Lee, "Design and Implementation of Grid Connection Photovoltaic Microinverter" in *IEEE Int. Conference*, 2012, pp. 2426-2432.

(This work is licensed under a Creative Commons Attribution 4.0 International License.)