A High Resolution FPGA-based TDC with Nonlinearity Calibration

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Abstract—This paper proposes multi-path delay line (MPDL) time-to-digital converter (TDC). Instead of traditional tapped delay line (TDL) TDC, the proposed MPDL-TDC can improve the linearity performance effectively. Implemented in a Xilinx XC5VLX110T-1FF1136 field-programmable gate array (FPGA) device, the proposed MPDL-TDC has 60 ps time resolution, and the ranges of differential non-linearity (DNL) and integral non-linearity (INL) are [−0.52, 0.52] and [−0.79, 1.06] least-significant-bit (LSB), respectively. Furthermore, 37.25 ps root-mean-square (RMS) is measured for the proposed MPDL-TDC inputting a constant delay source. Therefore, the proposed MPDL-TDC is recommended to implement in FPGA-based TDC achieving a high-resolution time and linearity performance.

Index Terms—Time-to-digital converter, Field-programmable gate array, Multi-path delay line, Differential non-linearity, Integral non-linearity.

I. INTRODUCTION

Time-to-digital converter (TDC) is an essential component in many scientific applications, such as positron emission tomography (PET) scanners [1]-[3]. Recently, many researches implement TDCs in field-programmable gate arrays (FPGAs) due to the cost, development time, and flexibility [4]-[12]. High time resolution and linearity is essential in the FPGA-based TDC design [5]. Kalisz et al. present the calibration circuit in QuickLogic pASIC FPGA to achieve 200-ps resolution time, and the measured range is 43-ns [6]-[7]. Song et al. employ the dedicated carry lines of an FPGA to implement the tapped delay line (TDL)-TDC [8]. After calibration, the resolution of the TDC implemented in an Altera EP1K50TC144-1 FPGA device is 65 ps, and that of the TDC implemented in a Xilinx XC2V4000-6BF957 FPGA device is 46.2 ps [8]. Due to the uncertainty of the placed and routed (P&R) from FPGA supported electronic design automation (EDA) tools, Wang et al. introduce the LOC and RLOC operands to allocate the delay cells in Xilinx family FPGAs [9]. Thus, the EDA tool can automatic handle the P&R instead of the time consuming man-made P&R. Besides, to improve the time resolution, Wave Union TDCs are presented in many previous works [10]-[12]. Employing the Wave Union architecture, the TDCs can improve the time resolution hugely because of the divided of the original bin size.

In this paper, a multi-path delay line (MPDL) TDC is proposed to improve the linearity. To choose the same time delay in all MPDL cells, the small differential non-linearity (DNL) values can be achieved. Therefore, the DNL and integral non-linearity (INL) values of proposed MPDL-TDC can be reduced hugely as compared with the traditional TDL-TDC. Implemented in a Xilinx XC5VLX110T-1FF1136 FPGA device, the proposed MPDL-TDC achieves 60 ps resolution and the ranges of DNL and INL are [−0.52, 0.52] and [−0.79, 1.06] least-significant-bit (LSB), respectively. Furthermore, based on the constant delay source, the proposed MPDL-TDC achieves 37.25 ps root-mean-square (RMS) time resolution. Thus, the proposed MPDL-TDC is suitable to be applied to the high-resolution applications in time measured.

This paper is organized as follows. In Section II, the design of proposed MPDL-TDC is presented that includes traditional tapped delay line architecture, important issues for FPGA design, and the proposed MPDL-TDC. Experimental results and discussions are presented in Section III, and conclusions.
are drawn in Section IV.

II. PROPOSED MPDL-TDC DESIGN

A. Traditional Tapped Delay Line TDC

The tapped delay line (TDL) is the most used architecture in FPGA-based TDC design. Figure 1 shows the architecture of the M-bin TDC with traditional TDL architecture. It is easily to be implemented using the M delay cells and registers, and FPGA is a recommended platform to implement the TDL-TDC because of its dedicated resources. The time resolution of the TDC is based on the delay cells in TDL architecture. Therefore, the smaller time delay for the delay cell, the higher time resolution can be achieved.

B. Issues of FPGA-based TDL-TDC Design

Two important issues in FPGA-based TDC with TDL architecture are resolution and non-linearity. The time resolution in TDL-TDC can be improved by using high speed FPGA. However, the non-linearity in FPGA-based TDC is difficult to handle by using advanced FPGA. Figure 2 shows the cell delay in Xilinx XC5VLX110T-1FF1136 FPGA device. By using the dedicated carry chains to implement the delay cells, the phenomenon of non-uniform distribution is existed in every FPGA-based TDC. Therefore, the non-linearity calibration becomes more and more important in FPGA-based TDC design.

C. Proposed Multi-path Delay Line TDC

Instead of the delay cell, the proposed selected multi-path delay line (MPDL) cell is applied to the FPGA-based TDC, and the proposed MPDL-TDC can improve the non-linearity effect of the non-uniform delay cells. The architecture of the proposed MPDL-TDC is illustrated in Fig. 3. The MPDL cell consists of N different delay cells \( \{ \tau_1, \tau_2, \ldots, \tau_N \} \), and the proposed TDC chooses the same delay time in every MPDL cell.
cells to achieve small DNL values. The definition of DNL is shown as follows:

\[ DNL_i (LSB) = \frac{t_i}{LSB} - 1. \]  

(1)

To achieve small DNL values, it must choose the delay cell \( \tau_{ik} \) which has the minimal deference from LSB \( \Delta \tau_{ik} \). For this reason, the choosing of the delay cell for each MPDL cell is the minimal \( \Delta \tau_{ik} \) not the smallest delay time \( \tau_{ik} \).

\[ t_1 \approx t_2 \approx \cdots \approx t_M \]  

(2)

\[ t_i = \min \{ \Delta \tau_{i1}, \Delta \tau_{i2}, \cdots, \Delta \tau_{iN} \} \]  

(3)

\[ \Delta \tau_{ik} = \text{abs}(\tau_{ik} - LSB) \]  

(4)

where \( \min \{ \bullet \} \) and \( \text{abs} \{ \bullet \} \) are the minimum and absolute operators, respectively.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The experiments are conducted with the Xilinx XUPV5-LX110T evaluation platform. The proposed MPDL-TDC is synthesized using Xilinx ISE 13.2 and implemented in Xilinx XC5VLX110T-1FF1136 FPGA device. For the code density test [13], two pulse sources (Agilent 81130A pulse data generator and a 100MHz oscillator with dedicated phase-locked loop) generate their own 166.7 MHz clock without synchronization. Thus, very slow ramp signal in time difference can be generated and \( 10 \times 2^{17} \) samples of averaged TDC outputs can alleviate the jitter effect. Due to 60 ps time resolution at 166.7 MHz frequency, 100 bins are needed to divide 6 ns time duration.

Figures 2 and 4 show the measured delay time of each bin for traditional TDL-TDC and the proposed MPDL-TDC, respectively. The non-uniform delay distribution can be improved by using the proposed MPDL architecture. For the linearity test, the DNL and INL of TDL-TDC are illustrated in Fig. 5. The obtained DNL is between \(-0.95 \) and \(1.78 \) LSB, and the obtained INL’s range is \([-8.56, 5.95] \) LSB. The LSB bin size of this measurement is 60 ps. After the histogram calibration, the proposed MPDL-TDC can improve the performance in DNL and INL. Thus, the DNL’s range

Fig. 5. The DNL and INL of traditional TDL-TDC.

Fig. 6. The DNL and INL of the proposed MPDL-TDC.
of the proposed MPDL-TDC can be reduced to $[-0.52, 0.52]$ LSB, and the INL’s range is $[-0.79, 1.06]$ LSB, as shown in Fig. 6. Large number of DNL and INL can be improved in FPGA-based TDC by using proposed MPDL architecture.

To verify the time resolution of the proposed MPDL-TDC, a constant time interval is fed as the Start signal which is with a constant delay from Stop signal. Figure 7 shows the histogram of the measured data after performing $10 \times 2^{17}$ measurements of the constant delay time. The measured mean time is 1728.5 ps, and the RMS is 37.25 ps. Consequently, the proposed MPDL-TDC can not only improve DNL and INL performance but also achieve a high resolution measurement in FPGA-based TDC design.

IV. CONCLUSION

This paper proposes the MPDL-TDC. The choosing of each MPDL cell delay time is based on the minimal DNL constraint. Therefore, the measured results show that a large number of DNL and INL improvement can be achieved and a high time resolution also can be reached in the proposed MPDL-TDC. Consequently, the proposed MPDL-TDC can deal with dedicated non-uniform delay distribution in FPGA to achieve high linearity and high resolution performance.

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