Design Optimization of High Bandwidth Memory (HBM) Interposer considering Signal Integrity

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Abstract—As total system bandwidth increased, memory industry has been imposed to satisfy its requirements. At last, innovative next generation memory named high bandwidth memory (HBM) with extremely fine micro-bump pitch of its bottom die is introduced for terabytes/s bandwidth graphics module. To establish HBM based graphics module, it becomes essential to fabricate silicon interposer due to its capability to process narrow signal width and space. Silicon based HBM interposer becomes the key solution to mitigate bandwidth bottleneck of graphics module for high computing system. To design HBM interposer successfully, the signal optimization of HBM interposer channels must be preceded thoroughly. In this paper, design optimization of top metal signals of HBM interposer considering routing feasibility is proposed. In order to analyze channel performance to determine optimal line width and space, frequency domain and time domain simulation are conducted respectively. All the proposed signals in HBM interposer are analyzed by comparing eye-opening voltage and timing jitter with 3D electromagnetic (EM) simulation results. Based on this proposed optimization design, not only HBM interposer can be applied to achieve high bandwidth with a less signal distortion but also it can be designed on the basis of a limited routing area.

Keywords—high bandwidth memory (HBM); HBM interposer; signal integrity; Insertion loss; far end crosstalk (FEXT); eye-diagram; design optimization;

I. INTRODUCTION

Recently, most computer systems are required to handle terabyte/s bandwidth for the higher computing interface. To keep up with IT trends such as big data management, cloud computing and 3D games required a high quality graphic, it becomes absolutely important to develop a terabyte/s bandwidth graphics module [1]. To address these needs, high bandwidth memory (HBM) has emerged as a solution to relieve the performance gap between a processor and a conventional DRAM [2]. It consists of 4 stacked DRAMs with 1024 numbers of data input/output (I/O) linked to a logic die at the bottom using through silicon via (TSV) technology. With 2 Gbit/s data rate in the second generation of HBM, total data bandwidth can be realized as 256 GB/s. To support its significantly large numbers of I/O, it is inevitable to fabricate the pitch of its micro bump at the logic die under 100μm [2].

The interconnection technology between HBM and a processor becomes a critical issue. In the conventional graphics module, a printed circuit board (PCB) is a main substrate to interconnect memory and processor. Since it is impossible to use a PCB for HBM, A silicon based interposer is a promising solution. A silicon substrate is commonly employed for an interposer because its technology has been applied to semiconductor industry and fine pitch routing is possible [3][4][5]. The cross-section view of a conceptual HBM interposer with 4 HBMs and a graphic processing unit (GPU) for 2.5D terabyte/s bandwidth graphics module is depicted in Fig. 1.

In this paper, HBM interposer is proposed to design using 5 layers stack-up for signals and transmission line structures as micro-strip and strip line which is suitable for applying the large numbers of I/O. Moreover the length of micro-strip line on the top layer and strip line on the third layer is designed equally as long as possible. We focus on analyzing electrical performances in terms of insertion loss and far-end crosstalk (FEXT) of micro-strip single-ended channels and proposing an optimal design guide for HBM interposer based on the case studies.

II. THE PHYSICAL DIMENSION AND THE PROPOSED STACK-UP OF HBM INTERPOSER FOR DESIGN OPTIMIZATION

All the information of HBM are given by JEDEC standard and the physical dimension related to a GPU is assumed to design HBM interposer [2]. As shown in Fig. 2, the size of a GPU is 28.5 mm × 27.0 mm based on the today’s GPU die size and the size of designed HBM interposer is 34.0 mm × 28.5 mm. We design the size of HBM interposer as small as...
possible to consider reduction manufacturing cost and high speed serial channels such as PCI express 3.0 and high definition multimedia interface (HDMI) which is not discussed in this paper. After designing HBM interposer, the critical length of HBM signal on the layer is designed as 5 mm. In addition, the allowable region for signal routing is also estimated as approximately 6,000 μm × 1,400 μm. This information is very important to determine the width and space of signals considering routing feasibility.

Ground and power for power distribution network are designed everywhere for sufficient and stable power supply and signal is routed through metal 3 to metal 5 layers. Fig. 3 represents the proposed stack-up of a signal routing area only and the design rule of HBM interposer with material property. Silicon interposer has been usually fabricated by copper (Cu) damascene process. The material property and physical dimension of layer thickness and signal line width and space are defined based on Cu-damascene process. The acceptable range of the line width and space is 0.4μm to 5μm [6], [7]. Metal 1 layer is used for power for IO interface normally known as VDDQ. Metal 2 and metal 4 layers are used for ground. Those layers are employed as return current paths for HBM channels. Metal 3 and Metal 5 are applied to signal layers. Especially, metal 2 layer is also used for power distribution network of HBM interposer. As shown in Fig. 3, transmission line structures are micro-strip line and strip-line. Following the proposed stack-up, the large numbers of signals over six thousand in the HBM interposer can be stably transmit and the required area for routing can be minimized compared to a coplanar wave guide structure.

III. THE ANALYSIS OF ELECTRICAL PERFORMANCES TO OPTIMIZE HBM INTERPOSER CHANNELS

Before optimizing of HBM channels, it is preceded to analyze HBM channel characteristic in accordance with the line width and space. Insertion loss and FEXT of HBM channels are simulated. The simulation environment is illustrated in fig. 3. Target channel is assigned in the center with the 4 aggressors to simulate FEXT.

A frequency domain simulation is conducted ranging from 0 Hz to 20 GHz using a 3D electromagnetic (EM) solver, ANSYS HFSS. Solution data are extracted from 50 Ω renormalization for each termination. The simulation set-up for

![Fig. 2. The top view of conceptual HBM interposer with physical dimensions to consider routability and critical length of signals.](Image)

![Fig. 3. The physical dimension and material property of proposed HBM interposer design.](Image)

![Fig. 4. The simplified model of initial set-up to simulate eye-diagram for single-ended channels.](Image)
conductor DC loss, designing the signal width wider could be an appropriate solution as plotted in Fig. 5(b). When it comes to the signal width, it is clearly observed that the wide channel of insertion loss in a low frequency region is improved. It represents that the resistance value is decreased. But this result cannot guarantee that designing wide width signals is always showing a positive result in the aspect of insertion loss. In the high frequency region, the effects of resonance from the capacitors and inductors of signals including mutual capacitors and inductors and impedance mismatching are noticeably increased. Consequently, insertion loss becomes more severe in the wide signaling. In the end, approximately over 4 GHz frequency region, the insertion loss of wide channel becomes rapidly decreased due to the resonance and impedance mismatching with the conductor AC loss.

Fig. 6 represents far end crosstalk (FEXT) according to the space and width variations. Since channels of HBM interposer are designed adjacently due to its limited routing area, the effect of cross-talk must be taken into account. As shown in Fig. 6(a), the wider spacing shows absolutely better performance over the entire frequency region. In the frequency region over 1 GHz, FEXT is dramatically fluctuated due to the combination of resonance, impedance mismatching and conductor loss as the same result of Fig. 5(a). As depicted in Fig. 6(b), wide width designing is substantially affected FEXT. That is because wide signal is more influenced by the fields induced by adjacent aggressors so that FEXT capacitive coupling is increased. Owing to the resonance of wide width signals as simulated in the Fig. 5(b), the fluctuation of FEXT magnitude is also observed near 2 GHz. Based on above simulation results, to minimize FEXT and better performance, the signal space is recommended more than 3.6 μm so that the transferred voltage from 4 numbers of aggressors that means far-end crosstalk can be mitigated under 5 % (0.06 V) of peak-peak voltage of HBM signals voltage swing (1.2V) [2].

B. The analysis of frequency domain simulating

A time domain simulation is the key simulation to optimize HBM interposer design. The result is presented in eye-opening voltage and timing jitter. Depending on the line width and space, time domain simulation results using MATLAB 3D-plot are illustrated in Fig. 7(a) and (b). Based on those 3D plots, channels of HBM interposer can be optimize conveniently. The target performance is assumed to 0.7 V of eye-opening voltage which is five times of LPDDR4 mask height and 75 ps of timing jitter which is 15 % of 1 UI at the data rate of 2 Gbps [8]. Dotted line is referring the target specification. A channel performance have to satisfy both eye-opening voltage and timing jitter specification with the consideration of rout-ability. The best signal performance considering minimum pitch from the case studies is simulated with the line with 3.2 μm and space 4.8 μm as shown in Fig. 8(c). The optimized signals for

![Fig. 5. The simulated insertion loss of single-ended channels (a) the space variation (b) the width variation](image)

![Fig. 6. The simulated FEXT of single-ended channels (a) the space variation (b) the width variation](image)
HBM interposer can be obtained by designing 3.0 μm width and 3.6 μm space signal. It satisfies assumed the target specifications along with an acceptable routing area approximately $1,200 \mu m \times 5,600 \mu m$. The eye opening voltage and timing jitter are simulated as 0.745 V and 57.0 ps respectively.

IV. CONCLUSION
In this paper, we successfully optimize HBM interposer signals on the top layer based on Cu-damascene process. The electrical performances of HBM interposer channels are simulated both in the frequency and time domain. As the previous step for optimizing HBM channels, the channel performances simulated from a variety of signals width and space variation are analyzed by an insertion loss magnitude of ISI and FEXT. With the consideration of routing feasibility and signal quality, we propose optimal design guide for HBM interposer. To design HBM interposer with over thousands of IOs, coupled micro-strip line is suggested. Especially, the 3D plots for the design optimization is conducted by approximately 200 numbers of case studies. By utilizing 3D plot figures, the process of the optimization for HBM interposer can be conveniently determined. The result of optimized line width and space is proposed as 3.0 μm and 3.6 μm respectively. Even if we only analyze HBM channels on the top, the procedure for the design optimization is almost similar in case of strip-line designed in metal 3 layer and high speed serial channels.

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