DESIGN AND SIMULATION OF A GaAs HBT POWER AMPLIFIER FOR WIDEBAND CDMA WIRELESS SYSTEM

M. S. Alam†, O. Farooq, Izharuddin
Department of Electronics Engineering
Z.H. College of Engineering & Technology
A.M.U. Aligarh 202002 India

and G. A. Armstrong
School of Electrical & Electronics Engineering
Ashby Building, Stranmillis Road
Queen’s University of Belfast
BT9 5AH, United Kingdom

1. INTRODUCTION

Power amplifiers are important circuit components used in wide-band code-division multiple-access (WCDMA) wireless communication systems. To accommodate more users and maximize the usage of the spectrum in WCDMA systems, power amplifiers (PAs) have to be highly linear and more efficient. In recent years, there has been a high demand for hetero-junction bipolar transistors (HBTs) for design of power amplifiers (PA) used in WCDMA wireless systems due to their better linearity and superior high-frequency performance [1]. The specifications of third-generation (3G) WCDMA PAs are listed in Table 1.

Due to lack of availability of a compact model from the foundry, an artificial neural networks (ANNs) based non-linear GaAs HBT model (given in [3]) has been used to carry out power amplifier design. A full PA simulation in ADS [4] using an ANN model [3] has been carried out and results shows that various third generation (3G) specifications such as gain, power-added efficiency (PAE), and adjacent channel power rejection have been achieved over nominal and extreme temperature conditions.

Key words: power amplifier, GaAs HBT, wideband CDMA, wireless system

† To whom correspondence should be addressed.
Tel/Fax: +91 571 2721148
E-mail: m.alam@ee.qub.ac.uk; m_shah_alam@rediffmail.com

Paper Received: 20 March 2007; Revised: 04 October 2007; Accepted: 28 November 2007
2. POWER AMPLIFIER DESIGN

The GaAs HBT power amplifier circuit shown in Figure 1 has been developed to operate in the frequency range between 1–2 GHz. It consists of two stages of amplification. The first stage has 10 transistors (unit cells) in parallel and the second stage has 36 transistors (unit cells) in parallel.

![Figure 1. The AC coupled schematics of the GaAs HBT power amplifier [1]](image)

Each unit cell is of size 2×3×30µm². Both stages have base ballasting for adequate thermal stability [1,5]. The coupling capacitance $C_C$ is used to couple the input signal and provide AC coupling between stages. Temperature compensated base supply voltages gives stable circuit performances such as gain, power added efficiency (PAE), and adjacent channel power ratio (ACPR) even at extreme temperature conditions. A harmonic trap is used to improve linearity and an RC feedback network is used to linearize the stages as well to improve the circuit stability. The first and the second stage base DC supply voltages are $V_{BI}$ and $V_{B2}$ respectively, which are derived from a temperature compensated bias control circuit [1]. The $V_{C1}$ and $V_{C2}$ typically 3.4 V are, respectively, the first and second stage collector supply voltages. Typically $V_{REF} = 3V$ provides a precisely controlled regulated supply to accurately define bias current. Control voltage $V_{CONT}$ determines the mode of operation of PA, which is a function of bias current ($V_{CONT} = 0V$; high mode of operation and $V_{CONT} = 3V$; low mode of operation). The number of cells in each stage of the amplifier is chosen to distribute the gain between the two stages, so that the maximum recommended current density of the individual transistors (unit cell) is not exceeded [1].

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>1.92–1.98 GHz</td>
</tr>
<tr>
<td>Maximum Output Power</td>
<td>+23 dBm− +35dBm</td>
</tr>
<tr>
<td>PAE @ Maximum Output Power</td>
<td>~ 30%</td>
</tr>
<tr>
<td>ACPR (3.84 MHz measured main channel)</td>
<td>-33 dBc @ 5MHz</td>
</tr>
</tbody>
</table>
2.1. Design Equations

Carrying out a similar analysis as in [6] for the circuit shown in Figure 1, the following design equations can be developed:

\[ R_{f2} = \sqrt{2A_{Y_S}R_sR_L} \]  \hspace{1cm} (1)

\[ R_e = (R_sR_L)/(R_{f2}/|g_m|) \]  \hspace{1cm} (2)

Given \( R_s \) and \( R_L \) equal to 50\( \Omega \), and known value of overall voltage gain \( A_{Y_S} \) equal to 25 dB in (1), \( R_{f2} \) is calculated as given in Table 2. With known device \( g_m \) at given bias and using (2), \( R_e \) can be calculated. Base ballasting resistance \( R_{ballast} \) is calculated from thermal stability consideration [5]. Effect of emitter bond wires inductance is critical for prediction of gain and linearity of PA. In order to determine value optimum value of bond wire inductance \( L_e \), power amplifier gain, third-order harmonic (IM3) and power added efficiency (PAE) are simulated in ADS [4] at \( L_e = 0 \) nH and \( L_e = 100 \) nH as shown in Figure 2.

![Figure 2. Comparison simulated gain, third-order harmonic (IM3) and PAE of PA at different bond wires emitter inductance \( L_e \) at \( V_{CONT} = 3 \) V and \( V_{REF} = 3 \) V](image)

As shown in Figure 2, by filled symbol marks at rated output power line, gain (\( \diamond \))\( \approx 23.4 \) dB, IM3 (\( \bullet \))\( \approx -35.8 \) dBc and PAE (\( \bullet \))\( \approx 33.5 \) % are obtained at mean inductance \( L_{mean} \) equal to 50nH. These performance measures are well within the power amplifier requirements for 3G wireless communication system [2]. Therefore, \( L_{mean} \) is taken for design of power amplifier to achieve optimum performance. Output impedance matching criteria has been used to calculate \( C_1, \) \( C_2, \) and \( R_C \) [7]. The designed power amplifier parameters are summarized in Table 2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>( C_1 ) (pF)</th>
<th>( R_C ) (k( \Omega ))</th>
<th>( R_{ballast} ) (( \Omega ))</th>
<th>( R_E ) (k( \Omega ))</th>
<th>( R_s ) (( \Omega ))</th>
<th>( L_e ) (pH)</th>
<th>( L_1 ) (nH)</th>
<th>( C_1 ) (pF)</th>
<th>( C_2 ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>2.50</td>
<td>2.50</td>
<td>75.0</td>
<td>0.28</td>
<td>2.50</td>
<td>50.0</td>
<td>50.0</td>
<td>0.45</td>
<td>0.25</td>
</tr>
</tbody>
</table>

2.2. Design Verifications

Figure 3 shows the simulated result of bias current over the temperature range – 20°C to 85°C when the value of \( V_{REF} = 2.9 \pm 0.1 \) V with \( V_{CONT} = 0 \) V for high mode, \( V_{CONT} = 3 \) V for low mode of operation. It can be observed from Figure 3 that the bias collector current \( I_C \) monotonically increases with increase in temperature both in low and high mode of
operation of power amplifier. The increase in \( \tau_C \) compensates for the roll-off in DC-current gain \( \beta \) with increase in temperature [1]. Thus, making gain of the HBT PA amplifier stable even under extreme temperature conditions as shown in Figure 4.

3. PERFORMANCE RESULTS

The PA module shown in Figure 4 has been assessed to evaluate performance measures such as gain, linearity (first ACPR), and power-added efficiency (PAE) under WCDMA excitation.

The graph of Figure 4 shows the behavior of PA with \( V_{\text{CONT}} = 3 \) V for power amplifier gain, PAE and ACPR for 1.925 GHz personnel communication system (PCS) band. The graph shown in Figure 4(a) show that amplifier gain lies within \( \pm 0.85 \) dB up to 28 dBm of rated output power at various temperature conditions, while maintaining the desired specifications of PAE > 30% and first ACPR<-33 dBc as shown in Figure 4(b-c).

4. CONCLUSION

In this work, a power amplifier for WCDMA has been designed. An ANN based non-linear model has been used to carry out PA circuit simulation. The designed PA circuit is verified through the simulation of various performances such as gain, PAE, and ACPR at different temperatures. The PA operates over a range of temperatures whilst maintaining credible performance. Gain of the power amplifier is above 22 dB over a wide range of operating output power. The
amplifier is able to deliver rated 28 dBm power with more than 30% PAE and maintains high linearity (first ACPR $<-33$ dBc). The results establish the suitability of the GaAs HBT PA suitability for wireless applications.

ACKNOWLEDGMENT

M. S. Alam is grateful to the Queen’s University of Belfast (United Kingdom) for help with Advanced Design System (ADS)-2005A based simulation to carry out this work.

![Figure 4. PA module performances with $V_{\text{CONT}} = 3V$ and $V_{\text{REF}} = 3V$ over temperatures for (a) power gain (b) PAE (c) ACPR](image_url)

*Figure 4. PA module performances with $V_{\text{CONT}} = 3V$ and $V_{\text{REF}} = 3V$ over temperatures for (a) power gain (b) PAE (c) ACPR*
REFERENCES


