AIP Applied Physics Letters

Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon

Byoung Hun Lee, Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi, and Jack Lee

Citation: Appl. Phys. Lett. **74**, 3143 (1999); doi: 10.1063/1.124089
View online: http://dx.doi.org/10.1063/1.124089
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v74/i21
Published by the American Institute of Physics.

Related Articles

Electrical and piezoelectric properties of BiFeO3 thin films grown on SrxCa1−xRuO3-buffered SrTiO3 substrates
J. Appl. Phys. 111, 114102 (2012)

Electrical properties of (110) epitaxial lead-free ferroelectric Na0.5Bi0.5TiO3 thin films grown by pulsed laser deposition: Macroscopic and nanoscale data
J. Appl. Phys. 111, 104106 (2012)

Tunable strain effect and ferroelectric field effect on the electronic transport properties of La0.5Sr0.5CoO3 thin films
J. Appl. Phys. 111, 103702 (2012)

Coexistence of unipolar and bipolar resistive switching in BiFeO3 and Bi0.8Ca0.2FeO3 films
J. Appl. Phys. 111, 104103 (2012)

Tunneling resistance and its effect on the electrical conductivity of carbon nanotube nanocomposites
J. Appl. Phys. 111, 093726 (2012)

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT

Agilent Technologies
Agilent Education and Research Resources DVD 2012
Packed with over 100 NEW articles, application notes, webcasts, and videos relating to Renewable Energy, Nanoscience, RF/Wireless, MIMO, Materials, Digital Signals, Photonics, and General Test & Measurement.
Click Here to Order Your DVD

Agilent Technologies

Downloaded 18 Jun 2012 to 203.237.57.191. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon

Byoung Hun Lee,[a] Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi, and Jack Lee
Material Research Center, University of Texas at Austin, Austin, Texas 78758

(Received 22 September 1998; accepted for publication 30 March 1999)

Effects of interfacial layer growth on reactively sputter-deposited TiO_2 films were studied. Leakage current was reduced to 10^{-8} A/cm^2 at +1 V after annealing in oxygen ambient and showed tunneling-like temperature dependence. As the interfacial layer grew, interface states and hysteresis were improved significantly. However, the reliability was degraded as the annealing temperature increased. © *1999 American Institute of Physics.* [S0003-6951(99)03121-6]

Binary metal oxides such as CeO_2,[1] Y_2O_3,[2] Al_2O_3,[3] Ta_2O_5,[4] and TiO_2 (Refs. 5 and 6) have been studied as alternative gate dielectrics for scaled metal–oxide–semiconductor field-effect transistors to overcome the scaling limit of conventional gate oxides. Among them, TiO_2 has received a lot of attention recently because of its high dielectric constant. However, the dielectric properties of TiO_2 are known to be degraded by several interfacial reactions with silicon, such as retarded crystallization,[7,8] intermixing with SiO_2,[9] and growth of a low dielectric constant interfacial layer. Thus, the reported dielectric constants of TiO_2 films are scattered in the range of 16–52,[9] 4–40,[10] and 20–86,[11] while that of rutile bulk TiO_2 is 170 along the optic axis and 89 perpendicular to the optic axis.[9] These adverse effects will become worse at the thin-film regime (<10 nm), where the effects of interfacial reactions are more substantial. However, only a few works have been done to assess the effects of the interfacial layer[6,12] and to the best of our knowledge the reliability characteristics of TiO_2 have not been studied yet. In this letter, we present the effects of the interfacial layer on the electrical characteristics of 10 nm TiO_2 films with a comparison of TiO_2 films deposited on a metal substrate.

TiO_2 films were reactively sputter deposited on a bare silicon wafer and an iridium-coated wafer, respectively, at a pressure of 10 mTorr of Ar with 20% O_2 using dc magnetron sputtering. A platinum electrode (thickness ~100 nm) was used. After wet etching the electrode, the samples were annealed at various temperature ranging from 500 to 900 °C in N_2 or O_2 for 5 min. The film thickness and refractive index were measured using a single-wavelength ellipsometer with a single-layer model and examined with scanning electron microscopy. The crystalline phase of the annealed film was analyzed by x-ray diffraction.

The equivalent oxide thickness (EOT) extracted from the accumulation capacitance stayed fairly constant after annealing while the physical thickness measured with the ellipsometer increased (Fig. 1). The unpublished x-ray diffraction analysis data showed that the peak from the anatase phase in as-deposited TiO_2 grew as the O_2 annealing temperature increased. The refractive index of the TiO_2 films increased from 2.3 to 2.5 after the 700 °C annealing, but decreased to 2.25 again after the 800 °C annealing. The decrease of the refractive index indicates that the interfacial layer growth becomes dominant beyond this temperature. The slow increase of the EOT is a result of a trade-off between the crystallization and interfacial layer growth.

The leakage current of the O_2 annealed capacitors decreased rapidly to 10^{-7}–10^{-8} A/cm^2 after annealing while that of the N_2 annealed capacitors fluctuated around the 10^{-3}–10^{-4} Al/cm^2 range (Fig. 1). The decrease in leakage current by the O_2 anneal seems to be related to the growth of interfacial layer and the reduction of oxygen vacancies.[13] The leakage current of the metal–insulator–silicon (MIS, $Pt/TiO_2/Si$) capacitor showed a tunneling-like temperature dependence while that of the metal–insulator–metal (MIM, $Pt/TiO_2/Ir$) capacitors showed the strong temperature dependence ($E_a \approx 0.78$ eV for both bias polarity) (Fig. 2). This trend indicates that the tunneling current passing through the interfacial layer limits the total leakage current of the MIS capacitor.

By comparing the EOT of the MIS and MIM capacitors, the thickness of the interfacial layer was found to be about 2.2 nm (Fig. 3). This value is very close to our previous transmission electron microscopy observation.[6] The nearly constant thickness of the interfacial layer at different physical thickness indicates that the interfacial layer was grown at the initial step of the deposition process. From the reciprocal slope of Fig. 3, the dielectric constant of TiO_2 deposited on metal was calculated to be about 95. The similar slope of the

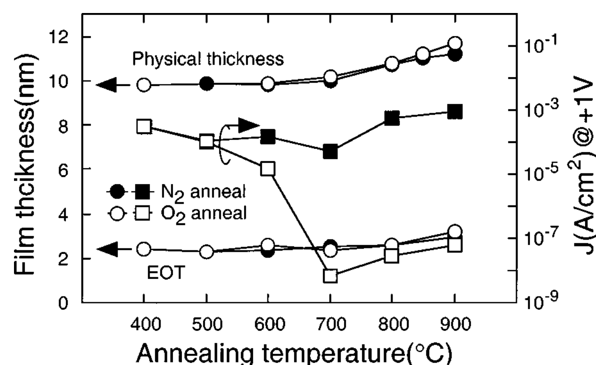

FIG. 1. The equivalent oxide thickness and the gate leakage current at +1 V changed by the postdeposition annealing.

[a]Electronic mail: bhlee@mail.utexas.edu

 © 1999 American Institute of Physics

Downloaded 18 Jun 2012 to 203.237.57.191. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

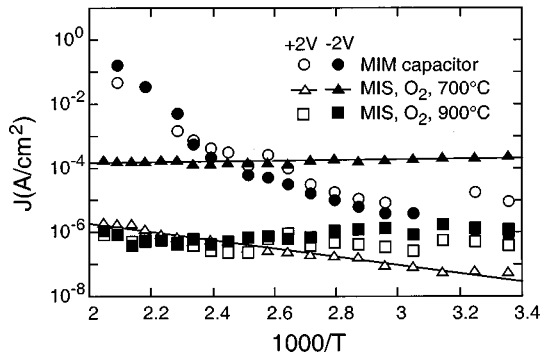

FIG. 2. The temperature dependence of leakage current measured at ±2 V (solid marks: +2 V and empty marks: −2 V).

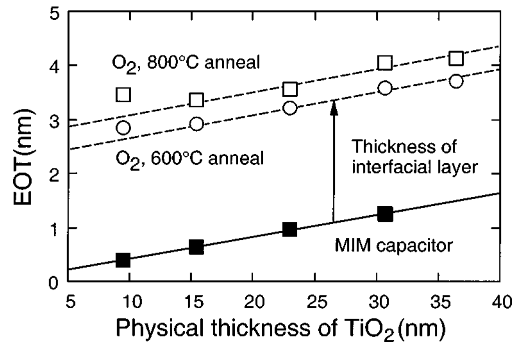

FIG. 3. The equivalent oxide thickness of the TiO_2 layer as a function of the physical thickness of the TiO_2 film.

MIS and MIM capacitors indicates that the dielectric constant of the TiO_2 layer deposited on top of the interfacial layer is close to that of the TiO_2 deposited on metal. Since the additional growth of the EOT by annealing was also thickness independent, the growth of the interfacial layer seems to be due to the reaction-limited oxidation.

Although the leakage current decreased as the thickness of the interfacial layer grew, the time zero dielectric breakdown voltage of the MIS capacitors degraded after annealing and the same trend was observed at the MIM capacitors (Fig. 4). This trend implies that the breakdown of the MIS capacitor is related to the properties of the TiO_2 layer rather than that of the interfacial layer.

To understand this result in detail, the breakdown voltage of the MIS capacitor was measured at different TiO_2 thicknesses (Fig. 5). The electric field applied to the TiO_2 layer and the interfacial layer were estimated, respectively, using a series capacitor model.[14] The interfacial layer was assumed to be 2 nm of SiO_2 to simplify the calculation. The calculated breakdown field of the TiO_2 layer was nearly constant at different thicknesses while that of interfacial layer increased to an unreasonably high value. The constant breakdown field at TiO_2 indicates that the breakdown process is driven by the same mechanism. This result further supports our contention that the breakdown mechanism is related to the characteristics of the TiO_2 layer itself.

Unfortunately, although the series capacitor model showed a qualitative trend matching with the experiment, it is not an exact model because the calculated electric field at the interfacial layer is not reasonable. If the electric field is so high, the interfacial layer should breakdown first. This discrepancy may be resolved by the charge accumulation model suggested by Nishioka, Shinriki, and Mukai.[14] According to this model, charge carriers are accumulated at the interface of the TiO_2 layer and the interfacial layer due to the different leakage current density and the accumulated charge limits the electric field applied to the interfacial layer below the critical breakdown field. Thus, the electric field applied to the TiO_2 layer increases further and the reliability characteristics are to be determined by the properties of the TiO_2 layer. The reasons for the reliability degradation of TiO_2 are not understood yet. It may be the intrinsic characteristics of crystallized TiO_2 or it may be caused by the degradation of the TiO_2 stoichiometry[15] and silicon interdiffusion.

As for the interface properties, a substantial amount of flatband voltage shift and hysteresis were observed at the

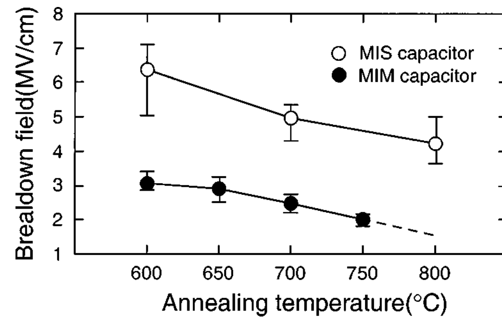

FIG. 4. Time zero dielectric breakdown voltage was decreased as the annealing temperature increased. The distribution of breakdown voltage was obtained from 30 points measurement.

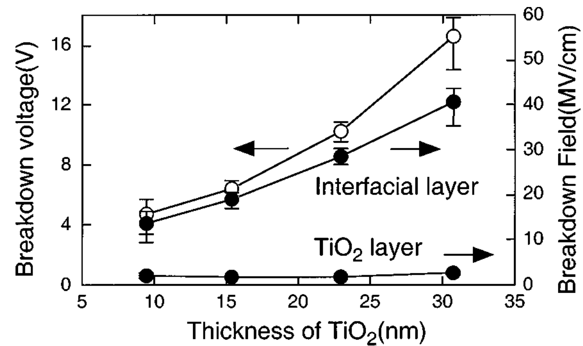

FIG. 5. Breakdown voltage increased as the physical thickness increased while the breakdown field applied to the TiO_2 layer was almost constant.

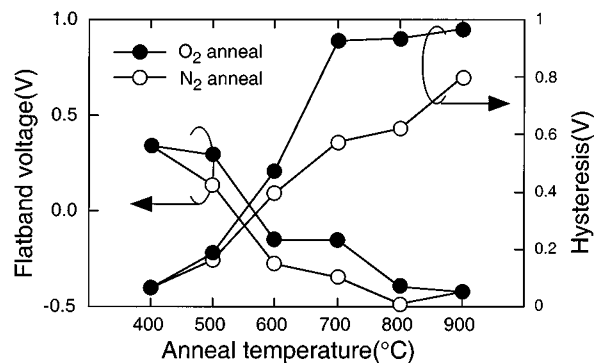

FIG. 6. The flatband voltage was restored to the ideal value after high-temperature annealing and the hysteresis was reduced to a negligible level.

Downloaded 18 Jun 2012 to 203.237.57.191. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

as-deposited films. However, as the annealing temperature increased, the flatband voltage was saturated at about 0.9 V in O_2 ambient (Fig. 6). Also, the counterclockwise hysteresis of $C-V$ curve due to the charge trapping at the negative gate bias was reduced to a negligible level. The interface state density of the TiO_2 films determined by the Terman method was comparable to thermal oxide ($<10^{11}/cm^2\,eV^{-1}$) after annealing.

In summary, it was found that the properties of the interfacial layer have crucial effects on the electrical characteristics of the MIS capacitor, such as leakage current, interface states, and hysteresis. However, the reliability of the TiO_2 capacitor was more affected by the properties of the TiO_2 layer itself.

This work was partially supported by SRC.

[1] T. Inoue, T. Ohsuna, Y. Obara, Y. Yamamoto, M. Satoh, and Y. Sakurai, Jpn. J. Appl. Phys., Part 1 **32**, 1765 (1993).
[2] L. Manchanda and M. Gurvitch, IEEE Electron Device Lett. **9**, 180 (1988).
[3] K. P. Pande, V. K. R. Nair, and D. Gutierrez, J. Appl. Phys. **54**, 5436 (1983).
[4] P. K. Roy and I. C. Kizilyalli, Appl. Phys. Lett. **72**, 2835 (1998).
[5] H. Kim, D. C. Gilmer, S. A. Campbell, and D. L. Polla, Appl. Phys. Lett. **69**, 3860 (1996).
[6] Y. Jeon, B. H. Lee, K. Zawadzki, W. Qi, and J. C. Lee, Tech. Dig. Int. Electron Devices Meet., 797 (1998).
[7] D. G. Howitt and A. B. Harker, J. Mater. Res. **2**, 201 (1987).
[8] N. S. Gluck, H. Sankur, J. Heuer, J. DeNatale, and W. J. Gunning, J. Appl. Phys. **69**, 3037 (1991).
[9] P. Alexandrov, J. Koprinarova, and D. Todorov, Solid-State Electron. **47**, 1333 (1996).
[10] W. D. Brown and W. W. Grannomann, Solid-State Electron. **21**, 837 (1978).
[11] T. Fuyuki and H. Matsunami, Jpn. J. Appl. Phys., Part 1 **25**, 1288 (1986).
[12] G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdal, Appl. Phys. Lett. **73**, 1517 (1998).
[13] S. C. Sun and T. F. Chen, Jpn. J. Appl. Phys., Part 1 **36**, 1346 (1997).
[14] Y. Nishioka, H. Shinriki, and K. Mukai, J. Appl. Phys. **15**, 2335 (1987).
[15] M. A. Taubenblatt and C. R. Helms, J. Appl. Phys. **53**, 6308 (1982).

Downloaded 18 Jun 2012 to 203.237.57.191. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions