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Impact of Injected Charges, Clock Noise and Operational Amplifier Imperfections on the Sample and Hold (SH) Overall Performance

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Abstract

The growing use of digital processing in analog environments underlines the importance of Analog Digital Converter (ADC) occurrence in circuitry. The quality and reliability of the conversion are closely linked to the Sample and Hold (SH) performance. Actually SH is a key component in the Analog/Digital chain. The Operational Amplifier being at the heart of the SH influences its output and subsequently impacts the reliability and quality of the conversion. In this paper we present the impact of both Operational Amplifier intrinsic characteristics and external factors such as injected charges, and clock noise on the SH overall performance. We limit our consideration to the offset and parasite capacities as the only relevant Operational Amplifier intrinsic characteristics. We'll introduce the Operational Amplifier and SH functional characteristics then address the impact of each of these parameters on the SH output which the ADC works on. A behavioral description of the Operational Amplifier based on the *Verilog-A* language under *Cadence* approach is used. Furthermore a behavioral/analog mixed description is considered for the SH: the Operational Amplifier described behaviorally in *Verilog-A* is associated to analog components in *Cadence* libraries and CMOS switches act as SH. However this simplistic approach doesn't reflect all the challenges involved, because it is not enough to connect a SH to ADC to flawlessly digitalize an analog signal. The SH architecture and the Operational Amplifier characteristics play also a role for a reliable sampling and therefore a good quality conversion prospect.In this study the SH performance is evaluated through its non-linearity which in turn determines the sampling accuracy a key factor for a conversion. This study is as shown that small amplitude signals are more sensible to sampling errors related to Operational Amplifier offset. Furthermore the stray capacities attenuate the SH signal output. The injected charges and the clocknoise as strongly interrelated contribute to the non-linearity of the conversion chain.

Keywords: ADC, SH, operational amplifier, injected charges, offset, clock noise, stray capacities

1. Introduction

Today the majority of the circuits and electronic systems use the digital processing of the acquired data.However in Nature phenomena are analogic in essence; therefore the need for converting those analogical signals numerically arises. This conversion is made through an ADC (Analog Digital Converter), in which the Sample and Hold (SH) circuit placed upstream is a key component.

As depicted in Figure 1, the SH handles the signal both at the entry and at any further stage in the ADC pipeline. The operational amplifier as fundamental component is shown in Figure 2, representing an elementary SH. This way of presenting analogical to digital conversion is not however free from imperfections: it is not enough to simply connect an SH to an ADC to flawlessly digitize an analogical signal. Structures of the SH and the Operational Amplifier are determining as shown in the subsequent sections for a good sampling and thus a reliable conversion.

The work presented in this paper consists the one hand developing and to validate a behavioral model of Operational Amplifier under the *Cadence* environment. Then, a study of impact on the SH of Operational Amplifier offset, the injected charges, the stray capacities and the clock noise will be presented.

2. ADC Pipeline and Operational Mode

General diagram of Analog-to-Digital Converter (ADC) pipeline 5 bits is shown in Figure 1, and further in references (Lewis et al., 1992; Cho & Gray, 1994; Brandt & Lutsky, 1999).

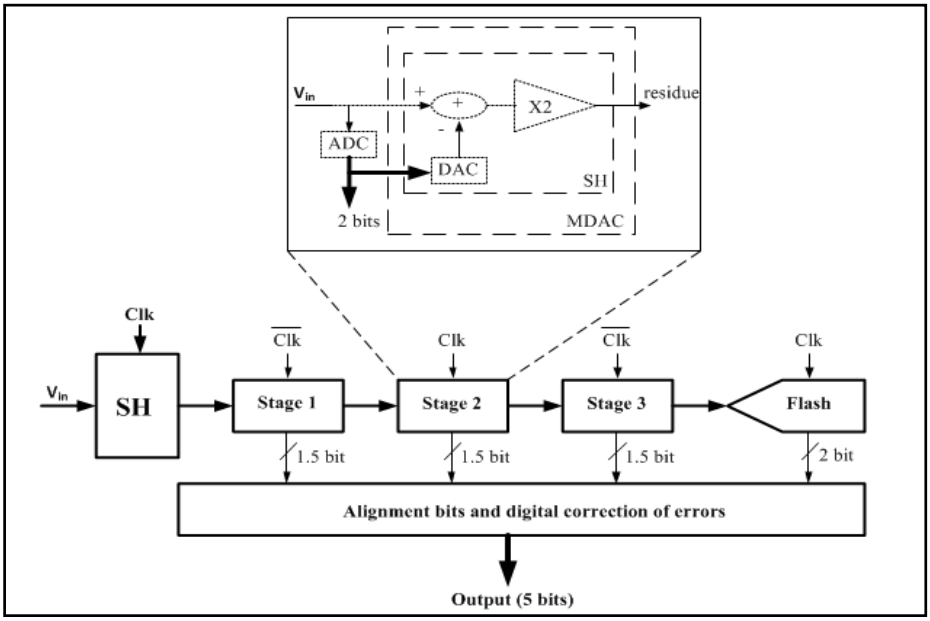

Figure 1. General diagram of the pipeline converter

SH is the first element of the pipeline ADC. It allows the sampling and holding of the sample during the conversion. The SH is followed by three successive stages low resolution followed by a flash last stage. They are successively controlled by the clock signal (Clk).

Each stage consists of:

- An ADC flash including 2 comparators and a transcoder two to two,
- A Digital to Analog Converter (DAC),
- A Circuit subtracter- multiplier by 2.

Each stage integrates a Multiplying Digital-to-Analog Converter (MDAC) which is key component and the most critical. MDAC realizes thedigital-to-analog conversion of ADC output and subtracting the output signal of the DAC (reference) of the sample danalog input (V_{in}) and multiplying this difference by 2. The residue represents the result of the multiplication.

The first stage samples the input signal further processed through the stages in the pipeline of the converter. Each one of these stages delivers a binary code corresponding to the input signal of the current stage. This binary code is converted into an analogical voltage which will be with drawn from the input signal. This difference is amplified before being sent on the entry of the following stage. The last stage is a flash.

The successive numerical results from the stages pipelines are aligned using shift registers. Then, the synchronized results corresponding to the same analogical input signal pass through a logic of errors correction due to offsets comparators.

The next section presents the operating mode of Sample and Hold (SH) and its parameters limits.

3. The Sample and Hold (SH)

The SH allows the analogic signal sampling, i.e. memorizing the entry signal amplitude value at a given time t, and holds this value throughout time interval T_{HOLD}. Figure 2 shows the elementary SH circuit, it features a MOS transistor acting as a switch.

3.1 Mode of Operation

A basic SH model as illustrated below in Figure 2. When switch Φ is ON, the capacity voltage is V_{IN} the SH

input; when switch is OFF, the capacity memorizes the acquired value right before the switch opening. Consequently for working at high speed, it is necessary to be able to charge the storage capacity very quickly. This requires a weak time-constant RC by actingon the value of C knowing that the second parameter, namely the resistance R depends on passing state of the switches (Standarovski, 2005). It is necessary to use active structures such as the Operational Amplifier to read the output signal.

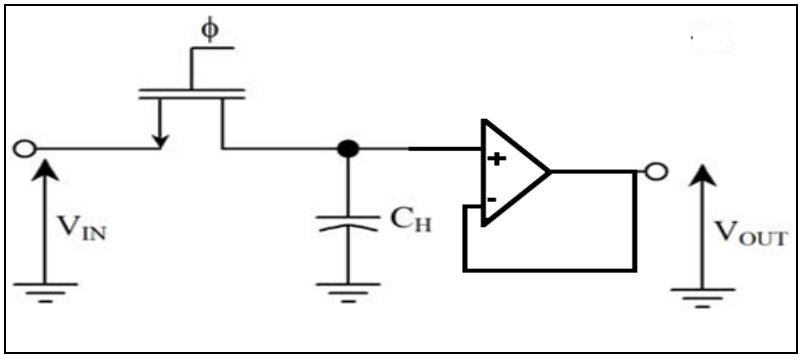

Figure 2. Elementary Sample and Hold

3.2 Parameters Limiting the SH Performance

There are several parameters affecting the SH performance. We are interested in this study in the injected charges, the clock noise, stray capacities and Operational Amplifier offset as described in (Laker & Sansen, 1994).

3.2.1 Injected Charges

A major limitation in the SH performance is often related to the phenomenon of charges injection i.e. residual charges when the switch passes from the ON to OFF state: the transistor operates in the conduction mode and presents a small potential difference between drain and source in the ON state; consequently a residual charge $Q_{channel}$ is stored. The charge injection occurs in two ways:

- The residual charges are injected in the circuit through the transistor's source and drain; expressed as follows :

$$Q_{canal} = -C_{canal}(V_{gs} - V_{th}) = -W_{eff}L_{eff}C_{ox}(V_{gs} - V_{th}) \quad (1)$$

And more thoroughly by (Ding & Harjani, 2000).

Q_{canal}: residual charge in conduction mode

C_{ox}: Capacity of grid oxide per area unit

C_{canal}: Capacity between grid/and the channel

V_{th}: threshold Voltage of MOS transistor

Vgs: Static voltage grid/source

W_{eff}: MOS transistor channel Width

L_{eff}: MOS transistor channel Length

- Recover capacity Cov between the grid and source-drain system builds with the storing capacity C_h capacitive divider bridge, consequently the MOS transistor voltage command became proportional to the equivalent voltage capacity as explained by (Eichenberger & Guggenbühl, 1991).

Furthermore the amount of injected charges is proportional to the switch sizes; actually the number of electrons transiting through the channel is directly proportional to the transistor size, W*L; whereby W refers to the transistor's width and L its length.

There are obvious limitations to reducing the transistor size; however we do have freedom to choose the storing capacity value to optimize the RC constant. The choice is but subject to the following relationship:

$$\frac{KT}{C} \leq \frac{SNR}{10} \quad (2)$$

Where K refers to the Planck's constant, T refers to the temperature, C refers to the storing capacity and SNR refers to the signal to noise ratio.

3.2.2 Clock Noise

During the hold phase the output signal may be altered by the clock signal due to possible capacitive coupling between the command signal output voltages. This results in the overlapping of a command signal image to the genuine signal as explained by (Standarovski, 2005).

3.2.3 The Stray Capacity

The transition from ON to OFF state of the analog switch induces a stray capacity C_p due to the recovering capacity. As said$C_p$and the storing capacity $C_h$build a capacitive bridge.The resulting error ΔV_p dealt with in detail in (Eichenberger & Guggenbühl, 1991) is expressed as:

$$\Delta Vp = -\frac{Cp(Vdd-Vss)}{Cp+Ch} \quad (3)$$

Where C_p is the stray capacity, C_h the storing capacity, V_{dd} the positive supply voltage, and $V_{ss}$the negative supply voltage.

4. The Operational Amplifier

We start off with a generic model, i.e. including all possible Operational Amplifier parameters.

To validate the model we carried out anAC and transient analysis as illustrated in Figure 3. The results showed an transient response between V_{dd} and V_{ss} centered around half V_{dd}; the common mode. On the other hand the AC response shows a 50.8 dB gain and a 50 MHz bandwidth corresponding to the input parameter values; thus validating our model.

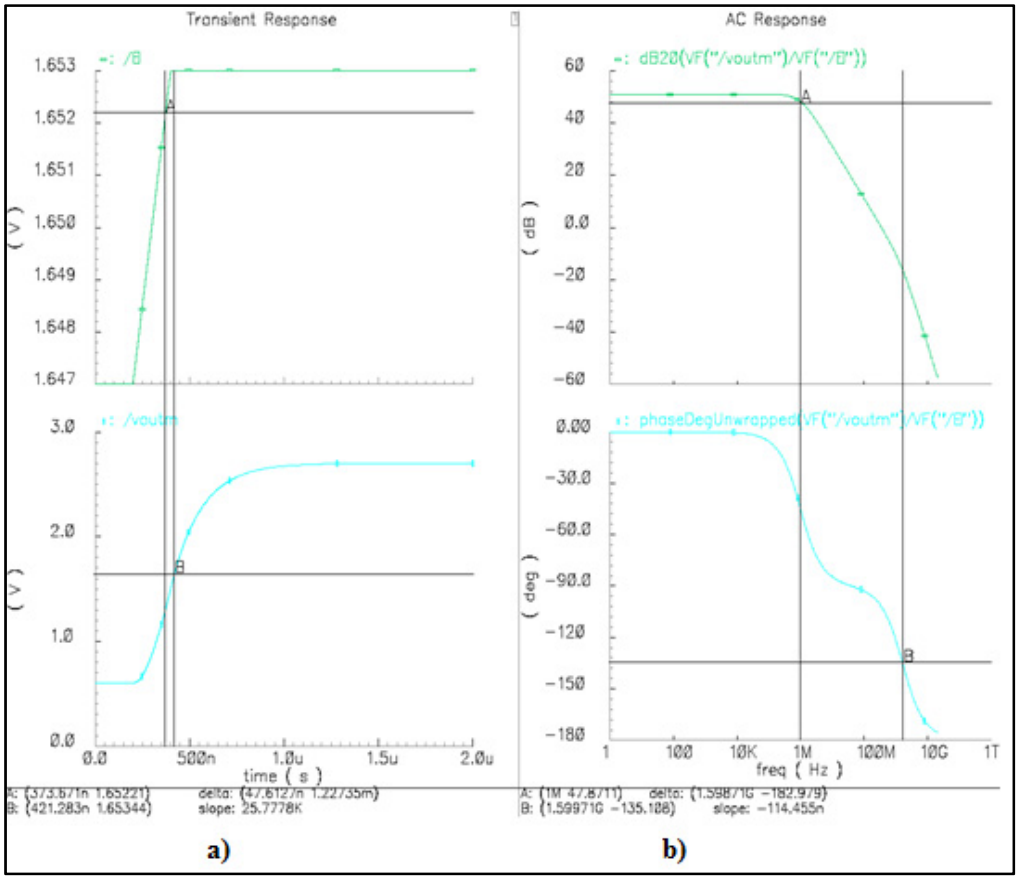

Figure 3. Operational Amplifier transient (a) and AC (b) responses

5. Results

We summarize the simulation results of the differential SH shown in Figure 4 using *CADENCE*.

5.1 Differential SH Architecture

This architecture consists of the Operational Amplifier configured differentially. On each of the two input terminals of Operational Amplifier, there are four identical MOS switches. However, these four switches are controlled differently as shown in Figure 5. Schematic of the architecture as it was used in the simulation in C*adence* tool which is shown in Figure 4. We choose this particular architecture because of its dynamics, its differential structure minimizing parasite noise and its common mode rejection as detailed by Dzahini and Ghazlane (2003).

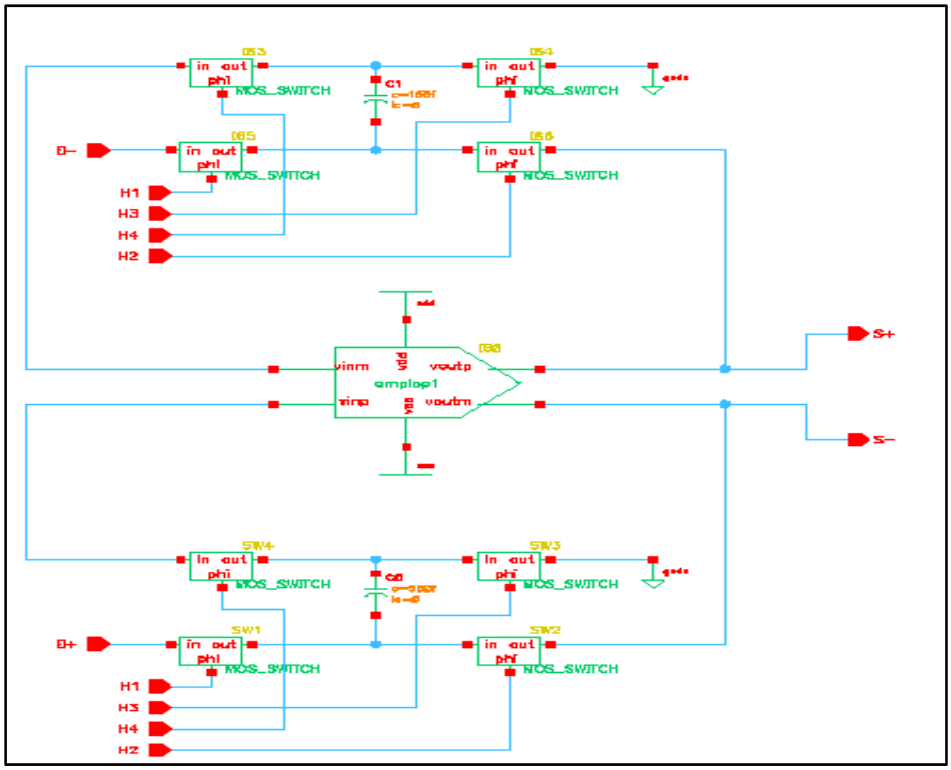

Figure 4. Differential SH architecture

5.2 Clock Sequences

The SH clock are set to minimize clock noise; the sequencing is shown in Figure 5.

To this effect the switch connected to the ground must be the first to open. We chose in all clocks to have the same frequency. The clock operation mode is as follows:

- Sampling phase: first H_3 activation then H_1 while H_2 and H_4 in OFF
- Hold phase: first H_4 activation then H_2 while H_1 and H_3 in OFF

This operation mode aims precisely to minimize the amount of injected charges as explained in section 3.2.1.

Switches connected to the ground the first switch. This can prevent the injected charges are proportional to the input signal and thus the injected charges are minimized.

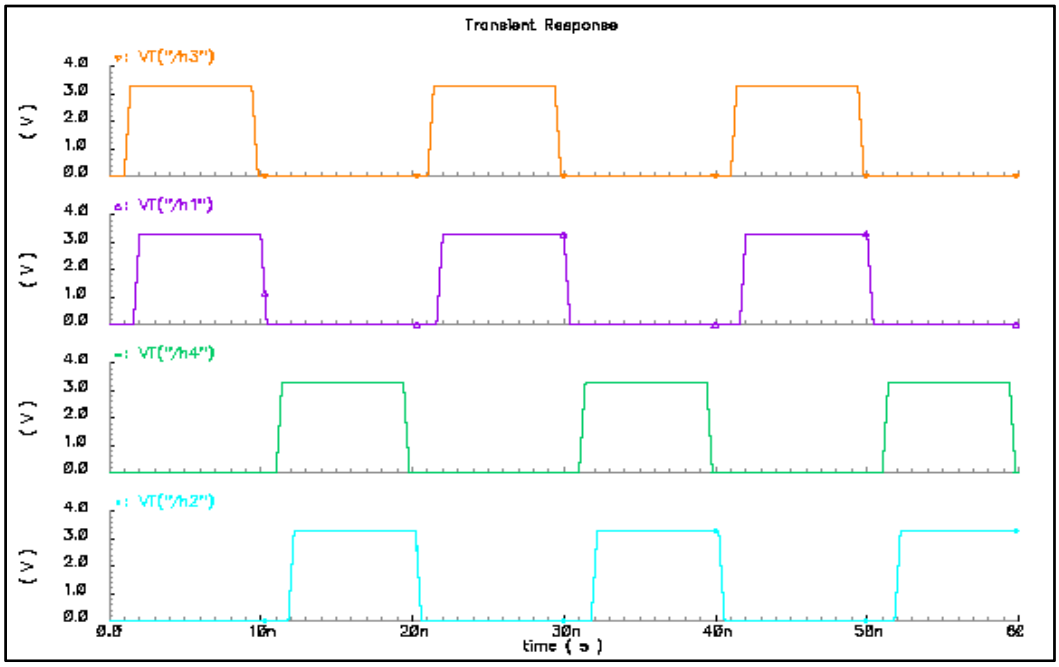

Figure 5. Clock sequencing

5.3 Offset Influence on the SH Non-Linearity (NL)

We are here interested in the SH non-linearity for different Operational Amplifier offset values. Actually we measured the error percentage NL for different offset on the input signal as described in the relation:

$$NL = \left(\frac{Vr - Vi}{Vi}\right) \times 100 \quad (4)$$

Where V_r is the measured output and $V_i$isideal output value.

Figure 6 shows the variation of the SH non-linearity for different values of Operational Amplifier offset.

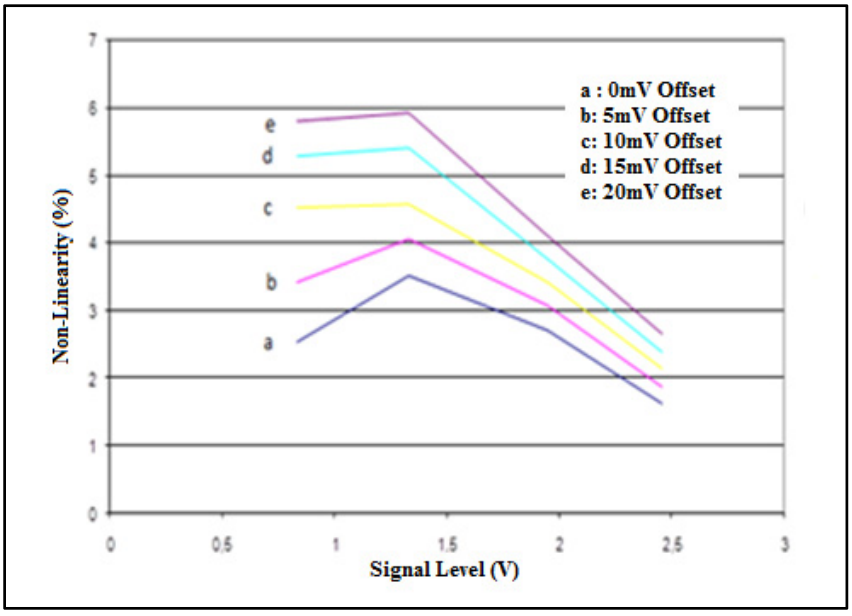

Figure 6. SH non-linearity for different Operational Amplifier offset

As depicted, the SH non-linearity is strongly related to the Operational Amplifier offset and is maximal around the common mode.

5.4 Stray Capacity Influence on the SH

We investigate the stray capacity influence on SH behavior according to the SH differential architecture (Figure 4). We are interested in output attenuation depending on the stray capacities as depicted below in Figure 7.

The Figure 7 shows that the stray capacity increases induced attenuation. The magnitude of this attenuation is about 0.1 mV/fF. Therefore the sampling error increases with the stray capacity.

The divider bridge formed by the stray and storage capacities contributes this attenuation. However the question is that between divider bridge and injected charges influences the greatest.

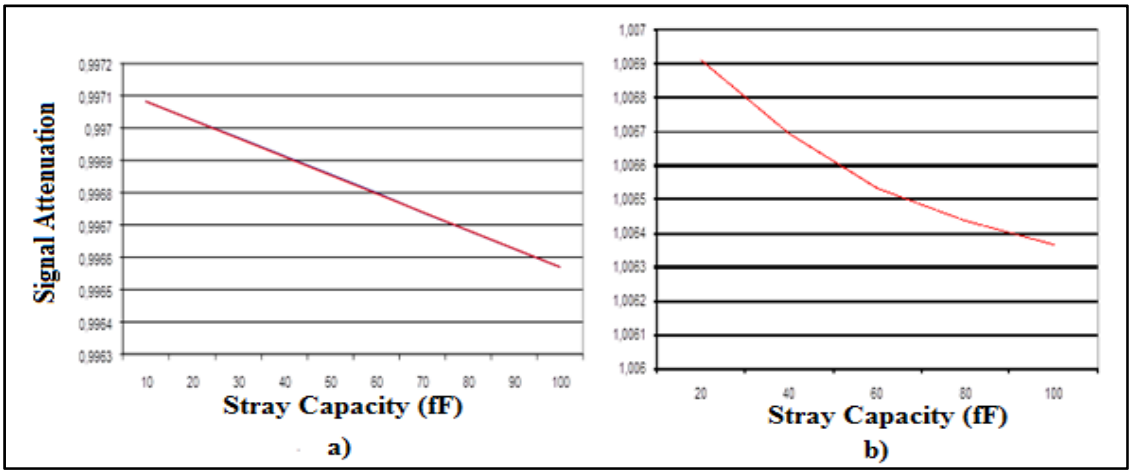

Figure 7. Measured SH signal attenuation variation b) versus theoretical a) for different stray capacities

5.5 Injected Charges Influence

To evaluate the injected charges influence, we first consider the SH shown in Figure 4 with the Operational Amplifier offset null; with the aim of having only the injected charges contributing. The Figure 8 shows an output value during the hold phase different from the expected value. In fact for the sampling related to Figure 8, there is a difference of 48 mV, due to the injected charges and the clock noise since the offset is null. The presence of glitches during commutation (ON/OFF or OFF/ON) also confirms the presence of injected charges.

A closing and opening of the switches, the charges present in the channel continue on their way. This explains the presence of glitches in switching. The glitches affect the accuracy of the sampling and therefore the accuracy of the ADC becomes worse.

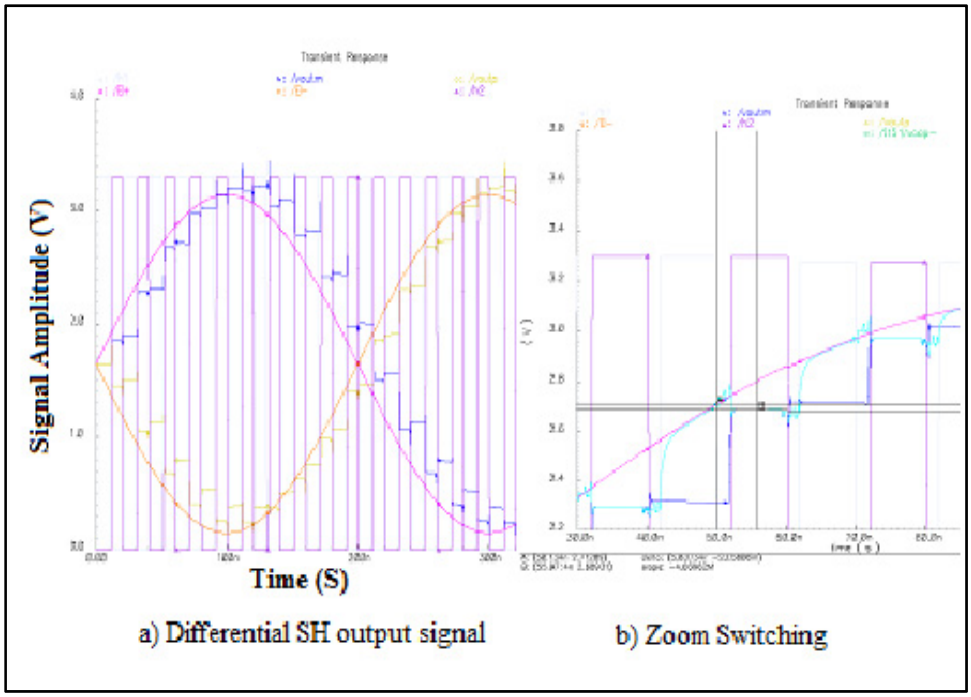

Figure 8. Effect of injected charges

6. Conclusion

The SH is a key component in the analog to digital conversion; therefore it is important to be able to control its behavior relatively to some characteristic parameters of its environment. Our study is based on a mixed SH behavioral-analog description. In fact the Operational Amplifier is entirely behavioral but described in *Verilog –A;* while the CMOS switches and capacitors are analog component from the *Cadence* libraries. Despite the simulation's limitations this work clearly helped us gain insight in the injected charges and clock noise effect on the SH. Furthermore the injected charges effect and clock noise are closely related. This study has shown the Operational Amplifier offset is more apparent on small signals and adversely affects the SH precision especially around the common mode.The stray capacity attenuates the SH output and therefore increase the sampling error.

In perspective this study lays ground for simulating a chain of ADC pipelines using behavioral differential Operational Amplifier and SH models developed.

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