Novel and general carbon nanotube FET-based circuit designs to implement all of the $3^9$ ternary functions without mathematical operations

Peiman Keshavarzian*

Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran

1. Introduction

Most computational operations today are performed with only two logical states (0 and 1). Multiple-valued logic (MVL) replaces the characterization of variables in the binary number system with higher-based systems such as ternary [1].

Ternary logic (or three-valued logic) (TVL) has attracted substantial interest due to several important advantages over binary logic in the design of digital systems [2,3]. For example, more information can be transmitted across the same communication channel or stored for a given register length. A reduction in chip area, the complexity of interconnections and power dissipation are some of the advantages that can be achieved [4]. Furthermore, serial and serial–parallel arithmetic operations can be performed faster, and more operative error-detection and error-correction codes can be employed in ternary logic implementations.

The carbon nanotube FET (CNTFET) alternatives to bulk silicon transistors are of particular interest. CNTFETs are promising for increased performance due to a unique one-dimensional band structure that displays near-ballistic transport and low OFF-current properties [2–10]. The design of a high performance universal TVL cell based on a CNTFET can result in low-power, fast-programmable logic circuit implementations such as CPLDs or FPGAs. Inefficient use of the chip area, low speed and high power consumption due to electronic switches are major problems with programmable ICs. A universal TVL cell has been presented in [11]. In this paper, new designs using ternary valued-logic and nanoscale CNTFETs are proposed. Therefore, future programmable logic ICs with low power and high speed properties can be achieved with minimal chip area. Two universal TVL cells based on CNTFETs with a resistive voltage divider are proposed in this paper. We know that the resistor is an undesirable element in the manufacturing process of ICs due to high power consumption and large dimension. Hence, the voltage division is performed by two CNTFETs (i.e., a pass gate).

In the CNTFET, the threshold voltage of the transistor is determined by the carbon nanotube diameter. Therefore, different threshold voltages for CNTFETs can be implemented by growing CNTs with different diameters (chirality vector). This quality makes CNTFETs an ideal platform to bring MVL to electronic chips [12–17]. CNTFET-based universal TVL cell designs with optimized threshold voltages are proposed and compared to previous implementations of universal cells. Extensive simulations with HSPICE are performed to show the impact of supply voltage and room temperature variations. Simulation results show that the proposed universal TVL cell with pass gate voltage division has better performance in terms of power consumption and delay compared with previous resistive-load CNTFET universal TVL implementations.

2. Carbon Nanotube FET

CNTFETs using semiconductor single-wall carbon nanotubes (SWCNTs) are used to build electronic circuits. Their properties are...
similar to MOSFETs. A SWCNT is a cylindrical shape made by a simple mechanized processing device and is an extremely promising choice over current MOSFETs. Whether the SWCNT has metallic or semiconductor characteristics contributes to its electrical properties, which depend on the angular arrangement of atoms along the tube. This arrangement is based on a chirality vector with a pair of integers \((m, n)\), i.e., the nanotube is metallic if \(n=m\); otherwise, the tube is a semiconductor. The CNT diameter is calculated by eq. (1), which is a function of \(m\) and \(n\) [18]. Fig. 1 shows a diagram of the CNTFET [18].

\[
D_{CNT} = \frac{\sqrt{3a_0}}{2} \sqrt{n^2 + m^2 + nm}
\]  

(1)

The threshold voltage has been defined as the voltage needed to turn the transistor on. The voltage of the CNT channel is approximately half of the band gap and is inversely related to the nanotube diameter [19].

\[
V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}}
\]  

(2)

\(D_{CNT}\) is the CNT diameter, \(e\) is the unit electron charge, \(E_g = 3.033\) eV is the carbon \(\pi-\pi\) bond energy in the tight bonding model, and \(a = 2.49\) Å is the carbon-to-carbon atom distance. For example, the threshold voltage of the CNTFETs that use \((19, 0)\) CNTs as channels is 0.289 V because the \(D_{CNT}\) of a \((19, 0)\) CNT is 1.49 nm. Simulation results have acknowledged the validity of this threshold voltage. Because the vector changes, the CNTFET threshold voltage will also change. The threshold voltage of the CNTFET is inversely related to the CNT chirality vector. The threshold voltage of the CNTFET using \((13, 0)\) CNTs at a gate length of \((19, 0)\) is 0.289 V. Fig. 2 shows the threshold voltage of both P- and N-type CNTFETs obtained from (2) and HSPICE simulation results for various chirality vectors (various \(n \) for \(m=0\)).

The current–voltage (I–V) characteristic of the CNTFET with different gate lengths is shown in Fig. 2, which shows that the I–V characteristics of the CNTFET are similar to those of the MOSFET. The CNTFET circuit current is saturated at higher \(V_{ds}\) (drain to source voltage) as the channel length increases, as shown in Fig. 3. The energy quantization in the axial direction at a 32-nm (or less) gate length causes the on-current to decrease, as expected [18].

3. Proposed designs

Two designs of universal TVL cells based on CNTFETs with high speed and low power consumption are presented. The first cell, with 16 N-type CNTFETs, is shown in Fig. 4. In this cell, voltage division is performed by two resistors, which increases the power consumption and makes the chip manufacturing process difficult.

Referring to the table of ternary logical functions (Table 1), we observe that each of the branches is used to achieve a state of the table.

For example, the branch named “1” is connected to ground if T1 and T5 are turned on. This means that inputs A and B are equal to “0”, which is implemented in the first step, according to the table. For a logical “0” in output, the related branch connects to “zero”, so we have “0” in the output. By changing to a logical “1”, the
corresponding branch connects to “one”, and the output will be equal to 1/2 \( V_{dd} \). Bear in mind that resistors are performing the voltage division. Finally, for a logical “2”, the related branch is floating because \( V_{dd} \) is connected to the output by R1.

In this design, a standard ternary inverter (STI) [6] is used to produce an inverse of INA and INB, which is connected to the gate of some , such as T6 and T7. Fig. 5 shows the STI circuit.

The second design of the universal TVL cell is presented in this paper. In this universal cell, 32 CNTFETs are used to implement all of the ternary functions that are shown in Fig. 6. The 16 NCNTFETs on the bottom perform a similar function to the previous design, and 16 PCNTFETs are used to achieve a logical “2” with less power consumption.

When a logical “0” is required according to the table, a namesake branch of the NCNTFET is connected to the output, and the related PCNTFET branch remains floating. To implement the logical “1”, the PCNTFET branch connected to “ONE2” and the NCNTFET branch connected to “ONE1” give a logical “1” in the output, and the voltage distributor in the output will produce 1/2 \( V_{dd} \). Voltage division is accomplished by R1 and R2, which pull the output voltage down to \( V_{dd}/2 \). Finally, for a logical “2”, a namesake branch of the PCNTFET is connected to the output, and the related NCNTFET branch remains floating.

The inverse of INA and INB is performed by the STI circuit that is shown in Fig. 7. In this inverter, T1 controls \( V_{dd} \), while logical “0” is required. Thus, the power consumption is lower than for the previous STI (Fig. 5).

A ternary universal circuit based on CNTFETs is proposed. The circuit has 32 transistors that consist of 16 NCNTFET and 16 PCNTFET transistors, according to Fig. 8.

To compare this design with the earlier designs, we used pass gate voltage division instead of resistor voltage division; thus, this circuit uses far less power, and it is possible to place all of the elements of the universal cell on a chip. The logical “0” control task is responsible for the NCNTFET network, and the logical “2” is controlled by the PCNTFET network. To achieve a logical “0”, the NCNTFET branch is connected to the output, and the PCNTFET branch remains floating. When a logical “1” is required, the related branch in the NCNTFET is connected to “ONE1”, and the same PCNTFET branch is connected to “ONE2”. Finally, for a logical “2”, the PCNTFET branch is connected to the output, and its NCNTFET branch is floating. Thus, all of the TVL functions have been performed in the same way as in the second design. Simulation

![Fig. 4. Schematic diagram of a 16 T CNTFET-based universal TVL cell.](image)

Table 1
Truth table of universal ternary logical functions.

<table>
<thead>
<tr>
<th>B\A</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>i</td>
<td>j</td>
<td>k</td>
</tr>
<tr>
<td>1</td>
<td>l</td>
<td>m</td>
<td>n</td>
</tr>
<tr>
<td>2</td>
<td>o</td>
<td>p</td>
<td>q</td>
</tr>
</tbody>
</table>

![Fig. 5. Schematic diagram of the CNTFET-based STI proposed in [6].](image)
of the circuits for 10 random and Gödel functions for the previous and proposed designs has been performed. The simulation results by using HSPICE are shown in Figs. 9 and 10 and Table 2. These results demonstrate that the proposed design has better performance in terms of power consumption and delay than the previous designs.

The inverse of INA and INB is performed by the STI circuit that was proposed in [18]. The STI inverter is shown in Fig. 11 and is implemented by 6 T CNTFET. This inverter has better performance compared with previous STIs in terms of delay and power consumption [18].

The output of the proposed design for a random function and its logical table is shown in Fig. 12. In the first step (0 to 10 ns), input A is a logical "0", and input B is a logical "2" (0.9 V). For implementation of this step "0" node, the NCNTFET units of the universal cell are connected to the output because, according to the logical table (Table 3), the output is a logical "0". Thus, in this step, T17 and T21 turn on and pull the output voltage down to "0". The output of the universal cell for the second step (A = 1, B = 0) is a logical "I" in the logical table and is implemented by the connection of the "I" node to "ONE1" in the NCNTFET unit and the connection of the namesake node to "ONE2" in the PCNTFET unit. In this step, T6, T10, T11, T22, T26 and T27 turn on, and the voltage division is performed by T33 and T34, which pull the output voltage down to 1/2 \( V_{dd} \) (logical "I"). Other states are obtained by these techniques.

Observing that the output of the circuit is full swing, the result shows that we used both types of CNTFET, PCNTFET and NCNTFET, to achieve a better control circuit.

4. Circuit optimization

Because the CNTFET transistor threshold voltage varies with the diameter of the nanotube, by changing the diameter of the nanotube or the CNTFET chirality, we can design circuits with different threshold voltages. Universal cells of a given design chirality \( n_1 = 19 \) and \( n_2 = 9 \) and a threshold voltage of 0.559 and 0.289, respectively, provide for use of N- and P-type CNTFETs. If the chirality of a CNTFET with a high threshold voltage and a low threshold voltage define \( n_i \) and \( n_j \), respectively, and \( m \) chirality is common to both CNTFETs, we can define \( (n_i, n_j, m) \) as the ternary index.

For example, for a CNTFET with a high threshold voltage when \( n = 10 \) and a low threshold voltage when \( n = 21 \), the ternary vector \((10,21,0)\) is defined. Extensive simulations for a random ternary
function with different ternary indexes on universal cells were performed until the optimal chirality for the final proposed design was obtained.

The simulation results are shown in Table 4. Observe that the universal cell for the ternary vector (9, 22, 0) has the best performance.

5. Impact of variations

Changes in supply voltage and temperature are important issues in the design of digital circuits. Systematic changes in the supply voltage and temperature are a major challenge in the design of electronic devices in terms of energy and delay. An extensive simulation was performed by HSPICE to specify the effect of temperature and supply voltage on the last universal TVL cell. Simulations for six different voltages (0.6, 0.9, 1.2, 1.5, 1.8, and 2.1) were performed. We also simulated temperature at each voltage change between seven different values (0, 9, 18, 27, 36, 45, and 54). Fig. 13 shows the power delay product (PDP) with different supply voltages and temperatures for the last proposed universal cell based on CNTFETs. In the CNTFET, due to ballistic transport, the power delay product variation of the CNTFET resulting from temperature and supply voltage variations is very small.

Thus, the CNTFET is very robust to systematic variations in voltage and temperature. However, the simulation result in Fig. 13 shows that the impact of temperature variations is much smaller than that of voltage variations and that the universal TVL cell is insensitive to systematic temperature and voltage variations overall.
Table 2
Transient PDP of CNTFET-based universal TVL cells.

<table>
<thead>
<tr>
<th></th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
<th>F6</th>
<th>F7</th>
<th>F8</th>
<th>F9</th>
<th>F10</th>
<th>Godel &amp;</th>
<th>Godel</th>
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<tbody>
<tr>
<td>Design2</td>
<td>1.44786E-16</td>
<td>4.68092E-17</td>
<td>1.01653E-16</td>
<td>1.0132E-16</td>
<td>9.01743E-16</td>
<td>1.26546E-16</td>
<td>4.61066E-17</td>
<td>1.53746E-16</td>
<td>52.054E-16</td>
<td>46.169E-16</td>
<td>10.731E-16</td>
<td>7.46793E-17</td>
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<tr>
<td>Proposed design</td>
<td>3.29522E-17</td>
<td>1.04362E-17</td>
<td>2.31257E-17</td>
<td>2.22424E-17</td>
<td>2.06481E-17</td>
<td>1.77249E-17</td>
<td>1.57185E-17</td>
<td>2.37179E-17</td>
<td>2.71465E-17</td>
<td>1.27619E-17</td>
<td>1.91476E-17</td>
<td></td>
</tr>
</tbody>
</table>
6. Conclusion

In this paper, we use CNTFET characteristics to propose a new universal circuit design. This design presents all operational ternary MVL functions ($3^3$) with two inputs. All of the operational MVL functions in the ternary universal field era can be described.

![Schematic diagram of the CNTFET-based STI proposed in [19.]](image)

**Fig. 11.** Schematic diagram of the CNTFET-based STI proposed in [19].

![Transient response of a random ternary function.](image)

**Fig. 12.** Transient response of a random ternary function.

<table>
<thead>
<tr>
<th>(A/B)</th>
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<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

**Table 3**
Logical table of a random ternary function.

<table>
<thead>
<tr>
<th>A/B</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Triple index</th>
<th>Power (ps)</th>
<th>Delay (ps)</th>
<th>PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>(9, 19, 0) CNTFET universal cell</td>
<td>2.6446E-08</td>
<td>26.257</td>
<td>6.94393E-19</td>
</tr>
<tr>
<td>(9, 18, 0) CNTFET universal cell</td>
<td>3.4408E-08</td>
<td>29.618</td>
<td>1.0191E-18</td>
</tr>
<tr>
<td>(9, 17, 0) CNTFET universal cell</td>
<td>2.9531E-08</td>
<td>33.529</td>
<td>9.9045E-19</td>
</tr>
<tr>
<td>(9, 16, 0) CNTFET universal cell</td>
<td>4.3295E-08</td>
<td>43.796</td>
<td>1.8961E-18</td>
</tr>
<tr>
<td>(9, 20, 0) CNTFET universal cell</td>
<td>2.5356E-08</td>
<td>23.023</td>
<td>5.8377E-19</td>
</tr>
<tr>
<td>(9, 21, 0) CNTFET universal cell</td>
<td>2.6542E-08</td>
<td>21.486</td>
<td>5.7028E-19</td>
</tr>
<tr>
<td>(9, 22, 0) CNTFET universal cell</td>
<td>2.7234E-08</td>
<td>19.727</td>
<td>5.3724E-19</td>
</tr>
<tr>
<td>(8, 19, 0) CNTFET universal cell</td>
<td>2.4271E-08</td>
<td>26.011</td>
<td>6.3131E-19</td>
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<tr>
<td>(7, 19, 0) CNTFET universal cell</td>
<td>2.5705E-08</td>
<td>26.683</td>
<td>6.8588E-19</td>
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<tr>
<td>(10, 19, 0) CNTFET universal cell</td>
<td>3.8398E-08</td>
<td>27.288</td>
<td>1.0532E-18</td>
</tr>
<tr>
<td>(11, 19, 0) CNTFET universal cell</td>
<td>1.3277E-07</td>
<td>30.023</td>
<td>3.9861E-18</td>
</tr>
</tbody>
</table>

**Table 4**
Table of properties for different triple indexes.

![Power delay product of the CNTFET universal cell versus power supply and temperature variations.](image)

**Fig. 13.** Power delay product of the CNTFET universal cell versus power supply and temperature variations.
using the new universal circuit designs. For each combination of inputs expected, the voltage division connects to the output joint, resulting in a progressive reduction in delay and power consumption. Therefore, we achieve progressive improvements in the circuit speed.

References