1.8 dB NF 3.6 mW CMOS active balun low noise amplifier for GPS

Y. Ji, C. Wang, J. Liu and H. Liao

A 1.227 GHz low power single-ended input, differential output low noise amplifier (balun LNA) for GPS is proposed. A two stage structure with current-reused technique is adopted to achieve low power, low noise factor and high voltage gain simultaneously. The LNA is fabricated in 0.18 μm CMOS process, consuming only 2 mA current from a 1.8 V supply. The LNA is measured to exhibit a differential voltage gain of 30.4 dB and a noise figure of 1.8 dB.

Introduction: Global positioning system (GPS) is a satellite based navigation system, which provides navigational information, such as the absolute position, velocity, and time for consumers. GPS applications are dramatically increasing in the navigation and location service market. In these applications, GPS receivers with low power, low noise, low cost and high integration are highly desirable [1–3].

In GPS receivers, a fully-differential approach is usually preferred to an unbalanced one for its higher immunity to common-mode noise, rejection to parasitic couplings and increased dynamic range. However, since the receiver’s input signal from the antenna is usually an unbalanced one, it is desirable to split it into two differential signals opposite in phase and equal in amplitude.

Some designers use off-chip baluns to generate differential signals. However, the external balun increases system cost and causes extra gain and noise figure (NF) degeneration of about 1 dB or even more. To deal with this problem, active balun LNAs are reported to achieve single-end to differential transition within the LNA circuit. References [1–3] are based on a conventional balun LNA, in which one branch is realised with an inductor-degenerated common-source MOSFET (M1) and a cascade MOSFET (M2); the other branch is realised with a common-source MOSFET (M2) amplifying the output of M1 to generate the signal in opposite phase. As M2 and M3 are in different operational condition, their gains are difficult to match with each other under process variation. At the same time, the low voltage gain of M1 makes the noise contribution of M33 significant and deteriorates the overall noise characteristics. Reference [4] is another conventional balun LNA, in which a common-gate MOSFET (Mb1) and a common-source MOSFET (Mb2) are parallelled to realise differential signals. The noise contribution of Mb1 can be cancelled in this structure; however, the device dimension of Mb2 is often much larger than that of Mb1 to make the noise contribution of Mb2 much smaller. As a result, power consumption is increased and the two branches are difficult to be balanced with process variation. This LNA also suffers from low voltage gain as common-gate input-matching is used. In this Letter, we propose a new balun LNA, which can overcome the limitations exhibited above.

Proposed balun LNA: The proposed two-stage balun LNA is depicted in Fig. 1. The first stage of the proposed balun LNA has a common-source common-gate (CS-CG) inductive degeneration topology, where C1 is used together with Ls and Lg to obtain power-constrained simultaneous noise and input matching [5, 6]. In the second-stage, M3 forms a common gate amplifier while M4 forms a common source amplifier. The output of M2 is used as an input to M3 and M4 via C4. The second stage (M3 and M4) reuses the current of the first stage, which guarantees a low power performance of the new structure. Note that M2 is the common-gate stage of the cascade configuration, used to eliminate the Miller effect and provides a better isolation from the output return signal. As can be seen, the proposed structure realises single-end to differential transition in the second stage and reuses the current of the first stage, which are the main differences between this structure and those of [1–4].

The large inductor L1 is used to provide a high impedance path to block the RF signal from the drain of M2 to the source of M4, and to provide a low impedance path to let DC current flow from M4 to M2. According to the current-reused configuration and proper design, the first stage of the LNA can provide sufficient voltage gain, which restrains the noise contribution from the second stage, so the overall noise performance of the proposed structure can be greatly improved.

To reduce the chip size, L1 is realised with an on-chip stack inductor. The top metal and the next three under metal layers are used to increase the series inductance of the inductor. With metal width of 6 μm, metal spacing of 2 μm, and inner radius of 60 μm, the inductor obtains 24 nH DC inductance and a peak quality factor of 4. Characteristics of the inductor are extracted from electromagnetic field simulation data and a single-π equivalent circuit model is used in the simulation of the proposed balun LNA.

If the transconductance of M3 is equal to that of M4, the drain current of M3 is equal in magnitude and different in polarity to the drain current of M4. A high voltage gain is designed to sufficiently reduce the noise contribution of the following circuits (M3 and M4). The LNA voltage gain is [1]

\[
A_v = g_{m1} R_{load} = \frac{g_{m1} g_{m2}}{g_{m2} R_L} \approx \frac{g_{m2}}{g_{m1}} R_{load}
\]

where \(g_{m1}\) is the effective quality factor of the amplifier’s input match network, which is valid at the series resonance frequency \(f_0\). Since the noise contribution of M3 and M4 is negligible, the LNA’s noise performance is very close to that of a conventional inductor-degenerated single-end structure. So a low noise factor can be achieved with the proposed balun LNA.

Usually, it is difficult to realise low mismatch on gain and phase for the conventional balun LNA in all process, voltage and temperature variation (PVT) corners. However, in the proposed structure of Fig. 1, the same bias points of M3 and M4 and the voltage gain in the first stage help to alleviate the impact of the MOSFETs’ mismatch to the differential outputs.

The input impedance obtained by the off-chip input impedance matching of the LNA can be calculated as [3]:

\[
Z_{in} = j \omega (C_L + L_g) + \frac{1}{j \omega (C_{gsp} + C_1) + \frac{g_m 2}{(C_{gsp} + C_1)}}
\]

where \(C_{gsp}\) and \(g_m\) are the gate source capacitance and the transconductance of M1, respectively. By choosing \(L_s\), \(C_1\) and \(g_m\) appropriately, this real term is matched to 50 Ω.

Experimental results: The proposed balun LNA is fabricated in a 0.18 μm CMOS process with an area of 0.66 mm² including pads. Fig. 2 shows the micrograph of the fabricated balun LNA with test
buffers (not shown in Fig. 1). Measurements are performed with the LNA mounted on an FR-4 PCB.

The LNA is measured at room temperature and 1.8 V supply with 2 mA current consumption. At the working frequency of 1.227 GHz, the measured input return loss $S_{11}$ is lower than $-14$ dB. The differential gain and noise figure are about 30.4 dB and 1.8 dB, respectively, as shown in Fig. 3. The gain mismatch is measured to be 0.25 dB.

![Graph showing gain and NF vs frequency](image.png)

**Fig. 3** Measured voltage gain and noise figure

Table 1 lists comparisons of the proposed LNA and the recently reported CMOS balun LNAs [1–4]. It can be seen that the proposed balun LNA achieves lower noise figure and higher voltage gain with lower power dissipation, compared with prior techniques listed. These results demonstrate its potential for low power, low cost and high performance GPS applications.

<table>
<thead>
<tr>
<th></th>
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<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
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<td>$S_{11}$ (dB)</td>
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<td>$-8$</td>
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<tr>
<td>Power (mW)</td>
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<td>35</td>
<td>3.6</td>
</tr>
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<td>29</td>
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</table>

*Including LNA and MIXER

**Table 1: Performance comparison of active balun LNAs**

Conclusion: A 1.8 dB noise figure balun LNA with a differential voltage gain of 30.4 dB is presented. By employing the current-reuse technique and single-end to differential transition in the second stage, the LNA core achieves a low power consumption of 3.6 mW, and obtains low noise figure and low mismatch. Experimental results show that the proposed LNA is suitable for low power GPS and other applications.

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One or more of the Figures in this Letter are available in colour online.

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**References**