Indian Journal of Pure & Applied Physics
Vol. 43, December 2005, pp. 899-904

Carbon nanotubes field effect transistors : A review

P A Alvi[1] , K M Lal[1], M J Siddiqui[2] & S, Alim H Naqvi[1]

[1] Department of Applied Physics, Z H College of Engineering and Technology, Aligarh Muslim University, Aligarh 202 002
[2]Department of Electronics Engineering, Z H College of Engineering and Technology, Aligarh Muslim University, Aligarh 202 002
*E -mail: parvez_amu@indiatimes.com

Received 25 February 2005; revised 8 October 2005; accepted 18 October 2005

Carbon nanotubes field effect transistors (CNTFETs) are one of the most promising candidates for future nanoelectronics. In this paper, the review of CNTFETs is presented. The structure, operation and the characteristics of carbon nanotubes metal-insulator-semiconductor capacitors have been discussed. The operation and *dc* characteristics of CNTFETs have been presented. In future, we expect the performance of CNTFETs will be better by improving CNT quality and on optimizing device structures.

Keywords: Carbon nanotubes, Field effect transistors, Nanoelectronics
IPC Code: H01F 41/30, G1221/06

1 Introduction

Over the past few years, critical dimensions of silicon transistor devices have decreased dramatically. Prototype transistors with gate length in 30-nm range have been successfully fabricated and were found to exhibit excellent electrical characteristics[1-4]. While there is still some room for further improvements, the consensus is that alternative concepts will become necessary at some point in future[5]. Since the early 1970s the conventional advancement in technology has followed Moore's law (Moore 1975) whereby the number of transistors incorporated on a memory chip doubles every year and a half. This has resulted from continual improvements in design factors such as interconnectivity efficiency as well as from continual decrease in size. The phenomenal progress signified by Moore's law has been achieved through scaling of the metal-oxide-semiconductor field effect transistor (MOSFET) from larger physical dimensions to smaller physical dimensions, thereby gaining speed and density. Shrinking the conventional MOSFET beyond the 50 nm-technology node requires innovations to circumvent barriers due to fundamental physics that constrains the conventional MOSFET.

With the end of silicon transistors scaling, a great deal of research activity is currently focused on identifying alternatives which would enable continued improvements in the density and performance of electronics information systems. Other alternatives for more density and performance of electronics information systems are high dielectric constant (high-k) gate dielectric, metal gate electrode, double-gate FET, and strained-Si FET. High dielectric-constant materials are useful as gate insulators as they can provide efficient charge injection into transistor channels and reduce direct tunneling leakage currents. Of the various materials systems and structures being investigated carbon nanotubes have shown the promising characteristics. Carbon nanotubes are hollow seamless cylinders that can be envisioned as being formed by rolling up a finite sized piece of graphite sheet. Depending on how the roll-up of the graphite sheet occurs during the growth process, carbon nanotubes can exhibit semiconducting as well as metallic character[6]. Moreover, the band gap of the semiconducting tubes scales inversely with the tube diameter[7]. The growth process can be tuned such that fine control of the tube diameter is achieved thereby forming semiconducting tubes with very similar electrical properties. Growth conditions giving the best yield produce carbon nanotubes with a diameter of around 1.4 nm [Ref. 8] resulting for semi-conducting tubes in an energy gap of 0.6 eV.

With respect to electronics applications the small tube size implies that a high packing density of tubes in an array can be achieved in principle. On the other hand, the existence of metallic as well as semiconducting nanotubes points towards a fully carbon nanotubes-based electronics where metallic tubes act as interconnecting wires and semi-

conducting tubes work as active device elements. However, the most important aspect in view of the electrical properties of carbon nanotubes is their one-dimensional (1 dim) character. Because of the confinement of carriers on the cylinder mantle of the tube, a strong quantization of electron and hole states occurs and charge transport in only one 1 dim-sub band (two counting the bands at $\pm k_F$ independently) becomes feasible in this material class even at room temperature. This has an important impact on scattering in these systems. The reduced phase space for scattering events reduces the probability of backscattering and manifests itself in a high conductivity of carbon nanotubes. In addition, the confinement helps to control in particular the transistor off-state when semiconducting carbon nanotubes are used in a field-effect transistor (CNTFET) geometry. Thus carbon nanotube field effect transistors (CNTFETs) are particularly attractive due to the possibility of near ballistic channel transport, easy application of high-k gate insulator and novel device physics. The CNTFETs were simulated by solving the Schrödinger equation using the non-equilibrium Green's function (NEGF) formalism, self-consistently with the poisson equation. Ballistic transport was also assumed. In this paper, a review of vertically scaled carbon nanotubes field effect transistors is presented and it is shown that these devices exhibit excellent electrical characteristics, including steep sub-threshold slope and high transconductance.

2 Carbon Nanotubes MIS Capacitors

A transistor's on current, an important performance parameter, is the product of charge induced by gate and the average carrier velocity, so that first step is to understand the gate-controlled electrostatics of a carbon nanotubes metal-insulators-semiconductor (MIS) capacitor. Theoretical studies of carbon nanotubes electrostatics have focused on two-terminal devices and the electrostatics along the nanotubes direction. In this section, MIS electrostatics of carbon nanotubes capacitors in three different geometries can be analyzed by solving the two dimensional Poisson equation self-consistently with carrier statistics of nanotubes. The results show that for the densely packed array of nanotubes on a planar insulator, the capacitance per tube is reduced due to the screening of the charge on the gate plane by neighbouring nanotubes. In contrast to silicon, planar MOS capacitors, the capacitance is strongly influenced by the nanotube's one-dimensional density-of-states. The results also show that careful electrostatic design will be critical for the performance of CNTFETs. The three nanotubes capacitor structures are discussed, each with a semiconducting nanotubes having a diameter of D=1 nm, are shown in Fig. 1, [Ref. 9]. In third dimension (out of the page) the nanotube is assumed to be connected to ground, which supplies the carriers to balance the charge on the gate. For comparison to silicon MOS capacitor, we assume a silicon doping of $N_A=10^{18}cm^{-3}$, insulator thickness t_{ins}=1 nm and a dielectric constant of κ_{ins}=4. It is important that results be compared at the same gate overdrive, (V_G - V_T), so the gate work functions were selected to produce the same threshold voltage V_T for the CNT and MOS capacitors.

The nanotube capacitance versus gate voltage can be computed as follows. For an assumed potential of the nanotube, the charge density, Q_L, was obtained from

$$Q_L = (-e).\int_{+\infty}^{-\infty} dE.\mathrm{sgn}(E)D(E)f(\mathrm{sgn}(E)[E-E_F]), \qquad \ldots (1)$$

where e is the electron charge, sgn (E) the sign function, D (E), the density-of-states (DOS) of the nanotube and $E_F = eV_{CNT}$ is the position of Fermi level relative to the middle of the energy gap (we assume the intrinsic nanotube), and V_{CNT} is the average potential of the nanotube. A semi-classical approach can be adopted in which the effect of gate voltage is to move the sub-bands of the nanotube rigidly up and down without changing the $D(E)$, the nanotube DOS.

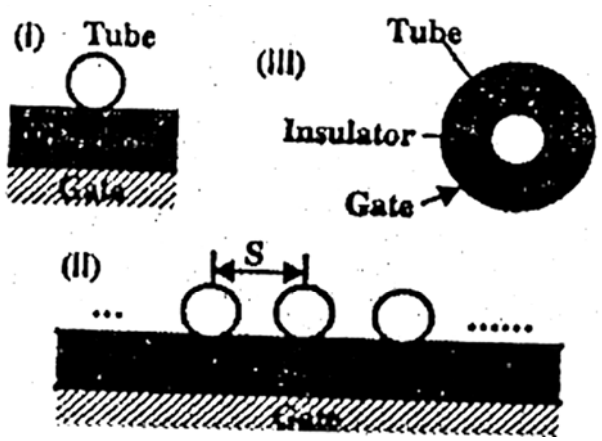

Fig. 1—Three geometries of nanotube MIS capacitors: (i) the nanotube planar capacitor, (ii) a periodic array of nanotubes, and (iii) the coaxially gated capacitor; nanotube diameter D=1 nm, t_{ins}=1 nm, and k_{ins} =4 are the same for all capacitors[9]

This assumption is valid for the co-axial geometry because the cylindrical symmetry produces the same potential for each carbon atom. But for a planar geometry, potential drops across the nanotube can perturb its hard structure. As long as the potential variation across a~1 nm diameter nanotube is below 0.8 V, the effect is small, so use of a 0.4 V power supply, as required for high-density digital systems, suggests that band structure perturbations will be small in this case.

The charge on the nanotube for an assumed potential, the corresponding gate voltage is

$$V'_G \equiv V_G - V_{fb} = V_{CNT} - Q_L/C_{ins}, \quad \ldots (2)$$

where C_{ins} is the gate to nanotube insulator capacitance (a constant independent of gate voltage), V_G, the gate voltage, and V_{fb}, the flat band voltage as determined by the gate metal to nanotube work function difference and any insulator nanotube work function difference and any insulator nanotube surface states. Because V_{fb} depends on species of experimental conditions, all results can be plotted as a function of V'_G except otherwise specified. By solving Eqs (1) and (2) self-consistently, the Q_L (V_G) relation is obtained and the gate capacitance is $C_G = -dQ_L/dV_G$. This procedure is analogous to the one commonly used to compute MOS C_G versus V_G characteristics. Before the C_G versus V_G characteristics can be evaluated, the insulator capacitance must be specified. There is a simple, analytical expression for the coaxial geometry, but planar capacitors require a numerical solution of two-dimensional Poisson equations because two different dielectric constants above the metal plate (the insulator and air) invalidate the simple, analytical expression. The numerical solution was first evaluated for a classical conducting cylinder on the top of an infinite conducting plane with a uniform dielectric material between them, and the result agreed well with the exact analytical solutions. The single nanotube planar geometry, which has two dielectric materials [case (i) in Fig. 1] was then simulated. Two limits were considered; (i) a classical distribution of charge in the nanotube, which assumes the charge redistribute itself to establish an equal potential over the nanotube like a classical metal and (ii) a single sub-band quantum distribution, which assumes that the charge distributes symmetrical around the nanotube. In the classical limit, we find C_{ins} = 0.61 pF/cm and in the quantum limit, C_{ins} = 0.53 pF/cm.

The significant difference between the classical and quantum limits occurs because the quantum charge distribution (the center of the nanotube) is located further from the metal than is the classical charge centroid, and the nanotube diameter is comparable to t_m. Note that in most of the experimental planar nanotube capacitors explored to date the difference between the classical and quantum limits will be small because the nanotube diameter (typically ~ 1 nm) is much smaller than insulator thickness (typically ~ 100 nm). The difference may become important, however, for the very thin insulators that will be used near the scaling limit.

Figure 2 shows the insulator capacitance of an array of parallel nanotubes [case (ii) in Fig. 1] versus the nanotube density, $\rho = 1/S$, where S is the spacing between neighbouring nanotubes. For small packing densities, the capacitance per unit area is proportional to the packing density. The largest capacitance per unit area (still 20%-50% below C_{ins} of the planar silicon MOS capacitor) is achieved when the tubes are closely packed, but increasing the normalized packing density above 0.5, does not result in the proportional increase of capacitance because each nanotube images to a narrower width, therefore, a smaller fraction of the charge on the gate. When the nanotubes are closely packed, the capacitance per tube decreases due to the screening of the gate charge by the neighbouring nanotubes.

Figure 3 (a) shows the one-dimensional (1D) charge density Q_L as a function of the effective gate voltage V'_G for the coaxial nanotube capacitor, which

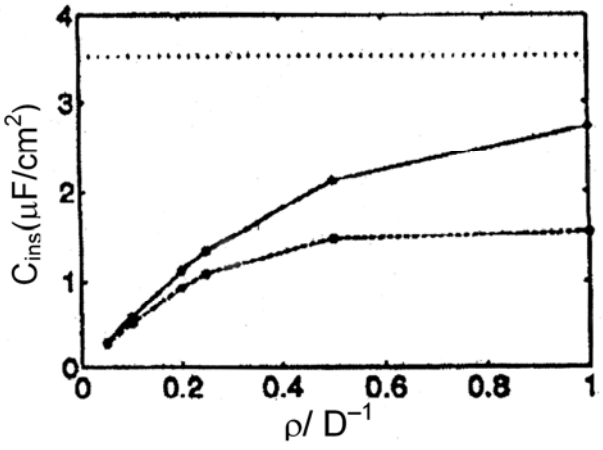

Fig. 2—Insulator capacitance C_{ins} versus the tube density ρ (normalized to ρ_{max}=1/D,the close-packed case) for an array of parallel nanotubes, compared to C_{ins}= K_{ins} ε_0/t_{ins} of the MOS capacitor (dotted line). The solid line assumes classical charge distribution and dash line one sub-band quantum limit.

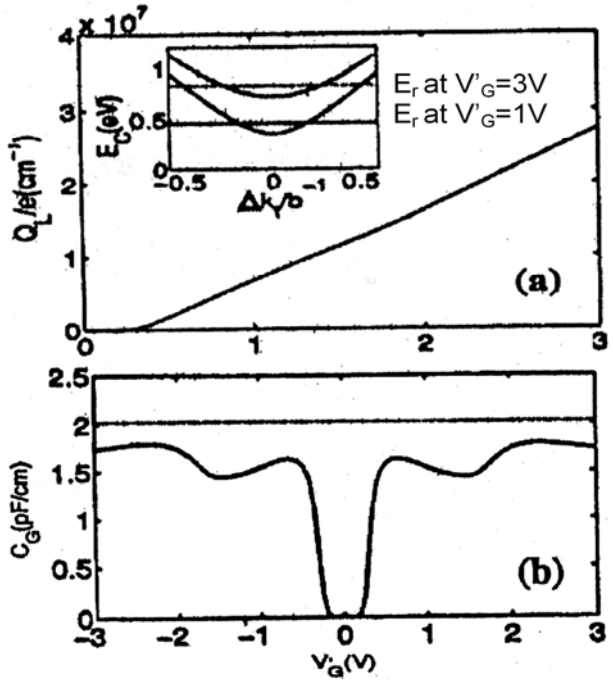

Fig. 3—Charge versus gate voltage for the co-axial capacitor, (a) charge density Q_L and (b) the gate capacitance C_G Vs. the effective gate voltage V'_G. The inset in (a) shows location of the fermi level in the first and second sub-bands as V'_G=1V, and 3V. The dotted line in (b) indicates the insulator the capacitance C_{ins} (Ref. 9).

provides the optimum geometry for gate control in a MISFET. The charge density is approximately linear with gate voltage above the threshold voltage and can, therefore be expressed as $Q_L \approx C_G (V_G - V_T)$. The effective gate capacitance per unit length, $C_G \approx 1.65$ pF/cm, is only 80% of the insulator capacitance, C_{ins} =2.03 pF/cm, because the gate capacitance is the series combination of the insulator and nanotubes. For very large gate voltage (where our semi classical treatments need to be critically examined), electrons occupy the second conduction band as shown in the inset Fig. 3 (a). The sub-band spacing decreases with increasing nanotube diameter, but for typical diameters of about 1 nm and operating voltage of < 0.5 V, only a single sub-band will be occupied. The one-sub band approximation, therefore, can be used in the calculation.

Figure 3(b) shows the computed C_G versus V_G characteristic of the coaxial nanotube capacitor. The striking difference from that for a MOS capacitor on an intrinsic substrate is due to the 1D DOS of the nanotube. The origin of local maxima is apparent when the nanotube capacitance is calculated at zero temperature $C_{CNT}(V_{CNT}) = -dQ_L/dV_{CNT} = e^2 D(e V_{CNT})$,

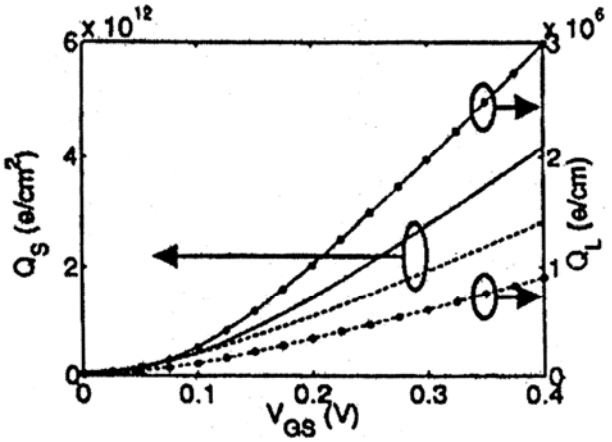

Fig. 4—Charge density versus gate voltage v_G on the left axis, the close packed array of nanotubes (dash line) is compared to the Si MOS capacitor (solid line). On the right axis, the co-axially gated capacitor (solid with circles) is compared to the single nanotube planar geometry (dashed with circles). To make a fair comparison, the gate were function of each capacitor is adjusted to produce a common threshold voltage, $V_T \approx 0.1$V (Ref. 9).

where D (E) is the DOS of the nanotube. Although the peaks in the 1D DOS are smoothed out by temperature, and the insulator capacitor in series, they still display local maxima on the C-V curve at room temperature. Experimental measurement of C-V curves, especially at low temperature using liquid-ion gating which provides a high insulator capacitance, could generate useful diagnostic information on the DOS of the nanotubes.

Figure 4 is an attempt to compare silicon MOS capacitors with carbon nanotubes MIS capacitors. The MOS C_G versus V_G characteristics was computed by a self-consistent Schrödinger-Poisson solver so that quantum confinement effects were included[9]. The same threshold voltage V_T, and the power supply voltage V_{DD}, were assumed for all capacitors. On the left axis, we show that the effective gate capacitance of the nanotube array (the slope of the curve above the threshold) is 66% of that of the silicon MOS capacitor because geometrical effects and the quantum charge distribution reduce the insulator capacitance. (For thicker gate insulator, a planar nanotube capacitor can out perform the corresponding silicon MOS capacitor because the capacitance decreases more slowly with the insulator thickness in the nanotube case). The performance of planar nanotube capacitors may be improved by embedding nanotubes inside the gate insulator which results in comparable performance to the silicon, planar MOS capacitor. On the right axis, we compare the charge

for a single tube in a planar geometry, case (i) in Fig. 1, so that on a coaxial geometry. The result shows a clear advantage for the coaxial geometry and suggests that careful electrostatic design should be important for CNTFETs.

3 Top-gated CNTFET

The Top-gated carbon nanotube field-effect transistors (CNTFETs) have the structure similar to that of conventional silicon metal-oxide semiconductor field-effect transistors (MOSFETs) with gate electrodes above the conduction channel separated from the channel by a thin (15-20 nm) SiO_2 dielectric, as shown schematically in Fig. 5 (a). This geometry allows for operation at low gate voltage, and it also allows for the switching of individual devices on the same substrate.

Most CNTFETs reported use of the conductive substrate as a back gate electrode, usually with gate dielectrics of considerable thickness (~100 nm or more). As a result, high gate voltage is required to switch the devices on. In addition, use of the substrate as a gate implies that all devices are turned on

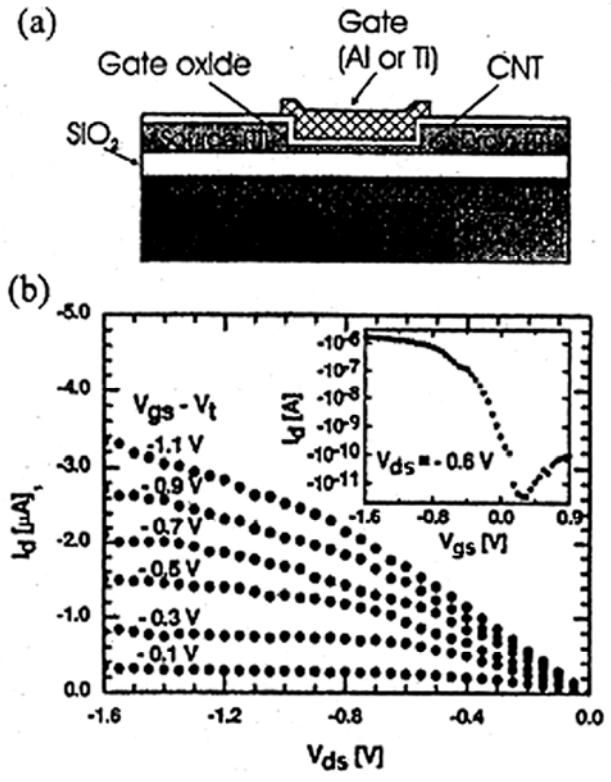

Fig. 5(a)—Schematic cross-section of top gate CNTFET showing the gate and source and drain electrodes (b) Output characteristic of top gate p-type CNTEFT with a Ti gate oxide thickness of 15 nm. The gate and gate voltage values range from –0.1 to –1.1 V above the threshold voltage, which is –0.5 V. Inset: Transfer characteristic of the CNTFET for V_{ds} = -0.6V.

simultaneously, precluding operation of all but the most basic circuits. Recently, Batchold *et al*.[10] reported an improved back-gate structure with a very thin (~2-5 nm) gate dielectric and with individual field effect transistor (FET) gating. Those devices did show low gate voltage operation and individual switch ability. However, the bottom gate structure used in that work, as well as in other previously published CNTFET studies[11-14] has open geometry in which the CNT is exposed to air. This presents electrostatic disadvantages in that the gate insulator capacitance is diluted by the lower dielectric constant of the air surrounding the CNT, the contrast in the top gate geometry the CNT is completely embedded within the gate insulator, offering the full advantage of the gate dielectric. A further disadvantage of the open geometry is that exposure of CNTs to air leads to *p*-type characteristics. Top-gate CNT, on the other hand, allows the fabrication of both *n*-type as well as p-type devices. This becomes possible by virtue of an *in-situ* annealing step prior to the deposition of the gate dielectric film. As pointed out by Dercycke *et al*[15]., thermal treatment in an inert atmosphere modifies the metal-nanotube interface at the contacts and results in *n*-type behaviour. An additional advantage of the top-gate structure is that with only slight modification it can be made suitable for high frequency operation, which is not possible with back-gate devices due to the large overlap capacitance between the gate, source, and drain, these features make the devices presented in this paper the most technologically relevant CNT transistors fabricated so far, and they only allow for a more direct comparison with mainstream silicon-based MOSFETs. Device fabrication is described elsewhere[15] by Derycke *et.al*[15] Single-crystal Si substrates (either *p*-type or *n*-type), with resistivities of 0.005-0.01Ω cm, were cleaned and coated with 120 nm of thermal SiO_2. Single wall nanotubes (SWNTs) produced by laser ablation were dispersed from a 1, 2-dichloroethane solution by spinning onto the substrates after mild sonication. The density of the solution was adjusted to yield approximately one CNT in an area ~5×5 μm^2. Atomic force microscopy of many devices of this type indicates the presence of a single CNT or a CNT bundle comprised of a small number CNTs per device. Ti source and drain electrodes were patterned by electron-beam lithography and lift off. The source-drain separation was 200-300 nm.

Samples were annealed at 850°C for 100 s to form titanium carbide at the metal-nanotube interface,

resulting in a reduced contact resistance. The top gate dielectric was then deposited from a mixture of SiH_4 and O_2 at 300°C. The deposited film thickness was 15-20 nm (+/-5%). Contact holes to the source and drain electrodes were opened in the oxide film, followed by a 0.5 h anneal at 600°C in N_2 to densify the oxide. Gate electrodes were then patterned by electron beam lithography and lift off using ~50nm Al or Ti, followed by a forming gas anneal to reduce trapped charge at the oxide interface. Figure 5(a) shows a cross sectional schematic of the top gate CNTFET structure. Figure 5(b) shows the output characteristic for a *p*-type CNTFET with a Ti top gate and a gate oxide of 15 nm. The device shows excellent turn on and saturation at gates voltage ~1V. The maximum transconductance in 3.25 μS, which is an extremely high value for a CNTFET device as compared to previously reported CNTFETs. The inset in Fig. 5(b) shows the transfer characteristic for the same devices. The linearly extrapolated threshold voltage is -0.5 V and the inverse sub-threshold slope for top gate operation is ~130 mV/decade. As these electrical results are exceptional for CNT-based device, it is believed that it is their performance relative to the *dc* characteristics of state-of-the art planar silicon MOSFETs.

Table 1 gives the key performance parameters for the CNTFET shown in Fig. 5(b) and for two published high performance Si *p*-channel devices, a 15 nm gate length MOSFET built on bulk Si reported by Yu *et al*[16]., which shows very high transconductance, and a 50 nm gate length device reported by Chau *et al*.[17] which is built using this silicon-on-insulator (SOI) technology. Recently intrinsic transconductance of CNTFET has been achieved of the order of 13000 μS/μm, in which CNT was grown by chemical vapour deposition[18]. This is considerably larger than those for state-of-the-art Si-MOSFETs. The restricted geometry of the thin SOI in the second device offers a good comparison for the one-dimensional nanotube channel.

Table 1—Comparison of key device performance parameters for a 260 nm long top gate p-type CNTFET, a 15 nm bulk Si p-type MOSFET, and 50 nm SOI p-type MOSFET (Ref. 15)

	p-type CNTFET	Ref. 16	Ref.17
Gate length (nm)	260	15	50
Gate oxide Thickness (nm)	15	1.4	1.5
V_t (v)	-0.5	~0.1	~0.2
Ion (μA/m)	2100	~–265	650
$V_{ds}=V_{gs}-V_t\simeq$-1V			
I_{OFF} (nA/μm)	150	<500	9
Subthreshold slope (mV/dec)	130	~100	70
Transconductance (μS/μm)	2321	975	650
See refs: 16, 17			

4 Conclusion

The review of carbon nanotubes metal-insulator-semiconductor capacitors are presented. The *V-I* characteristic top-gated CNTFETs are also described. These top-gate devices exhibit excellent electrical characteristics. These electrical characteristics of top-gate CNTFETs also compared to state-of-art silicon devices. For low-volatge, digital applications, the CNTFET with a planar gate geometry provides an on-current that is comparable to that expected for a ballistic MOSFET. Significantly better performance, however, could be achieved with high gate capacitance structures. Therefore, it can be concluded that CNTFETs are one of the most promising candidates for future nanoelectronics.

References

1 Yu B, Wang H, Joshi A, Xiang Q, Ibok E & Lin M R, *IEDM Tech Dig,* (2001).937.
2 Chau R, Kavalieros J, Roberds B, Schenker R, Lionberger D, Barlage D, Doyle B, Arghavni R, Murtthy A & Dewey G, *IEDM Tech Dig,* (2000)45.
3 Wakabayashi H, Ueki M, Narihiro M, Fukai T, Ikezawa N, Matsuda T, Yoshida K, Takeuchi K, Ochai Y, Mogami T & Kunio T, *IEDM Tech Dig,* 2000, p.49.
4 Appenzeller J, Martel R, Avouris P, Scholvin J, Rice P & Solomon, P, *IEEE Electron Dev Lett*, 23 (2002) 100.
5 Frank D J, Dennard R H, Nowak E, Solomon P M, Taure Y & Wong S. Ph, *IEDM Tech.Dig* 2001, p.259.
6 Dresselhaus M, Avouris Ph (Eds.) *Carbon Nanotubes: Synthesis, Structure Properties and Applications,* (Springer, Berlin) 2001.
7 Kane C L & Mele E J, *Phys Rev Lett,* 78 (1997) 1932.
8 Thess A, Lee R, Nikolaev P, Dai H, Petit P, Robert J, Xu C, Lee Y H, Kim S G, Rinzler A G, Colbert D T, Scuseria G E, Tomnek D, Fischer J E & Smalley R E, *Science,* 273 (1996) 483.
9 Guo J, Goasguen S, lundstrom M & Datta S, *Appl Phys Lett,* 81 1486 (2002).
10 Bachtold A, Hadley P, Nakashini T & Dekker C, *Science* 294 (2001) 1317.
11 Tans S, Verschueren A & Dokker, *Nature (London)*, 49 (1998) 393.
12 Martel R, *Appl, Phys, Lett* 73 (1998) 2447.
13 Martel R, *Proceedings IEDM,* 2001, p. 159.
14 Derycke V, Martel R, Appenzeller J & Avouris P, *Nano Lett,* 1 (2001) 453.
15 Derycke V, Martel R, Appenzeller J & Avouris P, *Appl Phys Lett (Unpublished).*
16 Yu B, *Proceedings IEDM,* 2001 p.937.
17 Chau R, *Proceedings IEDM* 2001, p. 621.
18 Nihey F, Hongo H, Ochai Y, Yudasaka M & Iijima S, *Jpn J Appl Phy,* 42 (2003) L1288.