



Low Power Wireless Sensor Networks

<http://www-mtl.mit.edu/research/icsystems/uamps>

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Emerging Networked Applications



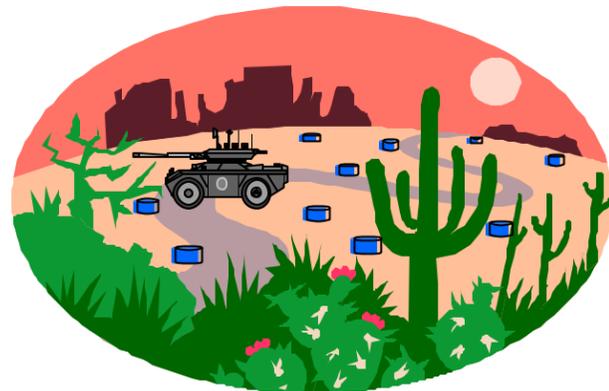
Integrated PDAs



Home/Office Networking
(e.g., Bluetooth)



Sensor Networks



Equipment Monitoring



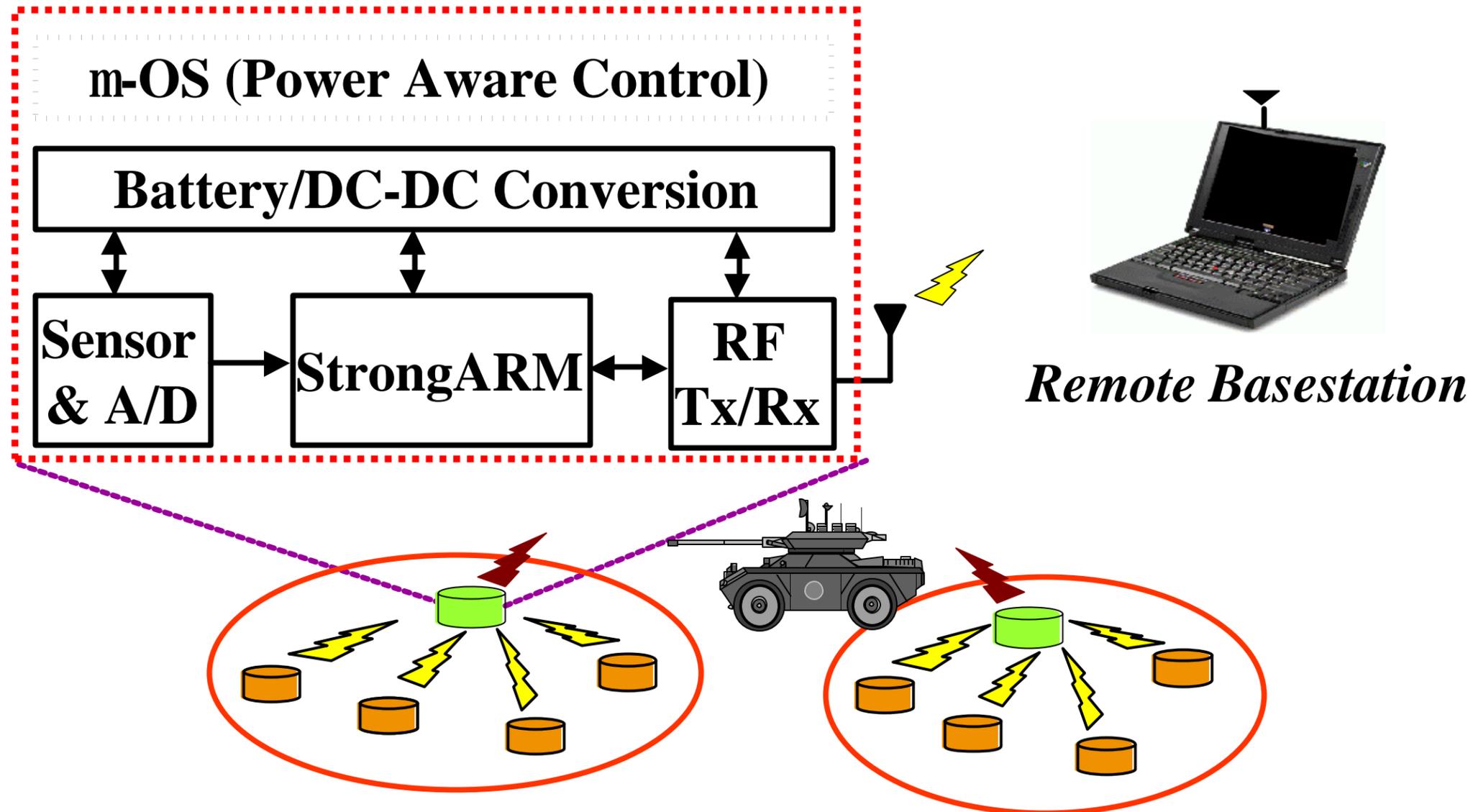
Medical Monitoring



*Integrated **system-on-a-chip** to sense, process and collaborate*



The MIT mAMPS Project



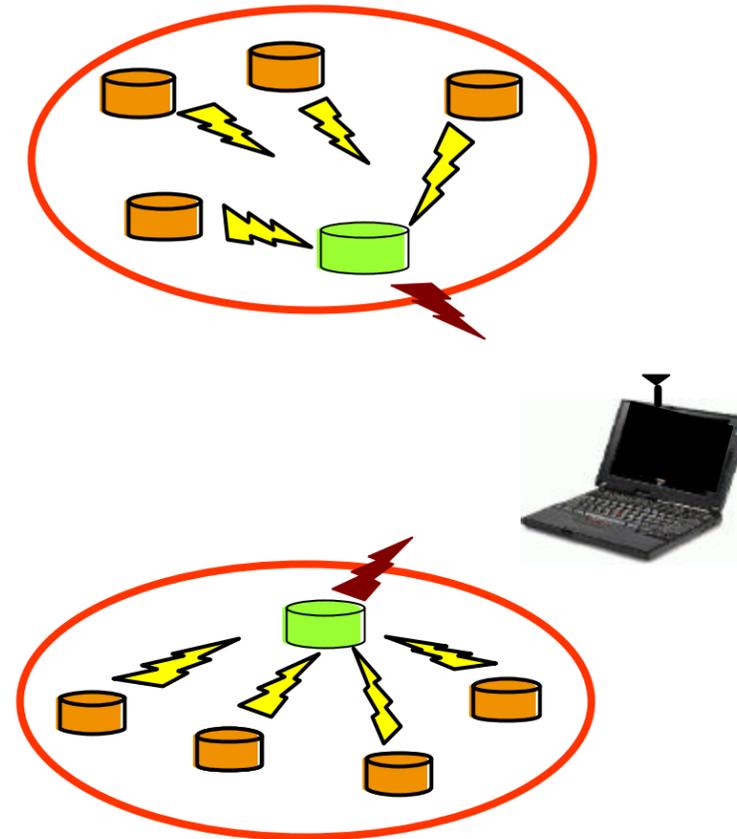
- A **universal substrate** for **power aware** data gathering from a massively distributed wireless network



System Requirements



- **Sensor Types: Low Rate**
(e.g., acoustic and seismic)
- **Bandwidth: bits/sec to kbits/sec**
- **Transmission Distance: 5-10m**
($< 100\text{m}$)
- **Spatial Density**
 - 0.1 nodes/m^2 to 20 nodes/m^2
- **Node Requirements**
 - Small Form Factor
 - Required Lifetime: $> \text{year}$
- **Operational Diversity:**



...from network roles

- Sensor
- Relay
- Data aggregator

...from the environment

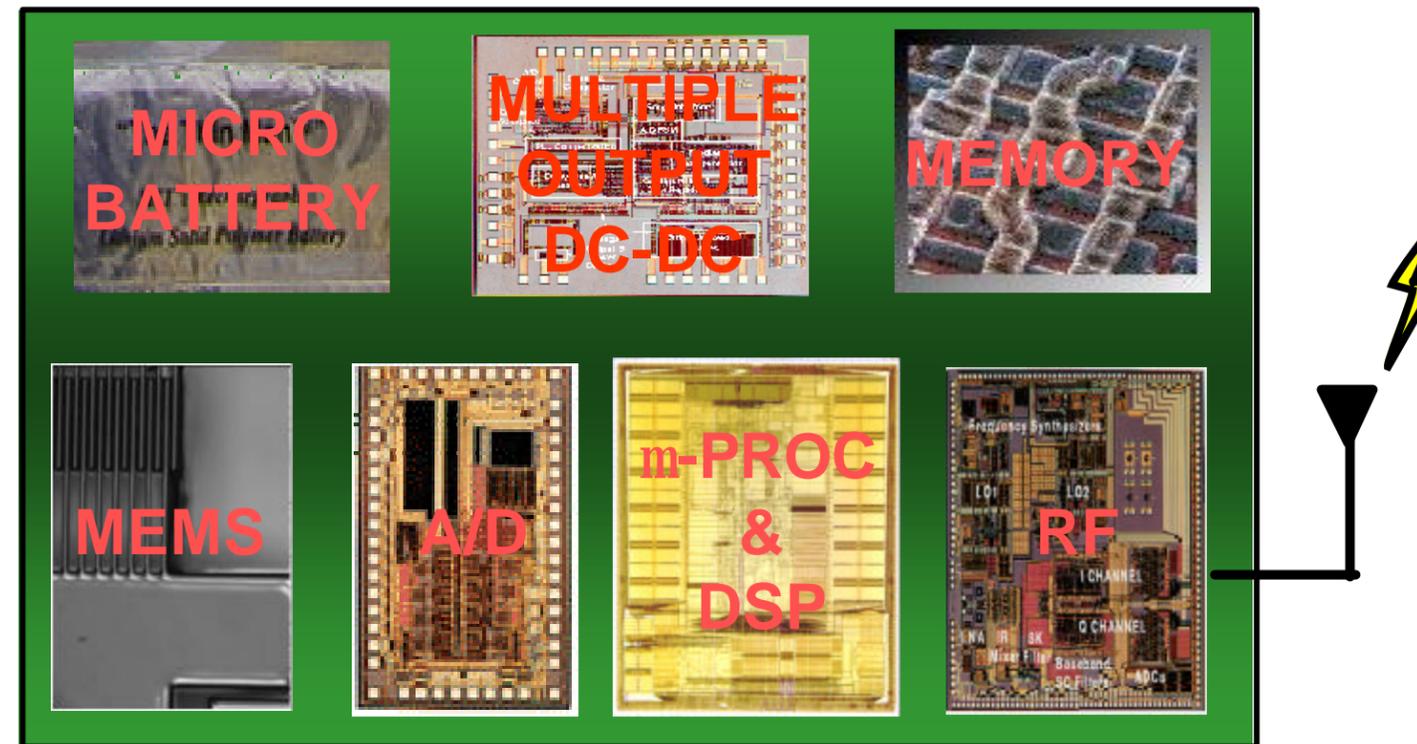
- Event arrival rate/type
- Ambient noise
- Signal statistics

...from user demands

- Tolerable latency
- Result SNR
- $\text{Pr}(\text{Detection})$



Integrated Sensor-Node-on-a-Chip

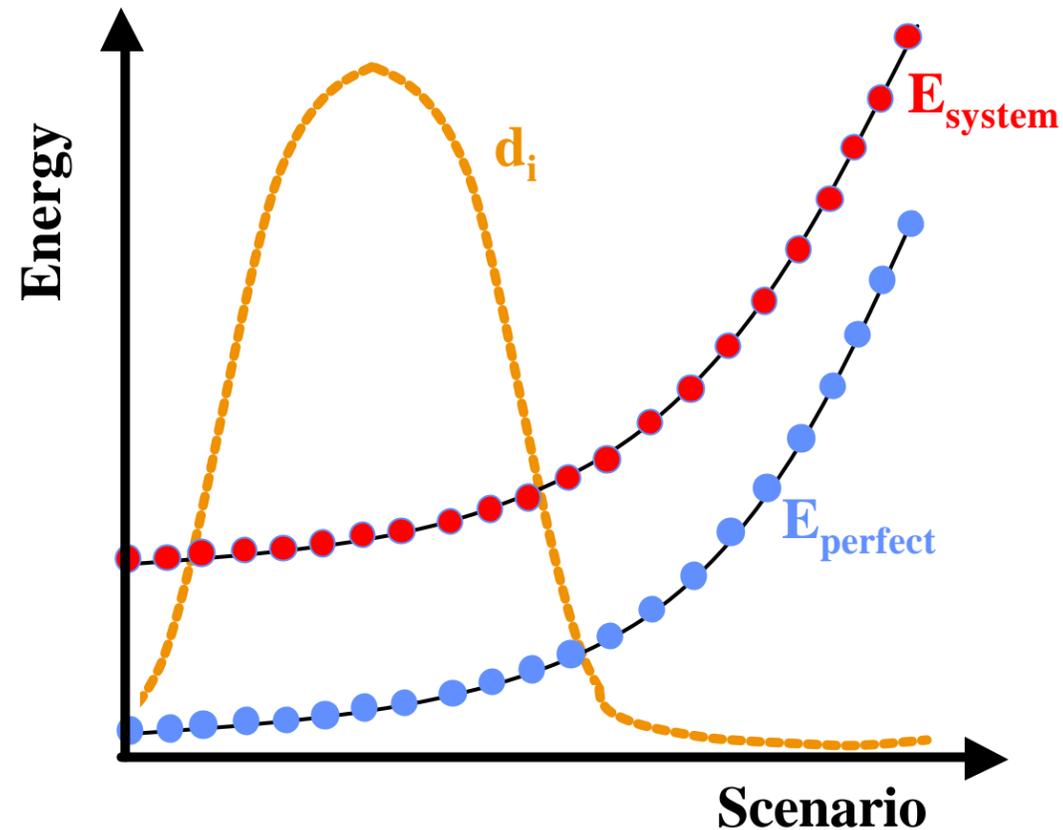


- **Integration** is the key enabler for massively distributed wireless sensing

*What is the best computation/communication fabric?
How coupled should protocol design be to the fabric?*



Power Awareness

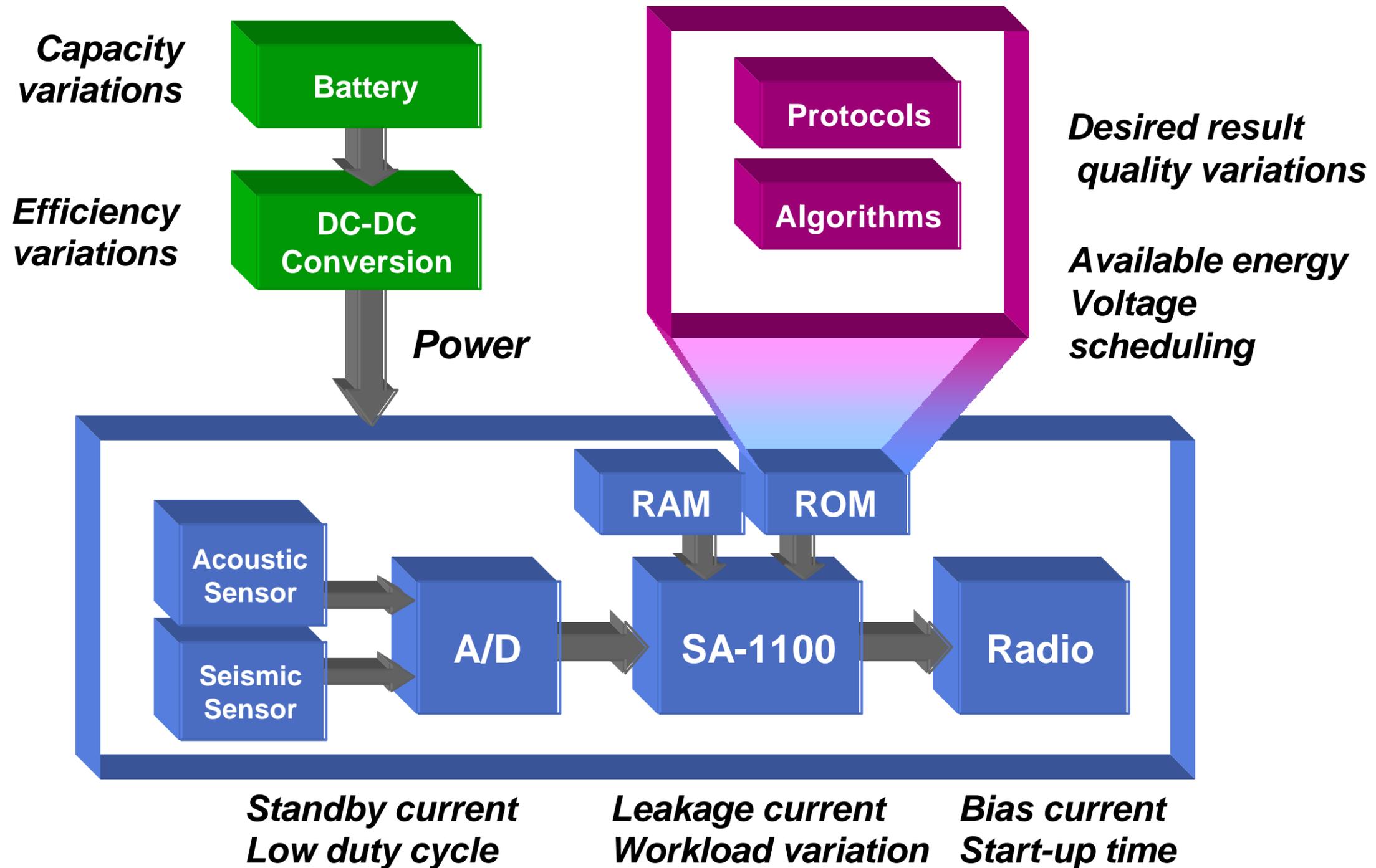


$$\mathbf{h}_{PA} = \left(\frac{\sum_{\text{Scenarios}} E_{system_i} d_i}{\sum_{\text{Scenarios}} E_{perfect_i} d_i} \right)^{-1}$$

- **Diversity in operating scenarios: number and type of events, signal statistics, desired quality, latency, etc.**
- **Cannot achieve $E_{system} = E_{perfect}$ at all points**
 - **Optimize at important scenarios ($E_{system_i} d_i$ is high)**



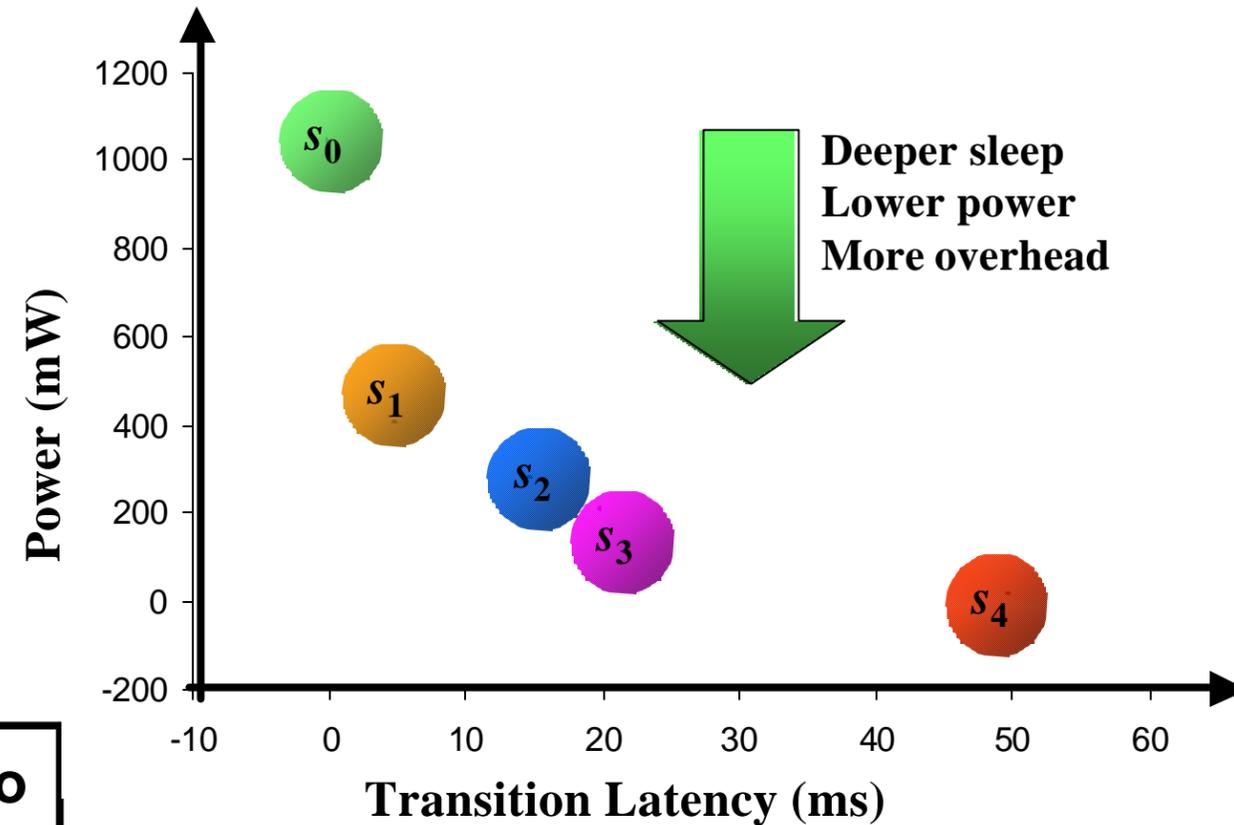
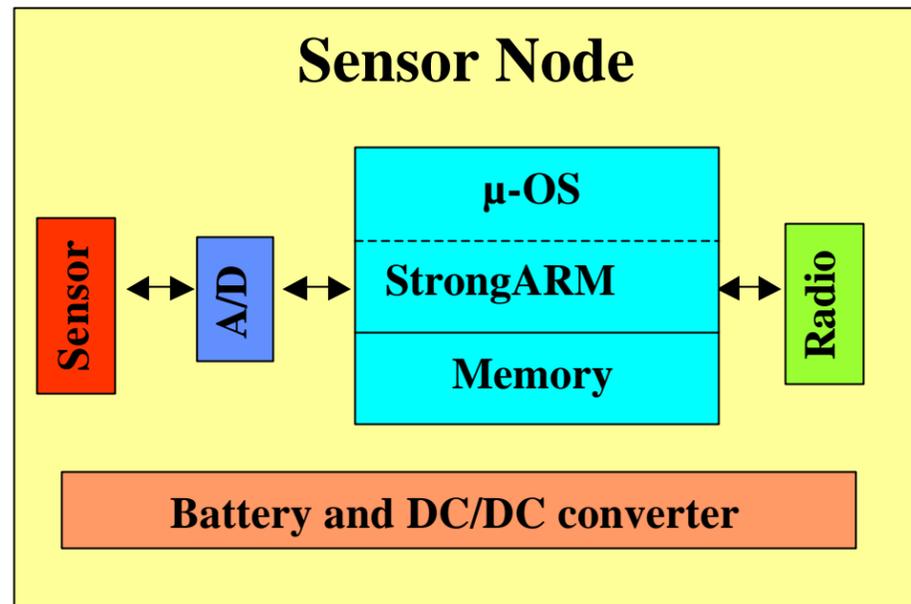
Power Aware Node Architecture



- Graceful energy scalability across a diversity of operating conditions and energy-quality trade-offs



OS Directed Power Management

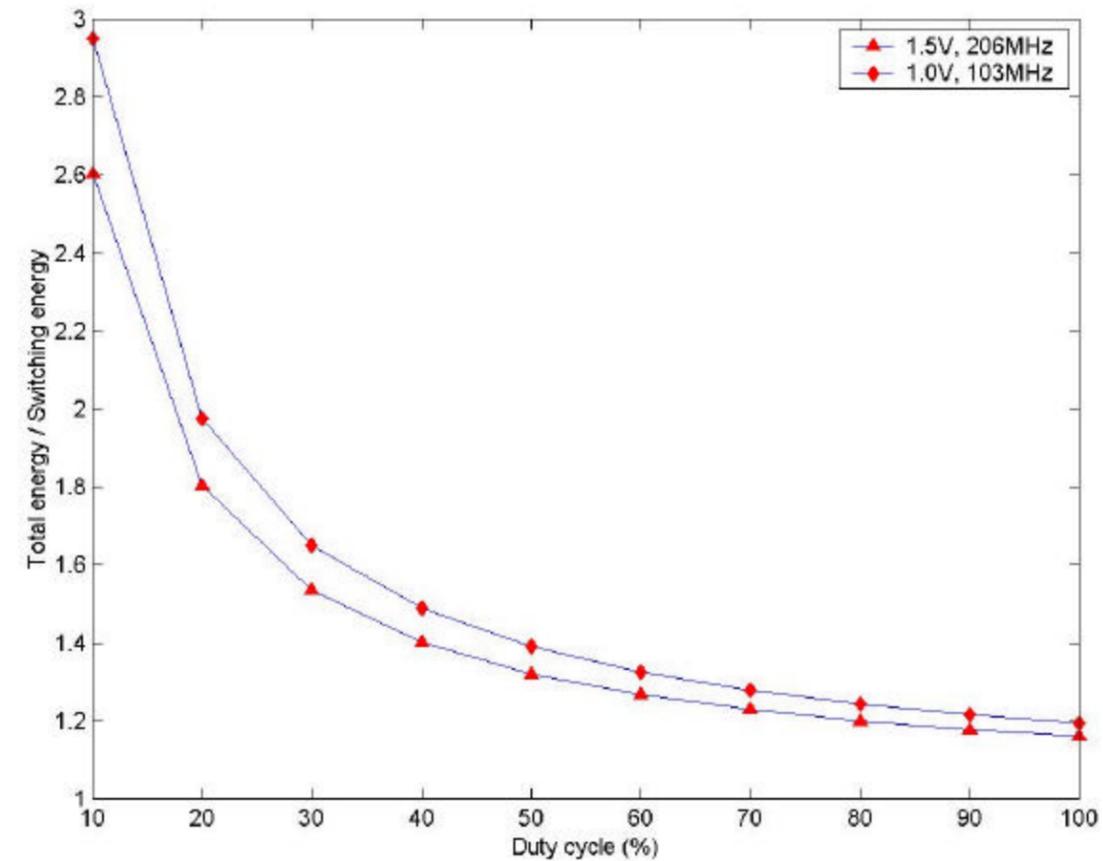
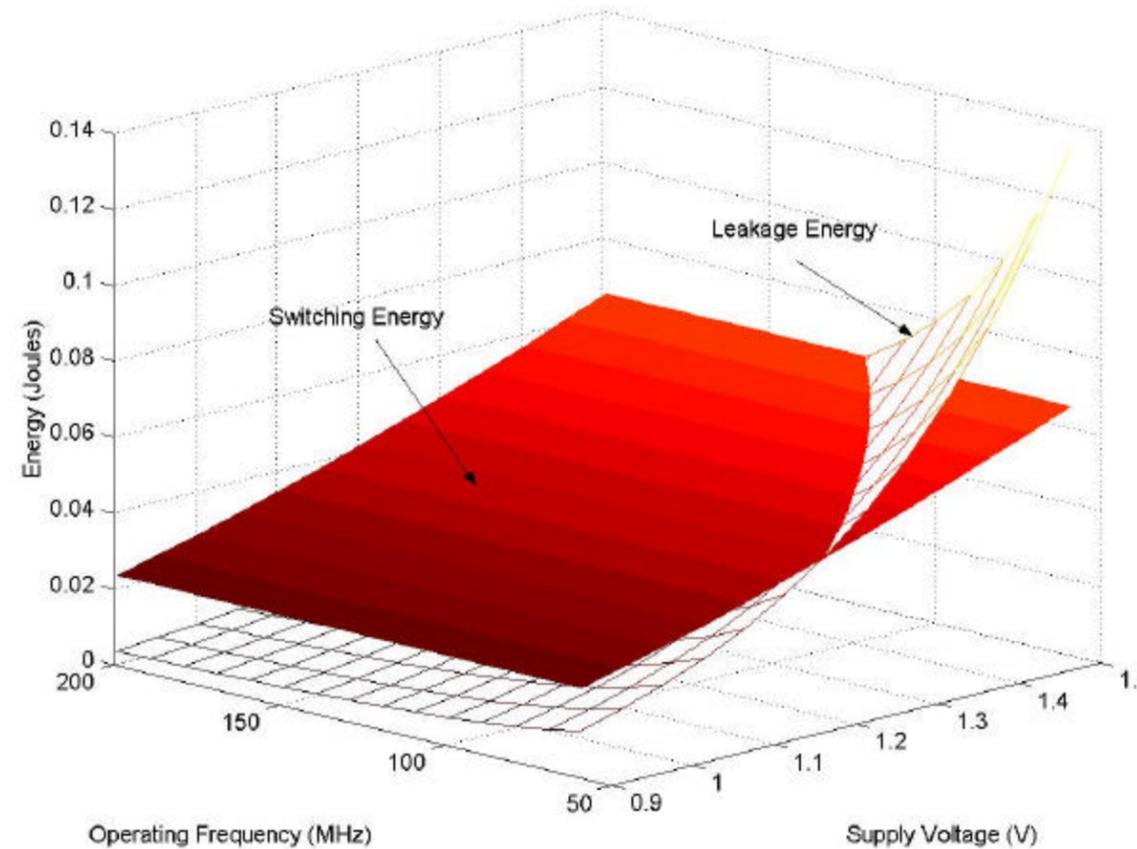


	ARM	Memory	Sensor	Radio
s_0	active	active	on	tx, rx
s_1	idle	sleep	on	rx
s_2	sleep	sleep	on	rx
s_3	sleep	sleep	on	off
s_4	sleep	sleep	off	off

- OS must decide suitable transition policy based on observed history



Idle Mode Leakage Power

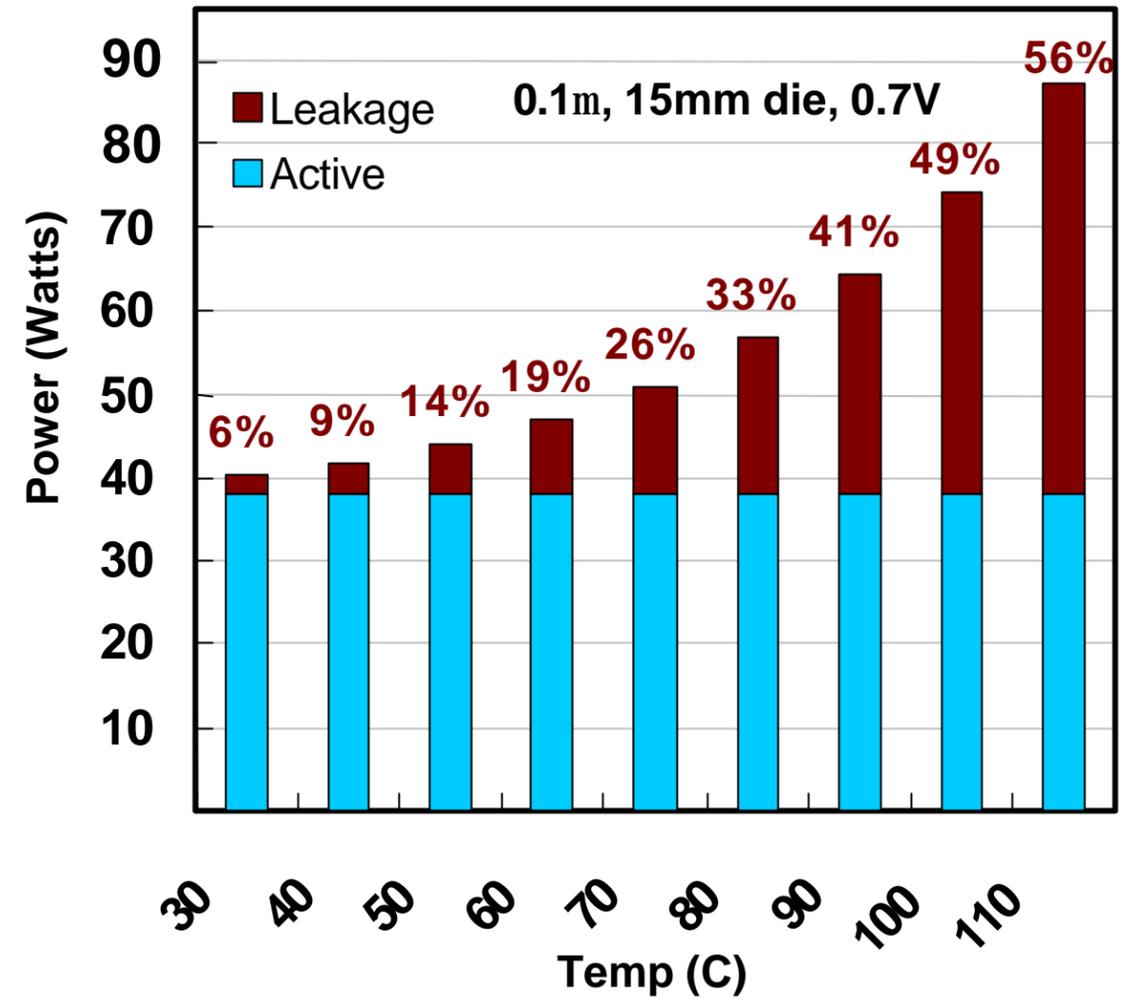
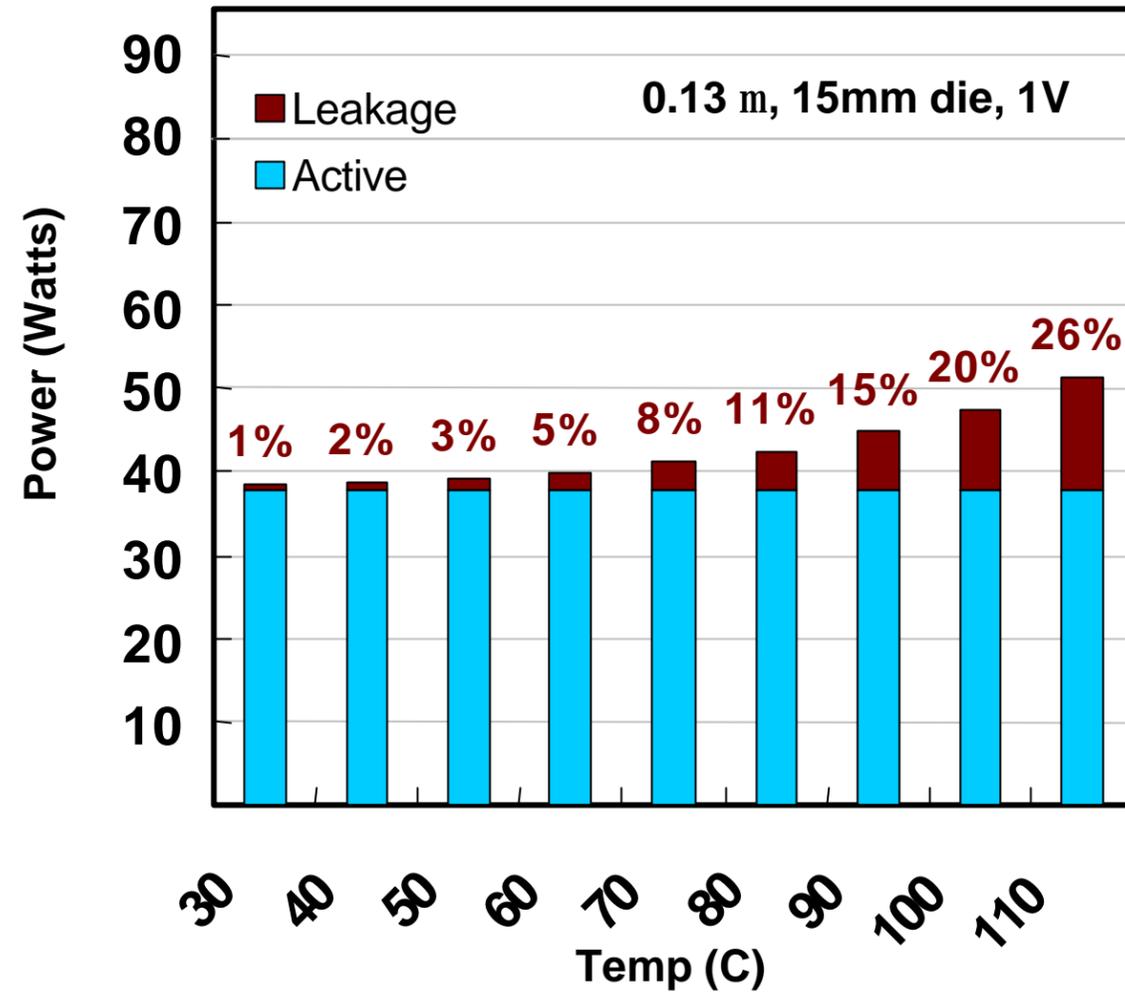


$$I_{leakage} \propto 10^{(-V_T / S)}$$

- Leakage dominates switching energy for **low duty cycles**
- A major concern for event-driven operation (PDAs, sensors, etc.)



Leakage and Switching Power

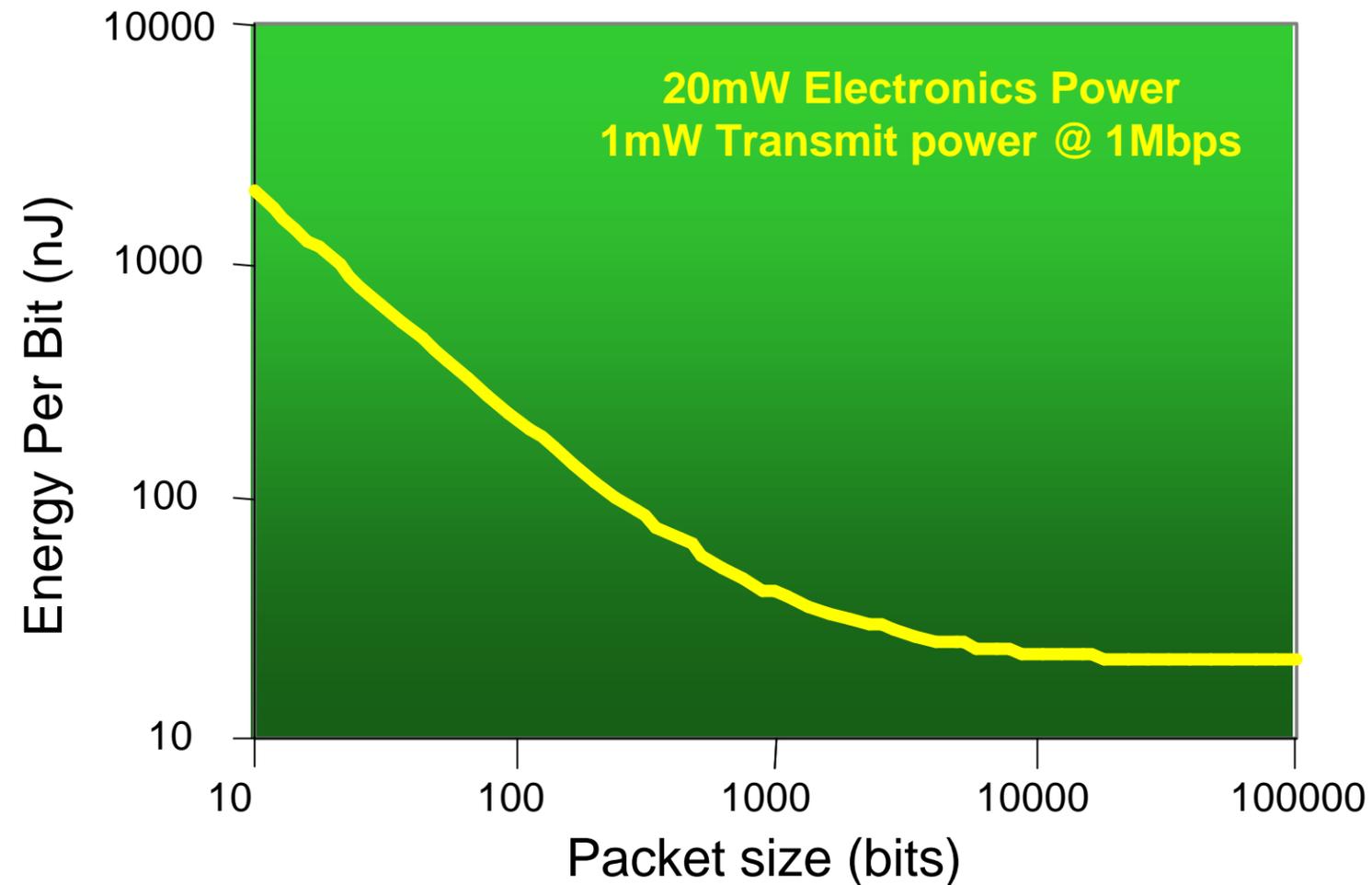


Courtesy of Vivek De (Intel)

Need to Develop Techniques for Leakage Control



Low Duty Cycle Radio

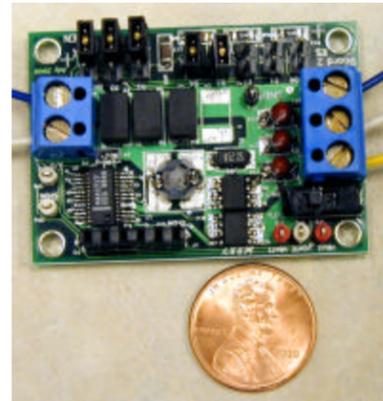


- Start-up time dominates the energy for small packet sizes
- Innovative radio design required...

***Startup Costs are Fundamental –
Latency not just a function of user requirement***

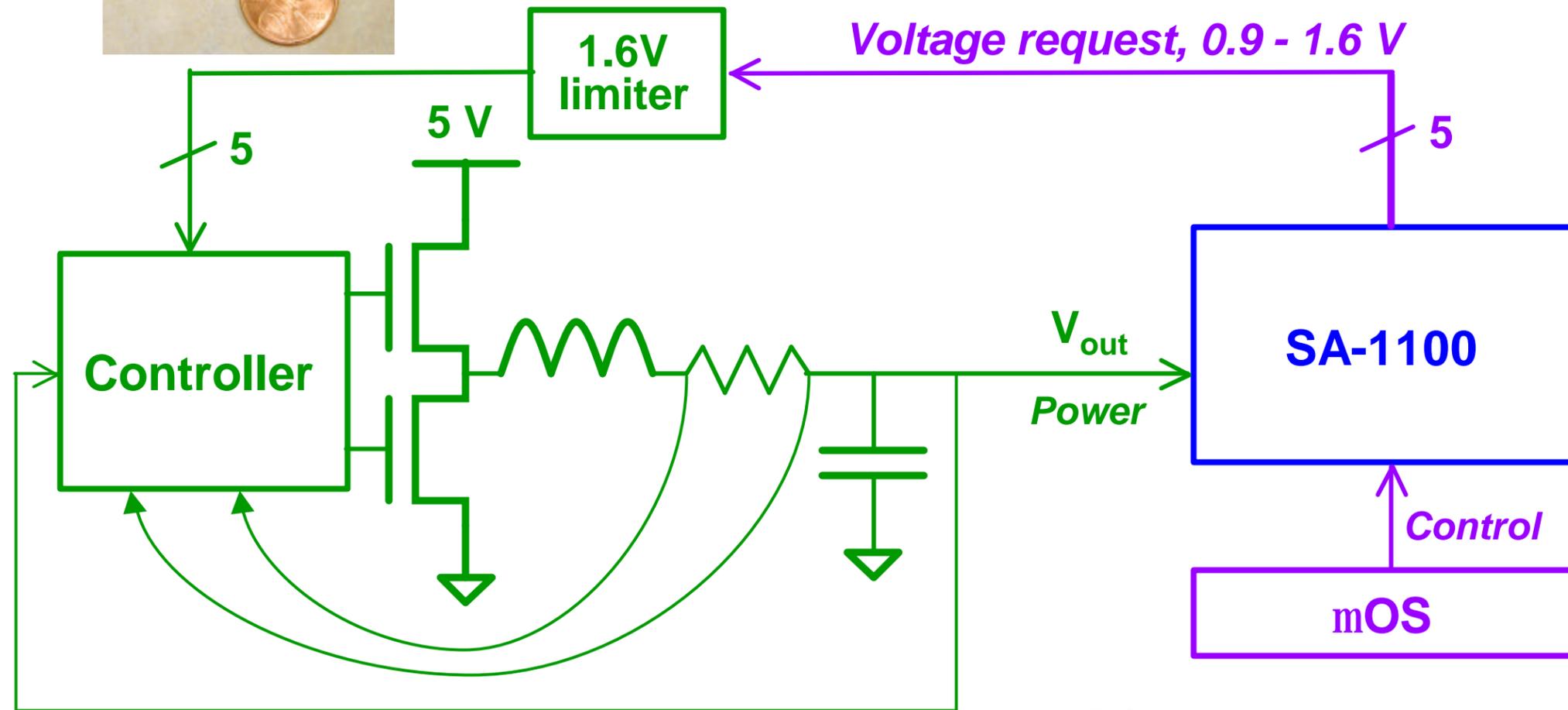


DVS on SA-1100

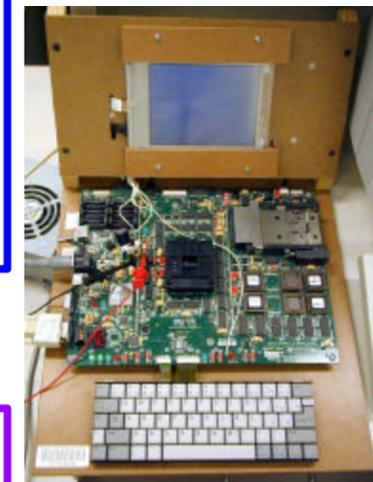


MIT DVS PCB

SA-1100 requests a voltage appropriate for its clock frequency



StrongARM Evaluation Board

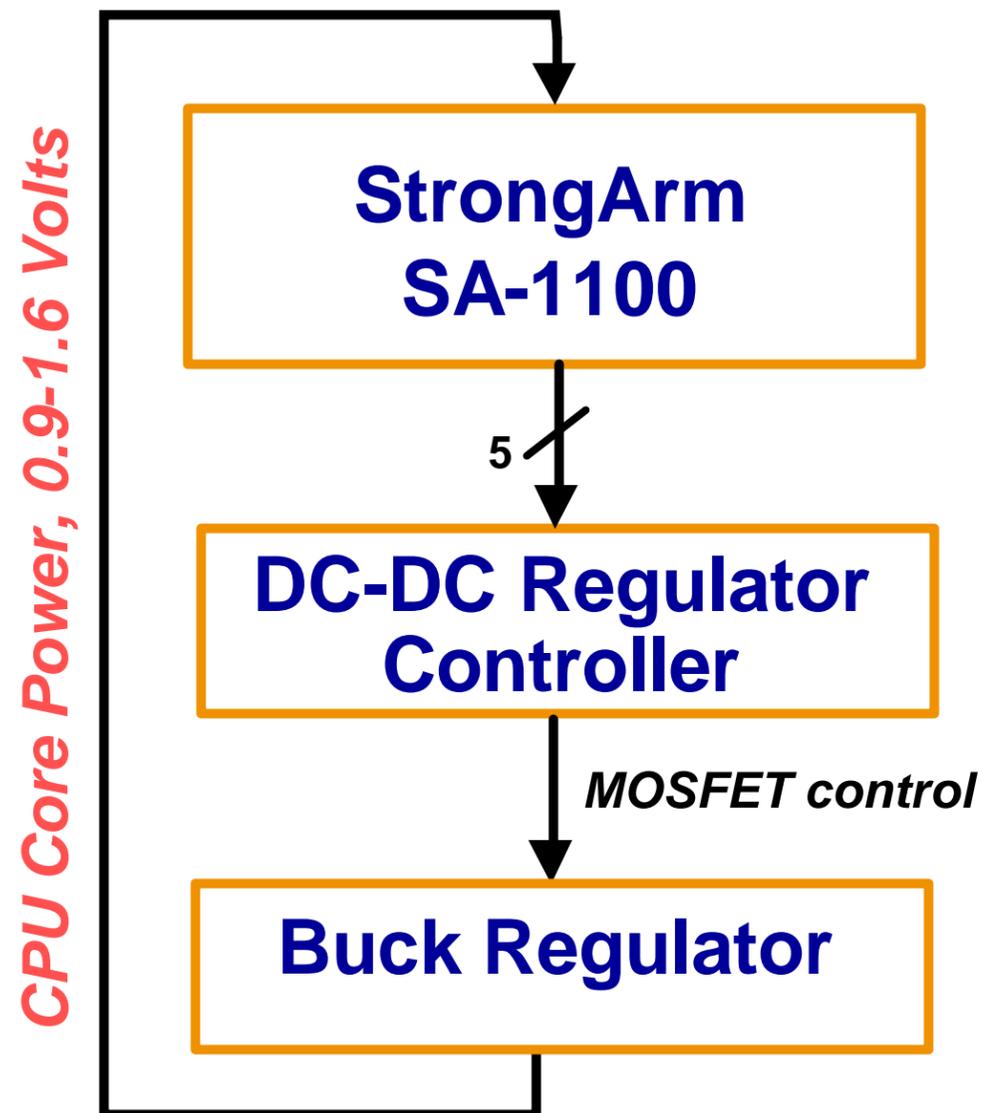


Digitally adjustable DC-DC converter powers SA-1100 core

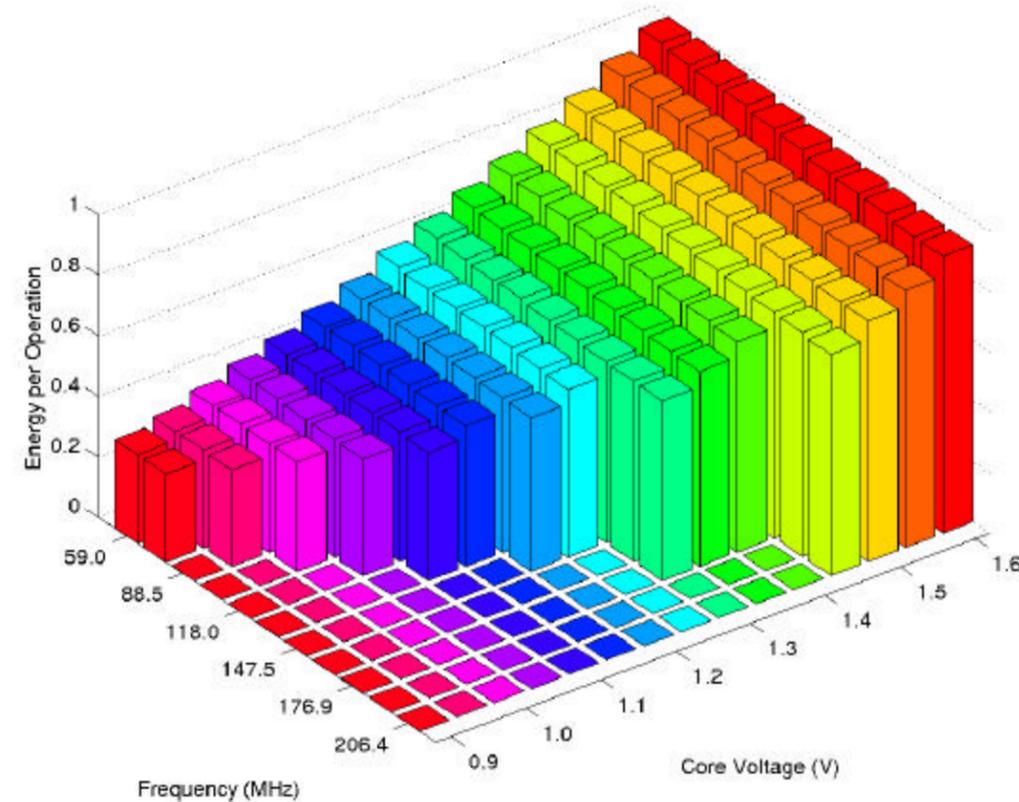
mOS selects appropriate clock frequency based on workload and latency constraints



Software Voltage Scheduling



Data from StrongARM-1100



- Operating system predicts and schedules the voltage
- Adapt power supply to deliver **“just enough performance”**



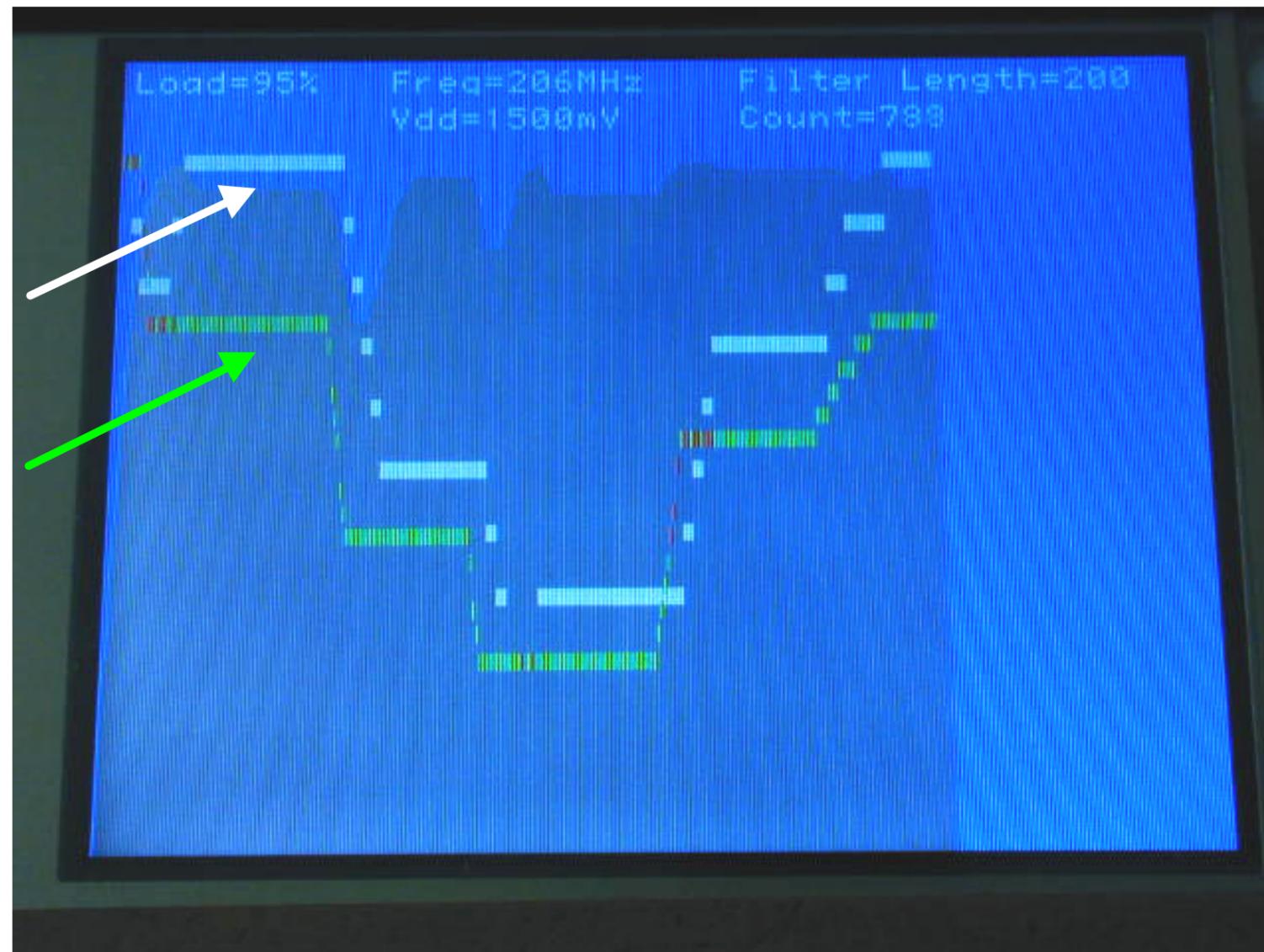
DVS Demonstration



- User adjusts number of filter taps
- Frequency/Voltage adjusted appropriately (via eCOS based mOS)

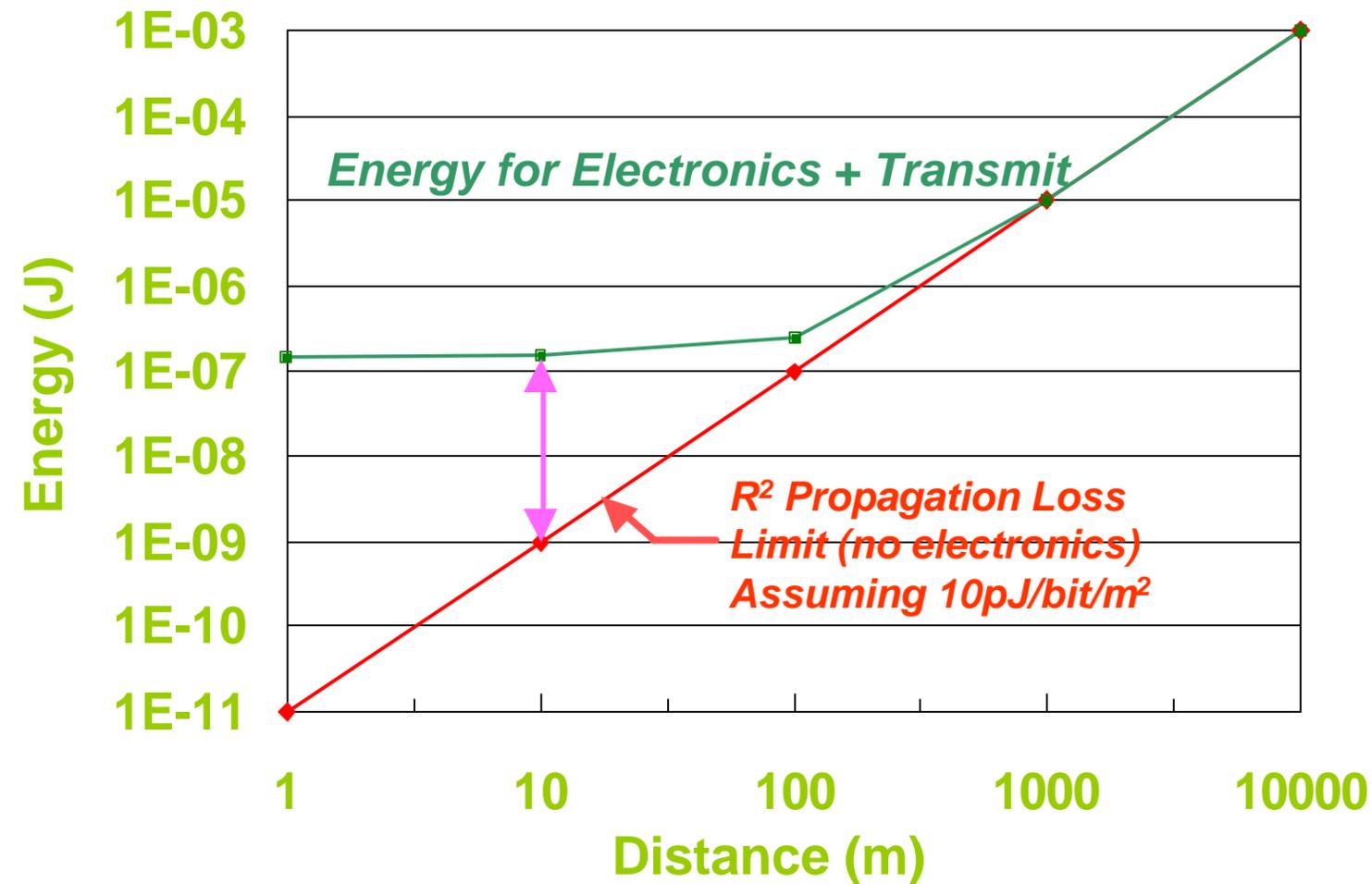
Frequency /
Voltage

Workload
(filter taps)





Computation vs. Communication

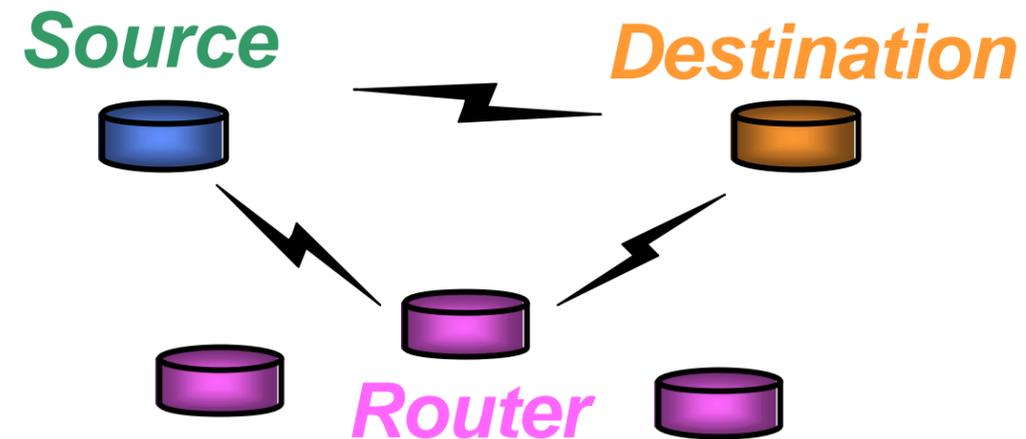


- **Computation: 1nJ/op (m-Processor) and Communication (@10m): 150nJ/bit**
- **@10 m: ~150 instructions/transmitted bit on a low-power processor**
- **@10m: > 1Million instructions/transmitted bit using dedicated hardware**

Compute, Don't Communicate



Protocol Architectures



Multi-hop Routing Example (ignoring electronics)

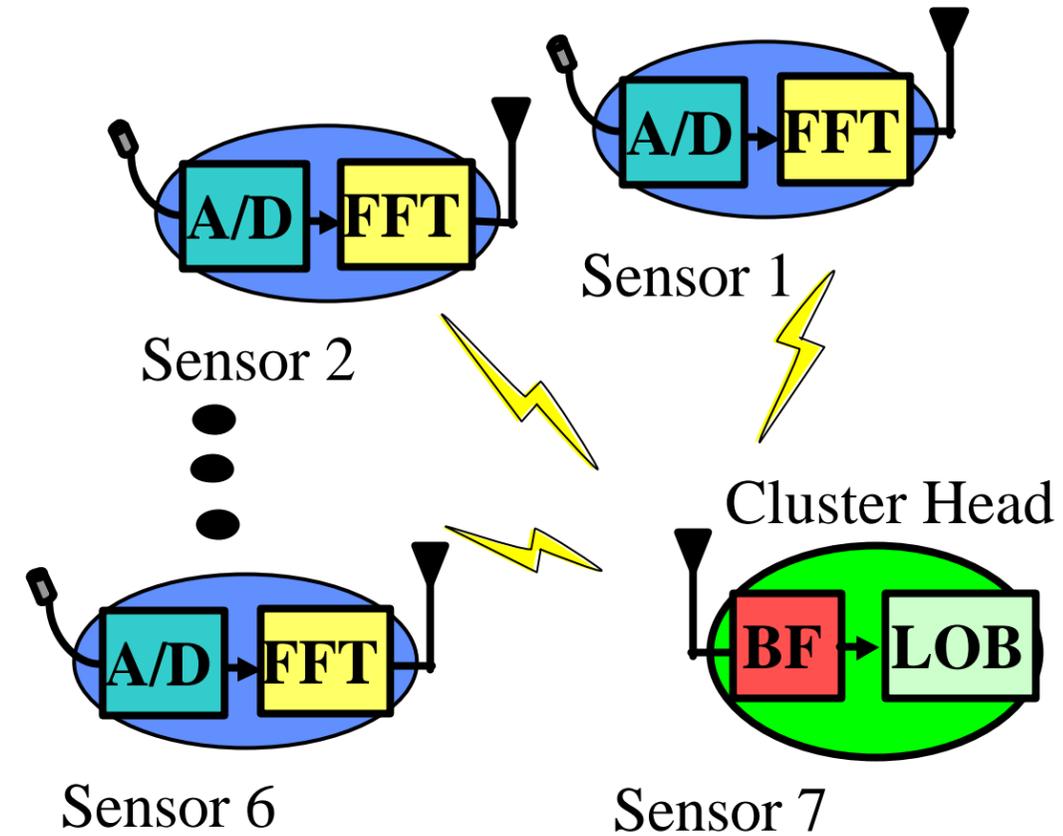
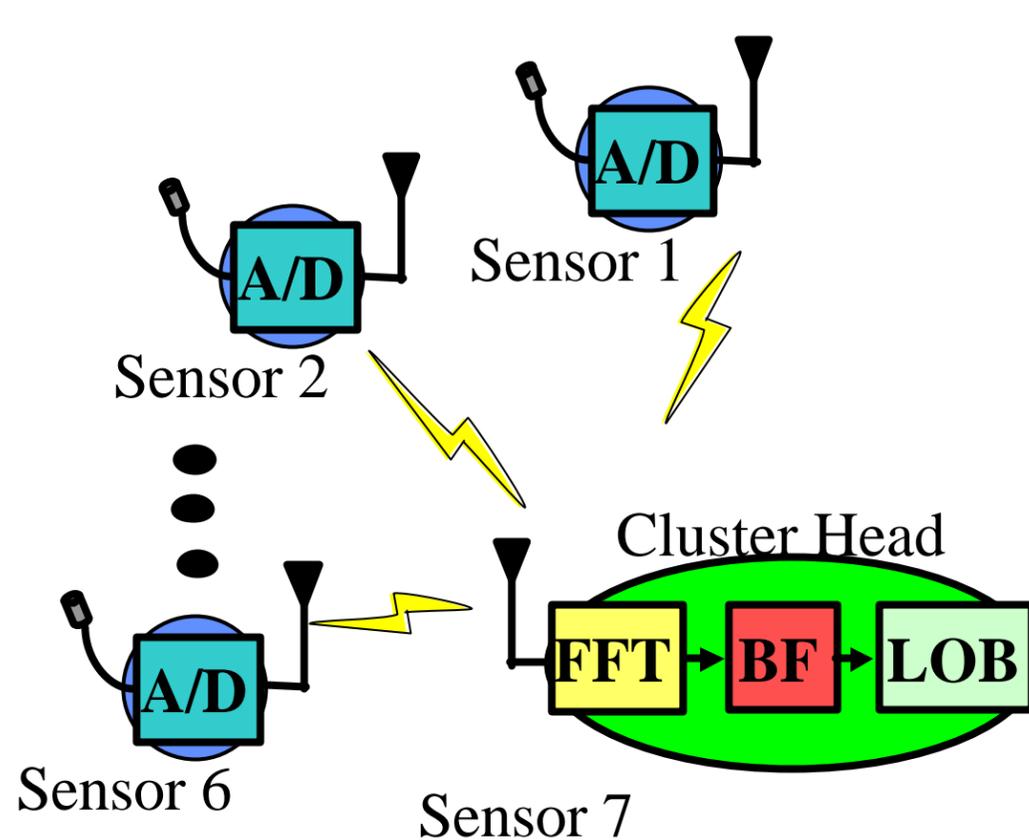
- 1 hop over 100 m: **100nJ/bit**
- 10 hops of 10 m:
 $10 \times 1 \text{ nJ/bit} = \mathbf{10nJ/bit}$

- Particular attention must be placed on multiple access schemes
- Scheduled vs. Reactive routing (synchronous vs. asynchronous)

Similar Trade-off to On-chip Interconnect



Distributed DSP using DVS



- **Approach 1** : All computation is done at C-H

$$E_{\text{comp}}(V_{\text{dd}}=1.5\text{V}) = 7 * E_{\text{fft}} + E_{\text{bf}} + E_{\text{LOB}}$$

$$= 27.27 \text{ mJ}$$

- **Approach 2** : FFT is done at node and transmitted to C-H

Parallelizing the FFT means we can reduce the supply voltage and frequency

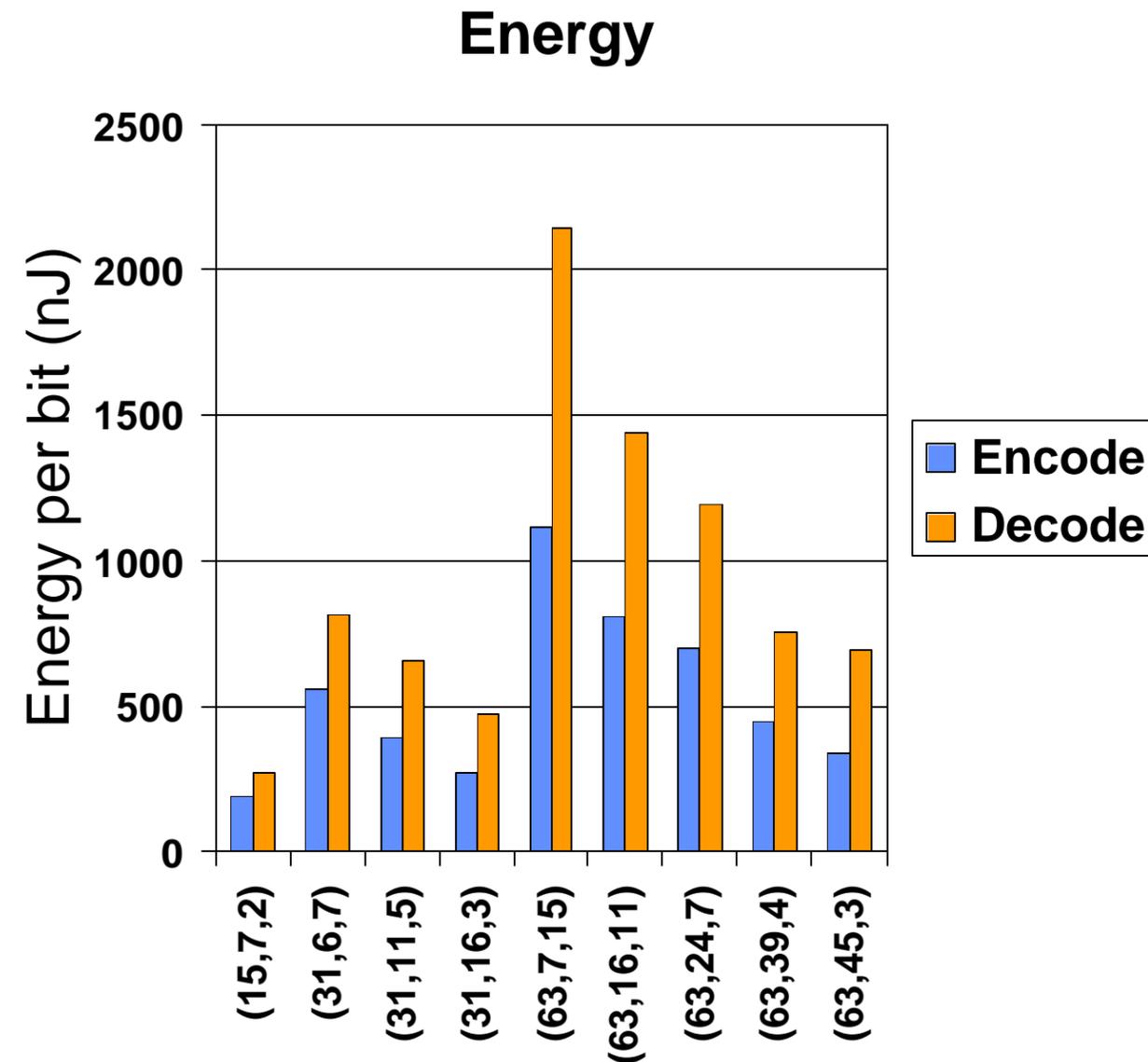
$$E_{\text{comp}}(\text{variable } V_{\text{dd}}) = 15.16 \text{ mJ}$$

FFT is operated at .9 V

BF & LOB is operated at 1.3 V



Energy Efficient Link Layer



- ***Energy scalability through variation of error-correction scheme***
- ***Computation-communication tradeoff between coding and Tx power for BER reduction***



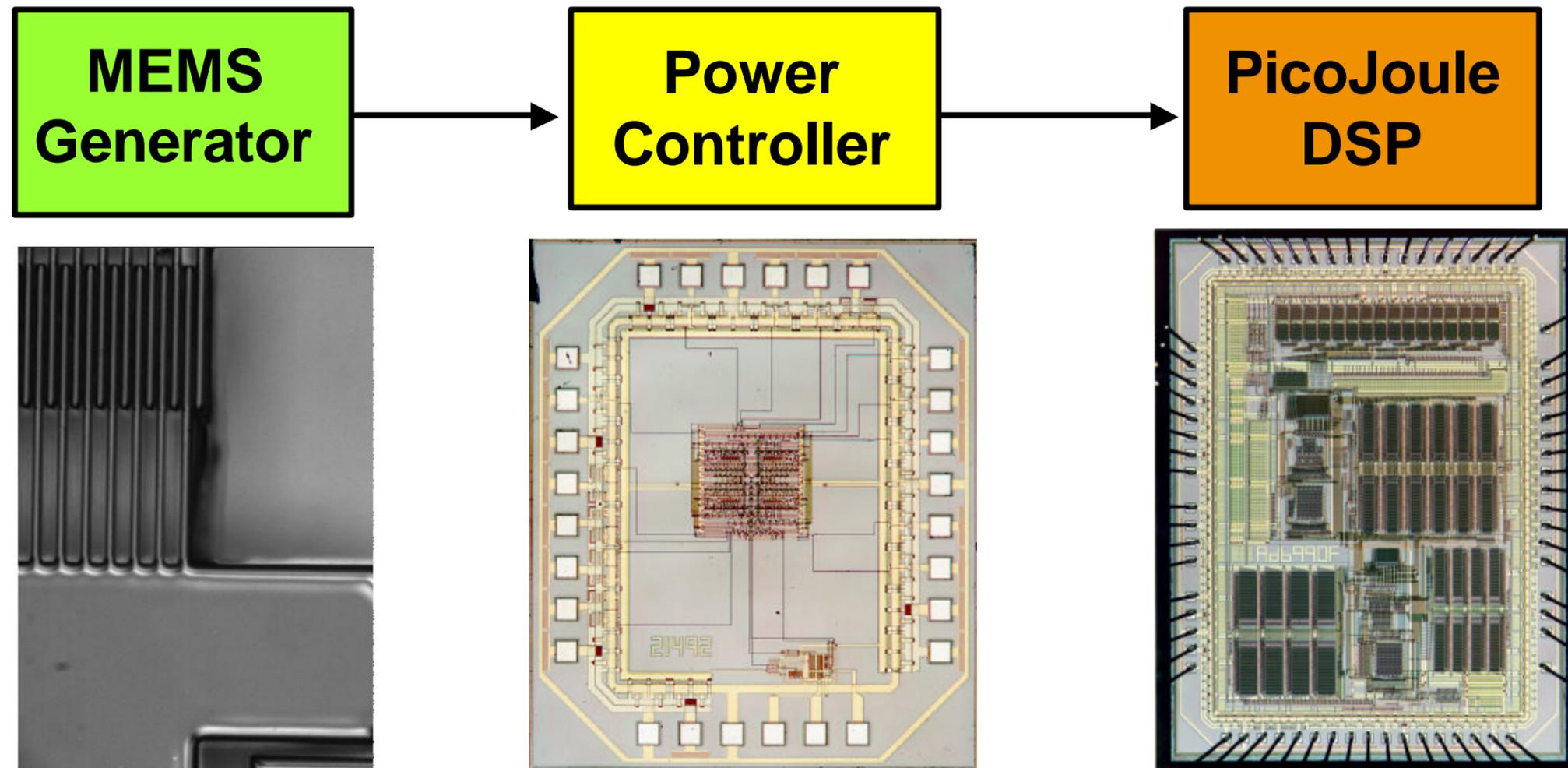
Energy Scavenging



- **Self-powered operation is a real option if the power dissipation can be scaled to 10's - 100's of mW**
 - Mechanical vibration (e.g., machine-mounted sensors)
 - Electromagnetic fields (RF)
 - ⋮
- **A major opportunity exists in developing **energy scavengers** (generator and associated electronics) for extracting useful energy from ambient sources**



Energy Scavenging



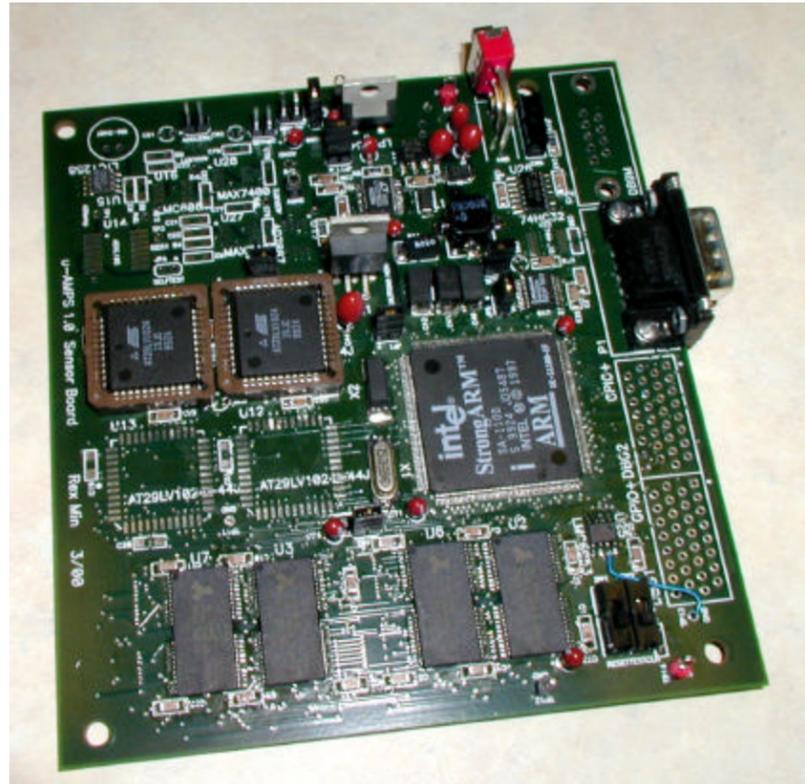
[Amirthrajah00]

- Scavenge energy from mechanical vibrations to power micropower sensor systems
- Power delivered ~ 10mW

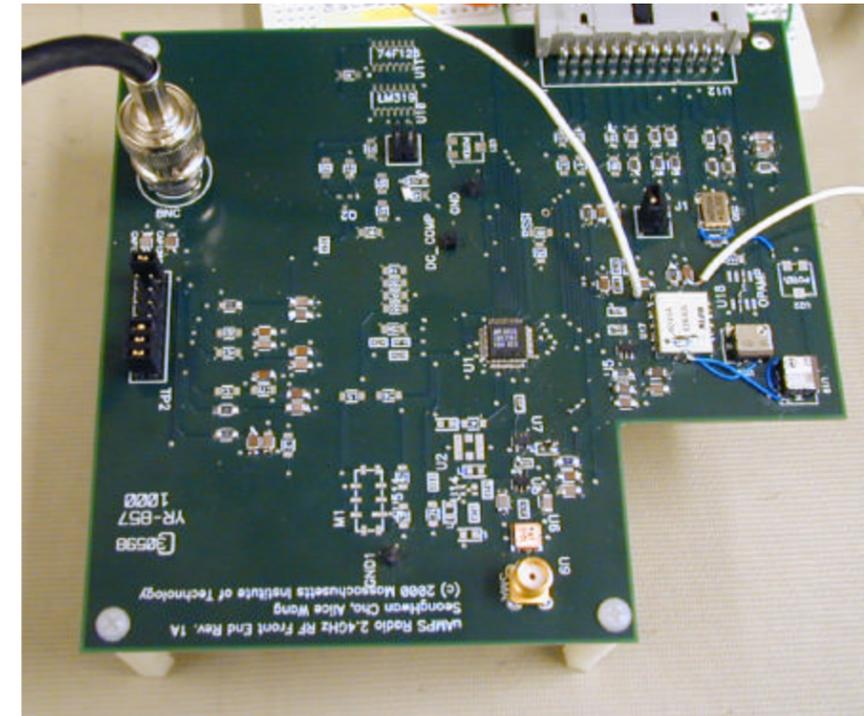
Hardwired Fabrics enable No Power Signal Processing



Node Prototype



sensor/processor board



radio baseband

- Version 1 prototype with COTS components
- Future nodes will feature custom chipsets



Node and Network API



- **Enable and encourage end-user to operate network in a power-aware manner**
 - Sufficient abstraction to hide complexity of distributed wireless network
 - *Get-optimize-set* paradigm to maintain network state

- **Functional interface, object abstractions, and behavioral semantics**
 - Gather and set state of nodes, links, network
 - Facilitate data exchange between node and basestation
 - Realize a user's desired operating point for the network
 - Visualize network state
 - Built-in and customizable energy models for energy, delay, etc.



Summary



- **Just-in-Time** computing through supply optimization minimizes energy dissipation
- Leakage is a first order issue – active leakage management at the architecture, circuit, and device levels are critical
- Focus must shift from computation to communication-centric design
- Protocols must be fabric and domain aware
 - Energy per operation (mW/MIPS) will scale with technology
 - Communication costs (nJ/bit) will not scale at the same rate

Low Energy Sensor Design Requires a System-level Approach – Tight Coupling Between Fabrics, Algorithms and Protocols