IC Compiler II
The Leader in Place and Route - Now With the Power of 10X

Overview
IC Compiler II is a complete place and route system that enables 10X faster throughput for designs across all process nodes, while improving final quality of results (QoR). IC Compiler II is specifically designed to address today’s hypersensitive time to market pressures while delivering best-in-class solutions for flat and hierarchical design planning, early design exploration and prototyping, placement and optimization, clock tree synthesis, routing, manufacturing compliance, and low-power challenges.

- Re-architected for speed, IC Compiler II offers 10X faster design throughput
- IC Compiler II is centered on a built-from-scratch, multi-everything infrastructure, providing near-instantaneous access to data with the ability to handle 500M+ instance designs
- A game-changing, global and analytical approach to optimization pushes the envelope on QoR, setting the new standard for power, area and performance
- New clocking technology in IC Compiler II simplifies and automates clock synthesis, delivering better timing QoR while accelerating clock generation
- Built from scratch and featuring many advanced new capabilities, IC Compiler II’s design planning slashes time-to-useful-floorplan
- IC Compiler II expands the use of the award-winning Zroute digital router technology across all design phases – from feasibility, to placement, to optimization – for even faster design closure
- Preserving user investment, IC Compiler II is designed to leverage all standard inputs and outputs, familiar interfaces and process-specific technology files

IC Compiler II is a complete netlist to GDSII system that includes early design exploration and prototyping, design planning, block implementation, and final chip assembly with native hierarchical support. Figure 1 shows the IC Compiler II physical implementation system with the Synopsys Galaxy Design Platform.

Figure 1: IC Compiler II part of the Galaxy Design Platform
IC Compiler II: The Leader in Place and Route - Now with the Power of 10X

The Power of 10X
IC Compiler II brings new game changing technology and benefits to physical implementation enabling 10X faster throughput that opens opportunities to rethink the entire product development process. Figure 2 shows the design planning and optimization throughput speedup on customer designs.

The Power of 10X faster throughput enables:

- **Accelerated product schedule:** Designers may use the same partition size to achieve faster iterations and faster product delivery. Project schedules are shortened because each block takes significantly less time to create and close.
- **More differentiated products:** With 10X faster throughput more cycles can be spent further refining the design to achieve faster clock frequency, better variation tolerance and less crosstalk – all while staying within current schedules.
- **Improved cost efficiency:** Larger capacity means fewer partitions. With IC Compiler II, valuable engineering productivity per project can be multiplied, allowing for more design starts and the ability to run multiple projects in parallel.

Enabling the Next Decade of Design
The continuously accelerating pace of innovation is dictating a complete rethink of the way place and route systems are built.

Traditionally, physical design flows were organized around simple, discrete steps: placement, clocking, routing and final chip assembly. Each step provided good enough results so that iterative optimization was not a significant impediment to design closure. As requirements evolved, systems became organized around local optimization engines, creating tighter design creation-refinement loops. This approach initially alleviated long iterations in the short term, but it is now running out of steam.

Enabling the next decade of design requires 10X in designer productivity. This means handling 100s of millions of placeable instances, 1000s of hard macros, 100s of clocks, power domains and busses, and 100s of modes and corners.

IC Compiler II represents the next step in place and route system evolution, introducing a novel, global-analytical approach to design optimization, built on a completely new infrastructure.

A New Infrastructure
Architected from the ground up for unsurpassed scalability, IC Compiler II features a brand new design infrastructure complete with compact data model and single timer engine.

Built for both flat and hierarchical design, the infrastructure efficiently coordinates logical, physical and hierarchical design views. It is natively multi-core, fully leveraging available hardware to enable faster runtimes. Library preparation is made trivial with library scaling technology that delivers 10X faster throughput.

A new, incremental timer and extractor provides near-instantaneous access to timing analysis for all system components, while leveraging proven algorithms for excellent out-of-the-box correlation with signoff.

IC Compiler II’s new infrastructure is the pillar that enables 10X faster throughput.

Global Analytical Optimization
IC Compiler II introduces the next step in place and route system evolution, featuring a new optimization framework built on global analytics. This new approach enables faster implementation while pushing the envelope on QoR and accelerating design convergence.

Level-based analytical algorithms continuously optimize during actual physical synthesis using parallel heuristics. Multi-factor costing functions deliver faster results on both broad and targeted goals.

New design closure technology eliminates unnecessary iterations between different metrics throughout the flow. The traditionally separate areas of pre- and post-route optimization are now fully integrated, offering a streamlined flow from floorplan to final SI timing closure. Transparent optimization of interface paths between blocks, or between block and top level, eliminates the need to iterate or re-budget.

Figure 2: IC Compiler II throughput on customer designs
Physical Implementation Metrics

IC Compiler II can be best understood through the examination of the standard measures of physical implementation:

- Quality of Results
- Turn-around Time
- Ease of Use
- Cost of Design

Quality of results

Innovative technology in IC Compiler II delivers improved QoR, measured in terms of the complete cost vector – timing, area, power, signal integrity, routability, and manufacturability.

Data Mismatch Support:

IC Compiler II has a design data mismatch inferencing engine that the user controls according to the quality of the inputs per the design phase. Ports and other constructs are created on the fly during early feasibility to deliver design insight when there are still many unknowns and “dirty” data.

Zroute Global Route Technology:

One of the key enablers to improved optimization is the use of Zroute global route technology during all phases of the design – placement, clock tree synthesis, routing, and optimization – enabling a consistent, monotonic progression towards design closure.

Global First:

Another key optimization improvement is a global first approach coupled with new abstraction methods. The global first optimization approach facilitates monotonic results by precluding localized bottlenecks that are only optimizeable within a larger scope.

Power Optimization:

The efficiency of the IC Compiler II data model enables fast and efficient cell-by-cell power selection as opposed to class-based selection (e.g., LVT vs. SVT). This finer cell selection granularity delivers superior power reduction performance.

Hierarchical TIO:

The IC Compiler II data model is natively hierarchical with the inclusion of the hierarchical context of all physical data. Thus, IC Compiler II’s transparent interface optimization (TIO) is capable of n-levels of reach down or up through the hierarchy to apply optimizations with pin-point accuracy and maximum efficiency.

New CCD:

IC Compiler II’s new concurrent clock and data (CCD) optimization features multiple primary optimization metrics including timing, area, and power - dynamic power for clock cells, leakage for data cells. Concurrent, multi-target clock and data optimization coupled with multi-threading, new abstraction methods and global scope deliver the highest possible QoR.

Turn-around time

IC Compiler II delivers 10X faster throughput, enabling the fastest path to design completion.

Models and Abstracts:

Model and abstract creation methods have been redesigned and refactored based on the new data model. Models and abstractions are created on the fly and the model contents are sensitive to the flow context in which they are created. These smaller, faster, fully hierarchical models greatly accelerate design throughput. An example of acceleration through improved modeling is the timing pane. The timing pane construct in IC Compiler II uses a fast extrapolated look-up model based on initial uptake of the timing data in the cell libraries. Timing panes significantly speed-up timer functions during optimization at all phases of the design.

Multi-Threading:

IC Compiler II is multi-threaded throughout for optimal scalability. Multi-threading efficiency is optimized by innovative optimization technology that successfully partitions large, complex designs across multiple threads.

Scalable MCM:

IC Compiler II is natively multcorner-multimode (MCM) aware and features enhanced handling for numerous, complex modes and corners, enabling unprecedented MCM scalability for “always-on” full MCM analysis.

Native Hierarchical DFA:

The logical, physical, hierarchical IC Compiler II data model enables hierarchical data flow analysis (DFA) natively within the IC Compiler II layout window. Data flow may be visualized up or down through n-levels of hierarchy and directly manipulated from any level to quickly complete early design exploration and prototyping as well as final floorplans. Figure 3 shows an example of the IC Compiler II GUI during native data flow analysis in early design exploration.

Native MIB Handling:

Multi-instantiated block (MIB) handling is native in IC Compiler II. From reshaping, pin and feed-through reflow to timing budgeting, native support makes working with MIBs faster and easier.
Ease of use

IC Compiler II advances ease-of-use with intuitive commands that deliver best out-of-the-box results.

- **New GUI:** IC Compiler II’s new GUI delivers on the design objectives of faster, easier, better. The main design window is larger with toolbars and panels that have been optimized for increased user observability, controllability and productivity. The GUI supports all tool features and delivers unlimited undo/redo and resume from its snapshot capability.

- **Command Search and Task Assistant:** Command search introduces a cockpit to find commands and build design scripts. Command search presents the best matches for commands and displays an organized set of compliant command results with associated command dialogs. Part of the IC Compiler II GUI, the task assistant guides the user through sub-flows either to provide the recommended best practices or to lower the learning curve.

- **Enwrap Technology:** Enwrap technology is a higher order scripting function around existing flow scripts. Enwrap scripting enables the insertion of meta-level snapshots and high granularity reporting during the execution of flow scripts. Exception conditions may be quickly identified in the reports at user specified decision points in the flow and the state snapshot enables resuming work from just before the exception. Enwrap technology eliminates restarting work from the beginning of the design script.

- **Transparent Hierarchical Editing:** Transparent hierarchy editing enables an “edit what you see” model. User controls expand cell and hierarchy visibility to enable cross hierarchy editing and object snapping.

Cost of design

IC Compiler II allows designers to utilize a variety of techniques to meet timing, power, area, routability and yield goals. This reduces the cost of design and increases predictability.

- **Correlation and Checkers:** Timing results correlate closely to PrimeTime, and the new IC Compiler II data model and infrastructure enable higher levels of extraction and timing accuracy with monotonic design convergence throughout the design flow. Checkers exist for design inputs such as libraries, models, timing and UPF constraints. Checking support in the IC Compiler II infrastructure minimizes the need for runtime checking, thus contributing to overall higher throughput.

- **Established Node Support:** IC Compiler II supports established node designs through best-in-class route editing and shape-based routing to facilitate analog mixed signal (AMS) designs. Additionally, IC Compiler II technology is applicable to advanced design work on established process node designs seeking market differentiation.

- **Emerging Node Support:**

  - **Double Patterning:**
    20nm and below designs require at least two masks to correctly expose the design patterns on silicon. IC Compiler II and IC Validator work in tandem to provide the sign-off solution for double or multi-patterning requirements at all emerging node foundries.

  - **Emerging Rule Support:**
    Zroute digital router technology ensures early and full compliance with the latest design rules required for new emerging node technologies. Synopsys collaboration with the foundries ensures that IC Compiler II is the first to deliver support for early prototype design rules and support for the final production design rules.

  - **FinFET Support:**
    IC Compiler II fully supports FinFET use through all physical design stages. A new power optimization metric is available for FinFET design because a FinFET’s dynamic versus leakage power performance may shift dramatically under load. Because of this, care must be taken to balance the overall power goals.

IC Compiler II is the most comprehensive physical implementation solution available. For the complete feature set and input/output specifications, or for detailed information regarding a specific technology need, please contact your local Synopsys account team.

For additional information, visit www.synopsys.com/ICCompilerII