POWER7™ Local Clocking
And
Clocked Storage Elements

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Introduction

• >2M Clocked Storage Elements (CSEs) on the POWER7™ chip

• CSE strategy critical to many aspects of the design
  • Reliability
    • Soft error rate (SER)
    • Stress-induced degradation/failure
  • Test and debug
  • Specific functional features
  • Power, performance, chip area
  • Operating range: voltage, temperature
  • Sensitivity to process variation
Reliability: Soft Error Rate (SER)

- Upset can occur when an ionizing particle deposits charge in the SOI transistor floating body.
- Body charge activates parallel parasitic bipolar mechanism.
- Device turns “on” momentarily, pulling down output.
- Circuit will later recover if input level is undisturbed.
POWER7™ SER Hardening Technique

- Output level is maintained unless both transistors in the stack are hit simultaneously

Bipolar mechanism turns on…

Current flow is Blocked by series device
Hardened Master-slave Latch (MSL)
Upset Cross Sections (SOI designs)

No Stacking  L2 Stacking  L2 DICE

Latch Node and Stored Data

Upset cross section (arb units)

L1_B "0"  L1_B "1"  L2 "0"  L2 "1"
POWER7™ SER Hardening: Net

• >5X improvement by device stacking
  • For most important case, when L2 latch node state matches tgate input node voltage
  • Pulsed-mode operation eliminates L1 as a concern
• ~ 6X improvement from SOI technology (compared to bulk technologies)
• Net: ~ 30X improvement compared to unhardened, bulk designs
Local Clocking

Clock grid input

NCLK

FORCE

ACT

THOLD_B

gate

DELAY_LCLKR

D_MODE_B

MPW1

MPW2

D1CLK

D2CLK

SG_B

LCLK

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Local Clocking

Clock grid input

Race-path stressing for reliability & debug
Local Clocking

Latch writeability stressing for reliability & debug
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Critical path timing improvement & debug
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Clock grid input

Activation of non-pulsed mode for debug work
Local Clocking

Clock grid input

Scan control: selects d1clk active vs d2clk active
Local Clocking

Clock grid input

ACT: local clock gate
FORCE: clock gate override
THOLD_B: global clock control
Example: Latch Writeability Stress

- Vmin shift from effect of narrower lclk pulse (MPW2)
Example: Local Frequency Division

- Allows local clock to fire only on alternate cycles
- Alignment control, + override (sg) for test purposes
CSE Power/Performance Optimization

- Pulsed-mode power
- Additional power in non-pulsed mode

Swap to lower VT (decrease in delay)

Swap to higher VT (increase in delay)

Similar delays; power reduced by layout optimization

A

B

C

D

E
POWER7™ CSE Design: Conclusion

• SER-hardened elements used for enhanced reliability
  • SOI-specific hardening technique
  • ~ 30X improvement compared to bulk-silicon, unhardened designs
  • Very little power, performance, area overhead
• Advanced features for rigorous stress testing at time 0
  • Guardbands against write margin degradation
  • Guardbands against effects of pulse width widening
• Local clock controls for enhanced design debug
• CSE design: Multi-variable optimization for power/performance
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