A Low Loss Wide Swing Cascode Current Mirror in 0.18-µm CMOS Technology

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ABSTRACT

Current mirror is an essential component in analog integrated circuit design for biasing and constant current generation. In this paper a design of a wide swing cascode current mirror circuit (WSCCM) is proposed by using Mentor Graphics Design Architect and IC Station which is implemented by using CEDEC 0.18-µm CMOS process. The widths of the transistors are varied to obtain best performance current mirror. For a width of 6 µm, 98.57 µA output saturated current is obtained. Besides, at this width the current reaches the saturation very quickly at a voltage of 0.44V. The results show that the circuit is able to obtain a minimum bias voltage, lower power dissipation and quicker saturation region than the previous works.

Key words: CMOS, WSCCM, Current Mirror.

Introduction

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS) (Hitesh and Goel, 2012; Reaz et al., 2006; Singh et al., 2009; Marufuzzaman et al., 2010; Akter et al., 2008; Reaz et al., 2007). It is a very useful building block in analog integrated circuit design and widely used in the biasing circuits in many analogue and digital systems as well as in constant current generation circuits (Reaz et al., 2005; Akter et al., 2008, Mohd-Yasin et al., 2004; Reaz et al., 2003). In many analog circuit applications, the performance of the current mirror focuses on the high accuracy, high output impedance, wide output voltage range, wide current mirroring range, and fast current switching time (Yang et al., 2008). Although there are several current mirror architectures demonstrated in different literatures (Sampietro et al., 2000; Sarao et al., 2002; Tseng et al., 2007; Kim et al., 2008; Azhari et al., 2011; Petrellis et al., 2012; Gupta and Sharma, 2012) but figure 1 shows the typical and most basic current mirror configuration using MOS devices.

Fig. 1: Basic MOSFET current mirror.

The studies and analyses on design and performance of Current mirror circuits are going on for the last couples of years (Tseng et al., 2007). In this paper an improved design of the wide swing cascode current mirror in purpose to reduce power dissipation and to increase performance through MOS devices width adjustment.

Architecture Of Current Mirror:

A high-swing current mirror includes a cascode current source and a current source bias circuit (Shukla et al., 2011). The current source includes first and second bias terminals and an output terminal whereas the bias circuit includes transistors Q1, Q2, Q3 and Q4. Transistor Q1 has a gate, source, and drain, with the gate coupled to the drain. Transistor Q2 has a gate, source, and drain, with the gate and source of transistor Q2 coupled to the...
gate and source, respectively, of transistor $Q_1$. Transistor $Q_1$ has a gate and drain coupled to one another and to the second bias terminal and a source coupled to the drain of transistor $Q_3$. Transistor $Q_3$ has a gate and drain coupled together and to the first bias terminal and a source coupled to the sources of transistors $Q_3$ and $Q_4$. The schematic diagram of proposed wide swing cascade current mirror is shown in figure 2.

![Fig. 2: Schematic diagram of typical wide swing cascade current mirror.](image)

The wide-swing current mirror represents an excellent accuracy with high output swing. As the structure with high output impedance is more convenient so in the purposed design output impedance is kept high (Blazes, 1991). The wide-swing cascode current mirror is a variant on the cascode on a lower bias voltage. Its small-signal behaviour is identical to the regular cascode, but its biasing is quite different. The extra MOSFET $Q_5$ is simply to ensure the rest stay in saturation. The biasing voltage is usually minimum as it is the total drain to source voltage of $Q_2$ and $Q_4$ (Nojdelov and Nihtianov, 2009). The output voltage is given by the total of bias voltage and drain to source voltage of $Q_2$ and $Q_4$ respectively. So the special arrangement and sizing of the MOSFETs ensures that $Q_3$ is always just on the edge of saturation and never switches off. In other words, we have to ensure that $V_{GS1} < 2V_t$. So $Q_1$ is not on automatically – we must ensure it is switched on by keeping its $V_{GS}$ below $2V_t$. This is not difficult to do, and usually follows automatically from the arrangement and sizes of the devices.

The drawback of standard cascode current mirror is its higher input and output compliance voltage (Fiocchi and Gatti, 1999). This high swing cascode topology shown in Figure 3 is better alternate as it provides the same output resistance as of standard cascode but it provides low input and output compliance voltage in comparison to standard cascode structure. An additional transistor $M_5$ is added in series with $M_1$ so as to make the drain voltages of $M_1$ and $M_2$ to be identical, thus eliminating any error because of channel length modulation.

![Fig. 3: High swing cascode current mirror (initial design without M5).](image)
The schematic diagram of the circuit is shown in Figure 4. After the schematic was checked and saved, then the symbol was generated for our test bench part for testing purposes. The layout for the circuit is then created in IC Layout of Mentor Graphics. Figure 5 shows the IC layout design for this circuit.

A single resistor placed between $V_{DD}$ and drain of $M_4$-NMOS transistor as shown in the schematic plays an important role in decrement of saturation time of the proposed WSCCM. The resistor, $R_1$ actually helped the mirror side of NMOS to reach the threshold and became saturated within a shorter period. Continuing to use the cascode method to increase the DC gain of the circuit quickly destroys the output swing of the circuit as each transistor needs to have a threshold voltage across it. To overcome this, increase in the output resistance (decreasing lambda) of the circuit is needed (Kim et al., 2008). This can be done by using an extra transistor as an amplifying feedback loop to the cascading transistor as was done by $M_5$.

**Results And Discussions**

Simulation has been done with Mentor Graphics DA-IC for output current of the circuit as a function of different width sizes of NMOS transistors and the result is plotted in figure 8 below.
Fig. 6: The output current obtained from different transistor width.

From the figure it is found that the greater the width of NMOS the better the performance in the mirror side. The red colour line in the graph shows the most stable output compared to others. The 6.0 µm width of MOSFET also enables a slight quicker saturation region than other sizes. The result is also represented in tabular form in table 1 below.

<table>
<thead>
<tr>
<th>Transistor width</th>
<th>Output saturated current</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µm</td>
<td>75.71 µA</td>
</tr>
<tr>
<td>3.0 µm</td>
<td>95.89 µA</td>
</tr>
<tr>
<td>6.0 µm</td>
<td>98.57 µA</td>
</tr>
</tbody>
</table>

However, the M₅-NMOS transistor should be exactly or closely to W/L ratio of 1 because this transistor supplies the gate bias of M₃ and M₄ transistors. However as the sizing rule limitation in IC layout design, we considered the minimum size of MOSFET devices which is 0.9 µm width for M₅ (Pennisi, 2005). For the other NMOS transistors M₁, M₂, M₃ and M₄, the width is 6.0 µm.

<table>
<thead>
<tr>
<th>Transistors Width</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁, M₂, M₃, M₄</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>M₅</td>
<td>0.18 µm</td>
</tr>
</tbody>
</table>

There are several characteristics related to the current mirror design. This work of WSCCM consumed a typical small bias voltage compared to other current mirror circuits (Singh et al, 2009; Blazes, 1991). A performance comparison of current mirror circuits in different works is shown in Table 3.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>This work</th>
<th>(Fiocchi and Gatti, 1999)</th>
<th>(Singh et al, 2009)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage supply (Vs)</td>
<td>1V</td>
<td>3V</td>
<td>2V</td>
</tr>
<tr>
<td>Power dissipation (P)</td>
<td>0.249mW</td>
<td>0.691mW</td>
<td>7.4mW</td>
</tr>
<tr>
<td>Resistor (ohm)</td>
<td>1kΩ</td>
<td>1kΩ</td>
<td>N/A</td>
</tr>
<tr>
<td>Minimum bias voltage (Vbias)</td>
<td>626mV</td>
<td>N/A</td>
<td>2kΩ (feedback)</td>
</tr>
</tbody>
</table>
Usually greater transistor width result in consumption of more power (Fiocchi and Gatti, 1999). Therefore, power dissipated by the WSCCM design in this design is kept small by using least amount of transistors. It also provides stable and continuous current supply. Figure 9 and figure 10 represents the minimum bias voltage consumption and output current of the circuit, respectively.

**Conclusion:**

This article proposes a best performance design of a wide swing cascode current mirror architecture. By attaching the resistor direct into the circuit, the output current will tend to saturate very quickly compared to other concurrent designs. The design also required a minimum bias voltage as less as 0.4V to operate and thus makes it compatible for application that require higher output impedance and where the voltage supply is critical.
References


