Research Article | Vol. 26, No. 7 | 2 Apr 2018 | OPTICS EXPRESS 8821
Optics EXPRESS

Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser

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Abstract: An electrically pumped DFB laser integrated on and coupled to a silicon waveguide circuit is demonstrated by transfer printing a 40 × 970 μm^2 III-V coupon, defined on a III-V epitaxial wafer. A second-order grating defined in the silicon device layer with a period of 477 nm and a duty cycle of 75% was used for realizing single mode emission, while an adiabatic taper structure is used for coupling to the silicon waveguide layer. 18 mA threshold current and a maximum single-sided waveguide-coupled output power above 2 mW is obtained at 20°C. Single mode operation around 1550 nm with > 40 dB side mode suppression ratio (SMSR) is realized. This new integration approach allows for the very efficient use of the III-V material and the massively parallel integration of these coupons on a silicon photonic integrated circuit wafer. It also allows for the intimate integration of III-V opto-electronic components based on different epitaxial layer structures.

OCIS codes: (250.5960) Semiconductor lasers; (250.5300) Photonic integrated circuits.

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#315855 https://doi.org/10.1364/OE.26.008821
Journal © 2018 Received 9 Jan 2018; revised 21 Feb 2018; accepted 7 Mar 2018; published 27 Mar 2018

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1. Introduction

Silicon-on-insulator (SOI) is amongst the mainstream photonic integration platforms regarded as the most promising candidate for ultra-compact photonic integrated circuits, due to the high refractive index contrast between the silicon waveguide core and the SiO_2 cladding. More importantly, the compatibility with the well-established CMOS fabrication technology, both in terms of the used materials and processing techniques, enables a low-cost and high-volume production of photonic integrated circuits (PICs) with high yield [1–4]. Driven by the telecom and datacom industry significant progress has been made in the field of silicon photonics in the past decade. A variety of high-performance passive building blocks and high-bandwidth Si and GeSi active devices (modulators and photodetectors) have been developed making use of a strong light-matter interaction, resulting from the high confinement of the optical field in the waveguide, thereby paving the way for scalable manufacturing of complex high-speed PICs [5]. Moreover, with a wide transparency window ranging from 1.2 to 4 μm, silicon photonics is emerging as a potential platform to realize miniaturized sensors [6–9]. Nevertheless, the absence of an integrated light source remains an obstacle for the proliferation of silicon photonics, due to the costly and time-consuming assembly processes that are used today to integrate III-V opto-electronic components on the platform. To overcome this issue, tremendous efforts have been devoted in the past decade to heterogeneously integrate III-V light sources on a Si PIC. Explored methods include the heterogeneous integration through bonding techniques [10–12], the direct epitaxy of III-V materials on Si [13-14] and the development of a Ge laser [15]. Although a variety of state-of-the-art III-V-on-Si lasers have been demonstrated based on die-to-wafer bonding techniques, the efficiency of the material use is poor, which is related to the millimeter-scale minimum die size that can be handled. This also prohibits the dense co-integration of different III-V epitaxial layer structures and at the same time the heterogeneous integration of

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III-V devices on a complex silicon photonic integrated circuit with a thick back-end stack. While epitaxial growth approaches do not suffer from these drawbacks, they are still in an early stage of research. Micro-transfer-printing on the other hand has in recent years gained interest in the field of PICs as an effective way to integrate III-V opto-electronic components onto a silicon photonic integrated circuit [16–19]. This novel technique allows the manipulation of micron-sized thin films such as III-V material coupons and devices, realized on their III-V native substrate in a dense array, such that they can be printed in a massively parallel way to another substrate (in our case a silicon photonics wafer), leading to a significant improvement in material use compared to wafer bonding methods and a significant increase in throughput compared to flip-chip-like assembly methods. The micro-transfer-printing concept is illustrated in Fig. 1. The device epitaxial layer structure is grown on a III-V source wafer, incorporating a sacrificial release layer (InGaAs or InAlAs in the case of InP-based epitaxy [20]). Devices or material coupons are patterned on the III-V source wafer as indicated in Fig. 1(b) and are covered with a photoresist encapsulation, with local openings to access the release layer. The release layer can then be selectively etched (using $FeCl_3$:H_2O in the case of InP-based epitaxy [18]), leaving the devices or material coupons attached to the substrate by the polymer tether structures. Using a polydimethylsiloxane (PDMS) stamp these coupons can then be individually or massively parallel picked from the substrate, by breaking the tether structures, and printed on a silicon photonic target wafer with high alignment accuracy (+/– 1.5 μm 3σ [21]).

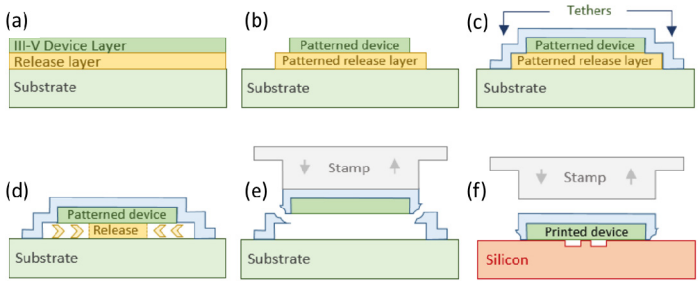

Fig. 1. Micro-transfer-printing concept, illustrating the release, picking and printing of a single coupon/device. The concept can readily be extended to massively parallel printing, by using a properly structured stamp.

Figure. 2 illustrates the cross-section of a III-V-on-silicon PIC that could be realized through transfer printing. Due to the fact that micron-scale III-V devices or material coupons can be transferred, a dense integration of III-V opto-electronic components based on different epitaxial layer stacks can be realized. Most waveguide-coupled III-V-on-silicon devices rely on adiabatic taper structures to couple light to and from the III-V device, which requires more stringent alignment than what can currently be obtained using transfer printing. Therefore, an attractive approach is to print III-V material coupons and process these coupons into opto-electronic devices after transfer printing, potentially on a wafer level, making use of high-alignment-accuracy lithography.

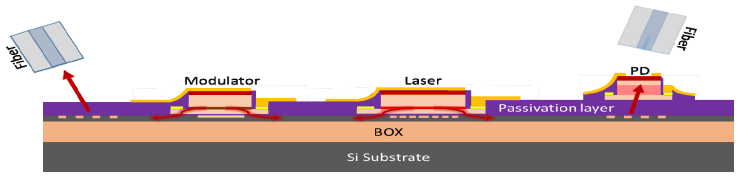

Fig. 2. Schematic of an integrated photonic circuit built on a passive SOI waveguide circuit based on transfer printing combining different III-V epitaxial layer stacks densely integrated together.

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In this work, we demonstrate the first III-V-on-Si distributed feedback (DFB) laser fabricated through transfer printing. The laser is integrated on and coupled to a passive SOI wafer that has a 400 nm thick silicon device layer, is etched 180 nm and is planarized using SiO_2 on top of the silicon device layer. The demonstrated DFB laser shows single mode operation in the C-band, 18 mA threshold current and 2.2 mW single-sided waveguide-coupled output power at 70 mA bias current at 20°C. This work demonstrates the potential that transfer printing has for the integration of III-V opto-electronic components on a silicon photonic integrated circuit. It paves the way to build complex III-V-on-silicon PICs on a low-cost passive silicon photonics platform. The paper is structured as follows: in Section 2 the III-V coupon preparation and release process is discussed. In Section 3 the III-V transfer-printing process and post-processing of the III-V device on the silicon photonic target substrate is discussed. In Section 4 the device characteristics are presented.

Table 1. III-V laser epitaxial layer stack

Layer	Layer type	Material	Thickness (nm)	Doping level (cm^{-3})	Dopant
26	Cap layer	InP	100	nid	
25	Contact P	InGaAs	100	$>1 \times 10^{19}$	Zn/C
24	Contact P	InGaAs	100	$\sim 1 \times 10^{19}$	Zn
23	Cladding P	InP	1000	$\sim 1 \times 10^{18}$	Zn
22	Cladding P	InP	500	$\sim 5 \times 10^{17}$	Zn
21	Transition	$(Al_{0.9}Ga_{0.1})_{.47}In_{.53}As$	40		
20	Confinement	$(Al_{0.7}Ga_{0.3})_{.47}In_{.53}As$	75		
9 × 6	Barrier	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10		
8 × 6	Quantum well	$(Al_{.25}Ga_{.75})_{.3}In_{0.7}As$	6		
7	Barrier	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10		
6	Confinement	$(Al_{0.7}Ga_{0.3})_{.47}In_{.53}As$	75		
5	Transition	$(Al_{0.9}Ga_{0.1})_{.47}In_{.53}As$	40	1×10^{18}	Si
4	Cladding N	InP	200	2×10^{18}	Si
3	Etch stop	InP	60	nid	
2	Sacrificial layer	InGaAs	1000	nid	
1	Buffer	i-InP	150	nid	
0	Substrate	InP Sub		n-type	

2. III-V coupon release

The III-V laser epitaxial layer stack used in this work is shown in Table 1. The laser structure consists of a 200 nm thick highly-doped InGaAs p-contact layer, a 1.5 µm p-InP cladding, a pair of 75 nm InGaAsP SCH layers, a pair of 40 nm AlInGaAs transition layers, an active region with 6 AlInGaAs quantum wells separated by AlInGaAs barriers, and a 200 nm n-InP contact layer with 60 nm intrinsic InP underneath. A 1 µm thick intrinsic InGaAs layer is used as the release layer. A 100 nm thick InP cap layer is included in the layer stack to obtain a high quality p-contact. The overall thickness of the III-V layer stack that will be printed onto the target photonic circuit is around 2.3 µm.

The release process is described in Fig. 3. The III-V coupon is defined by first etching a mesa through multiple steps of wet and dry etching using a SiN hard mask – after removing the 100 nm thick InP cap layer (Fig. 3(b)). In order to have a "V" shape waveguide cross section and thus a narrow taper tip in the laser waveguide definition by wet etching of the p-InP [22], the long side of the coupons was oriented along the [011] crystal axis. After etching into the n-InP layer, a second mesa which is 5 µm wider than the first one was defined, as shown in Fig. 3(c). For this purpose a 1:1 $HCl:H_2O$ solution was used to etch the n-InP and stop on the InGaAs release layer. Using a photoresist mask and dry etching the release layer was etched through 300 nm into the InP substrate (Fig. 3(d)). Then the coupons were

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encapsulated by a 2.5 µm thick photoresist layer patterned in such a way that the device coupon is protected, the release layer is locally exposed, while also tethers are defined that will anchor the coupon to the substrate after release. A top-view of the coupon after photoresist encapsulation is shown in Fig. 3(f). The under-etching of the InGaAs release layer was carried out using an aqueous $FeCl_3$ solution at 7°C. For under-etching a 40 µm wide coupon close to 8 hour etching was required.

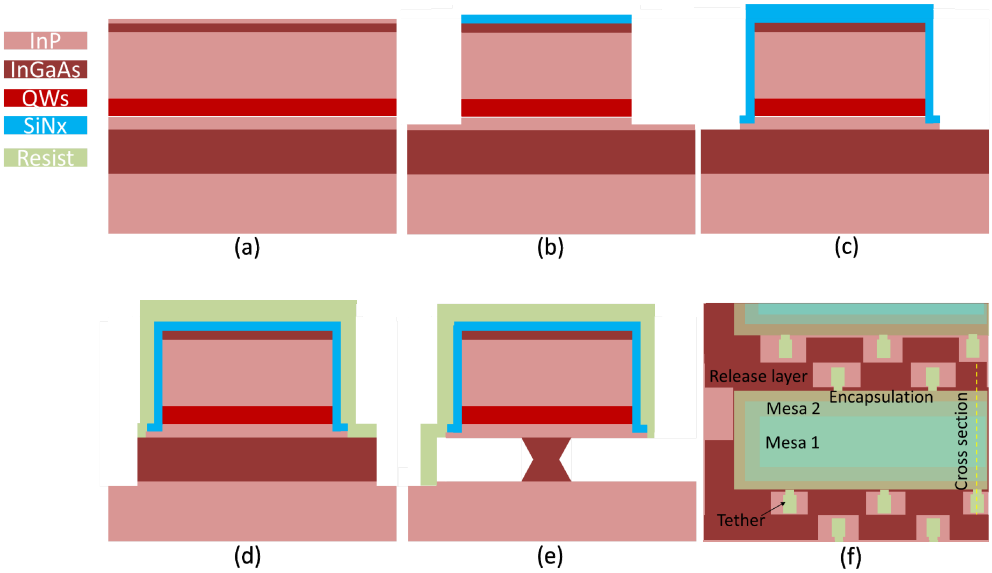

Fig. 3. Process flow of coupon patterning and release. (a) The initial III-V layer stack, (b) Sacrificial layer removal and first mesa definition, (c) Second mesa definition, (d) Etching of the release layer, (e) Resist encapsulation and under etch of the release layer, (f) Layout of the device coupon after photoresist encapsulation.

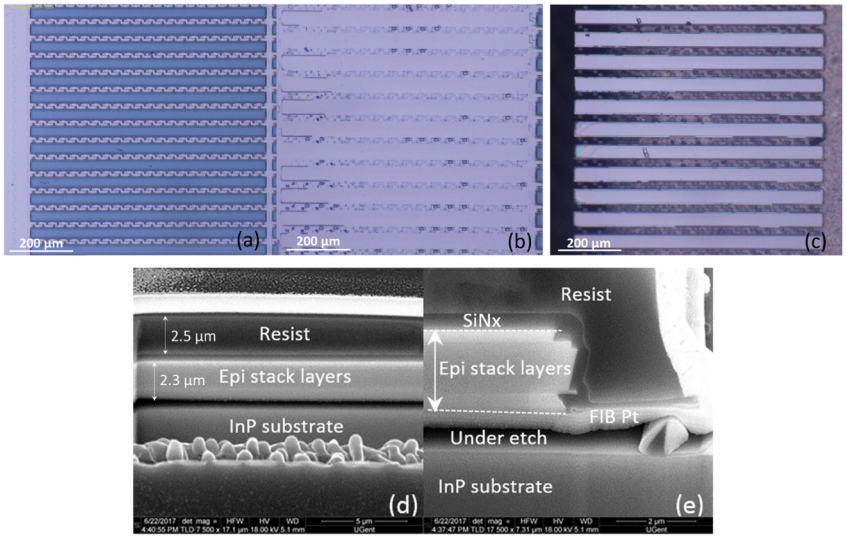

Fig. 4. The released coupon arrays patterned on the native InP substrate, (a) Dense coupon array, (b) Surface of the InP substrate after picking an array of coupons, (c) Bottom surface of the coupons, (d) Focused ion beam (FIB) cross section image of a released coupon, (e) Zoom-in image of the cross section.

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Figure. 4(a) shows a microscope image of the coupon array patterned on the InP substrate. Coupons with a length of 970 μm and a width of 40 μm were patterned on a ~1 × 1 cm^2 III-V die in arrays with a vertical pitch of 70 μm. Figure 4(b) shows the InP source substrate after picking an array of device coupons. A clean and smooth substrate surface beneath the coupons testifies to the successful release. Figure 4(c) shows the bottom surface of the picked coupons. As the focused ion beam (FIB) cross section image shows in Fig. 4(d) the InGaAs release layer is completely etched away, leaving the coupon suspended on the InP source substrate. The sidewall of the coupons, as shown in Fig. 4(e), is well protected by the SiN hard mask, which prevents the penetration of $FeCl_3$ to the active region and InGaAs contact layer during the release.

3. Transfer printing of the III-V coupons and their post-processing

3.1 Transfer printing of III-V coupons on the Si PIC

The transfer printing process is illustrated in Fig. 5. The stamp is laminated to the source substrate and is then accelerating away from the substrate such that the velocity of the stamp is high enough to break the tethers and therefore pick-up the coupons. In the printing process the stamp with the coupons is laminated against the target waveguide circuit - onto which a DVS-BCB bonding layer was spin-coated - such that a good contact and hence a high-quality adhesive bonding is obtained. Then the coupon was detached from the stamp by slowly lifting up the stamp after applying a shear, leaving the III-V coupon attached to the target waveguide circuit.

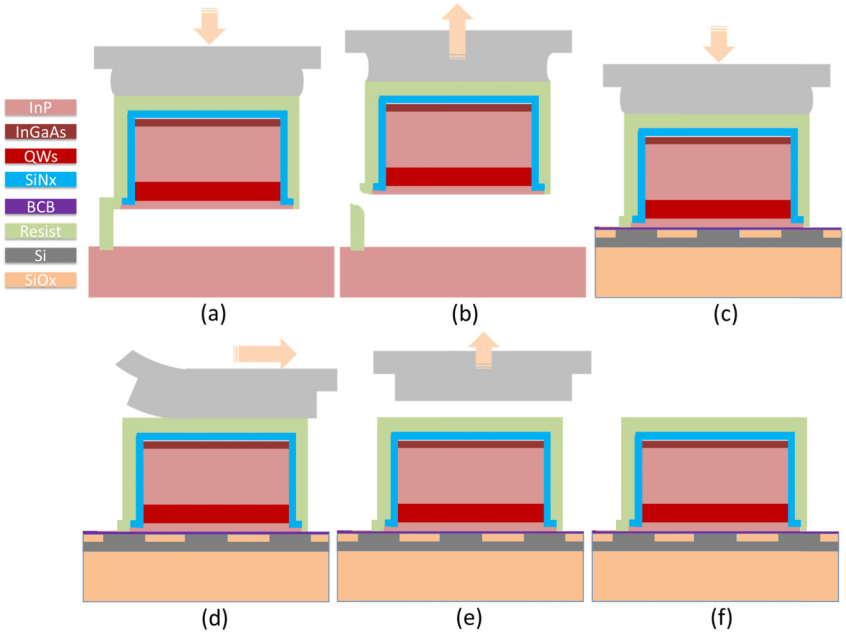

Fig. 5. Transfer printing of the III-V coupons: (a) Laminating the PDMS stamp to the released coupon on the source substrate, (b) Picking up the III-V coupon by rapidly lifting up the stamp, (c) Laminating the III-V coupon against photonic target substrate with a slight overdrive, (d) Applying a shear force to detach the III-V coupon from the stamp, (e) Lifting up the stamp, (f) The transfer printed III-V coupon on the target photonic circuit.

For process development purposes III-V coupons were printed on a passive silicon photonic waveguide circuit consisting of a 400 nm silicon device layer on a 2 μm buried oxide layer, etched 180 nm to define the waveguide structures and planarized using SiO_2 down to the silicon device layer. A DVS-BCB:mesitylene 1:6 solution is spin coated at 3000

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rpm on the silicon photonic target substrate, followed by a soft bake at 150°C and cooling down to room temperature, resulting in a 20 nm thick DVS-BCB bonding layer. 970 μm long and 40 μm wide coupons were printed onto this target waveguide circuit. A PDMS stamp with a 1000 x 60 μm^2 post was selected to pick up and transfer print the coupons to the desired locations on the PIC, using an X-Celeprint μTP-100 tool. As the coupons are long, additional care has to be taken to have good angular alignment between the coupon and the photonic waveguide structure. After the source and target substrates were loaded in the X-Celeprint μTP-100 tool, the source and target stages were carefully mapped such that the devices have the best angular alignment possible. An example of an array of printed III-V coupons is shown in Fig. 6(a), before the removal of the photoresist encapsulation. A 40 μm wide tilling free area, showing as the bright bars in Fig. 6(a) are used to define the printing area. A cross-section image of the III-V-on silicon coupon at the end and in the middle of the coupon is shown in Figs. 6(b) and 6(c) respectively. No air voids or delamination could be observed, illustrating the high quality of the bonding interface. The n-InP thickness varies between 240 nm and 145 nm from the center to the edge of the coupon along the long axis of the coupon due to the limited etch selectivity of the aqueous $FeCl_3$ [18, 20]. The thickness of the DVS-BCB bonding layer is uniform thanks to the elastic PDMS stamp which makes the pressure uniformly distributed along the coupon when the stamp is laminated against the target waveguide circuit in the printing process. The variation of the n-InP thickness along the laser length leads to a longitudinal variation of the coupling coefficient with the highest coupling near the edges of the coupon. This has little effect on the laser behavior, on the contrary the κ-profile suppresses the spatial hole burning [23]. The average κL-value, extracted from the stopband, is close to 5, a value giving low mirror loss.

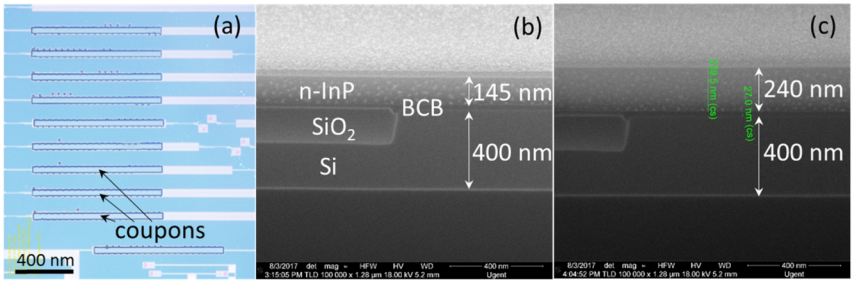

Fig. 6. (a) Array of printed III-V coupons on a silicon photonic target substrate (before photoresist encapsulation removal). (b) Cross section image at end of the coupon; (c) Cross section image in the middle of the coupon.

3.2 III-V coupon process flow

In our DFB laser demonstration, a group of second order DFB lasers with a grating length of 300 μm was studied. The period and duty cycle are 477 nm and 75%, respectively. A pair of two-step adiabatic tapers 50 μm away from each side of the grating were implemented to allow the optical mode to couple from the III-V to the silicon waveguide [24]. In order to reduce the DFB grating coupling coefficient, an additional 15 nm of SiO_2 was deposited on the silicon waveguide circuit, before spin coating the DVS-BCB bonding layer. This results in a larger separation between III-V and silicon and hence a weaker DFB grating coupling coefficient. Figure 7 describes the process flow for the definition of the III-V mesa structure in the transfer-printed coupon. After printing, the photoresist encapsulation is removed by an RIE oxygen plasma. Then the DVS-BCB bonding layer is fully cured at 270°C. The exposed DVS-BCB layer is also removed by the O_2 plasma, as indicated in Fig. 7(b), leaving the Si waveguides exposed. Therefore, a SiN protection layer is deposited (Fig. 7(c)) and a resist layer is used to planarize the structure (Fig. 7(d)). Then the resist is thinned down and the SiN

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hard mask layer on top of the III-V is removed through dry etching to expose the p-InGaAs contact layer (Fig. 7(e)). Again, a SiN layer is deposited and patterned using 300 nm UV lithography as a hard mask to define the laser mesa and taper structures, accurately aligned (<300 nm) to the underlying Si waveguide circuit. ICP etching was used to etch the laser mesa down to the AlInGaAs active layer, after which a short HCl etch is used to create the V-shape waveguide cross section [22] (Fig. 7(f)). After exposing the AlInGaAs active region to 1:1:20 H_2SO_4:H_2O_2:H_2O and 1:10 BHF: H_2O to remove the surface oxides, 50 nm SiN is deposited at room temperature together with a 150 nm thick SiN deposited at 270°C to passivate the active region. This SiN is also used as a hard mask to etch the active region. The quantum well active region is kept 6.3 μm wide in the laser mesa (while the p-InP mesa is 2.35 μm at the bottom), while it is narrows down to the width of the p-InP mesa close to the taper tip, in order to achieve efficient optical coupling to the silicon waveguide layer (Fig. 7(g)). Ni/Ge/Au is deposited on the n-InP layer through a lift-off process, as shown in Fig. 7(g). Again, the sample is passivated using SiN (Fig. 7(h)), after which the device structure is planarized using DVS-BCB, which is etched back (together with the SiN) to expose the InGaAs contact layer for Ti/Au metal deposition (Figs. 7(i)-7(j)). After opening the vias to reach the n-contact metal (Fig. 7(k)), the process is finished by a thick Ti/Au deposition (Fig. 7(l)).

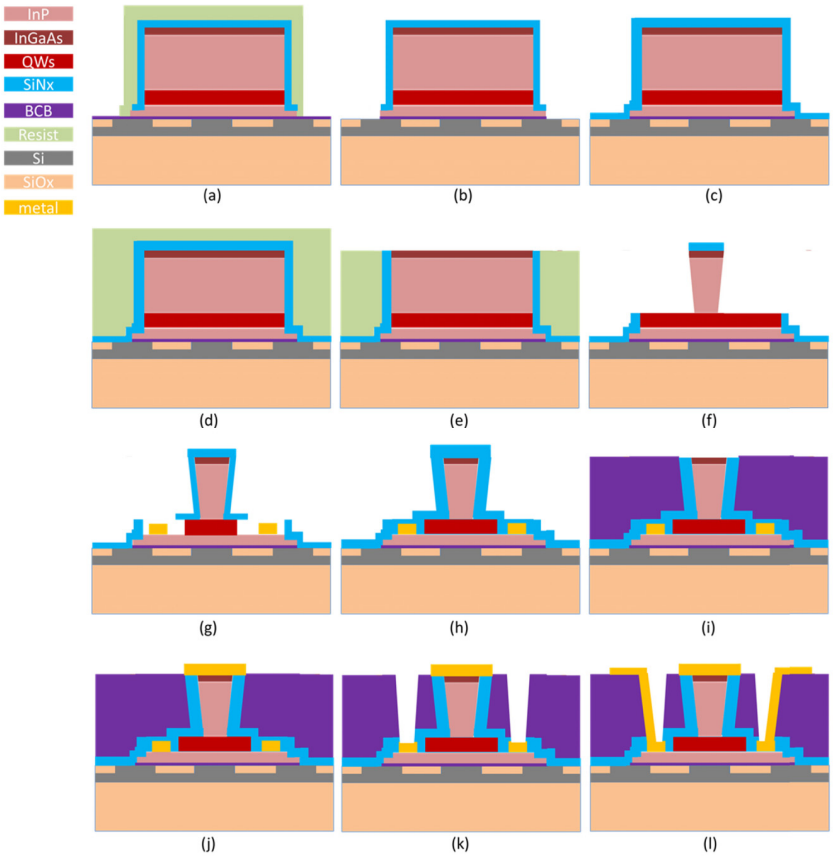

Fig. 7. Process flow for the definition of the III-V mesa structure in the transfer-printed coupon. (a) Transfer printed III-V coupon onto Si PIC, (b) Resist removal, (c) SiN deposition, (d) Resist planarization, (e) Etching back to expose the p-InGaAs layer, (f) Laser mesa and taper definition, (g) QW patterning and n-contact metal deposition, (h) SiN passivation, (i) DVS-BCB planarization, (j) p-contact metal deposition, (k) n-via opening, (l) Final Ti/Au metallization.

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Figure. 8(a) shows a top-view of a transfer printed III-V-on-silicon DFB laser. Figures 8(b) and 8(c) show the V-shaped III-V mesa in the III-V-on-silicon laser and close to the III-V taper tip respectively, resulting from the HCl based anisotropic etching. Due to charging induced by the DVS-BCB and SiN the silicon waveguide underneath is not visible in Fig. 8(b). As shown in Fig. 8(c) an alignment accuracy better than 250 nm is obtained. A III-V/Si separation (SiO_2 + DVS-BCB) of ~35 nm can be observed in Fig. 8(c).

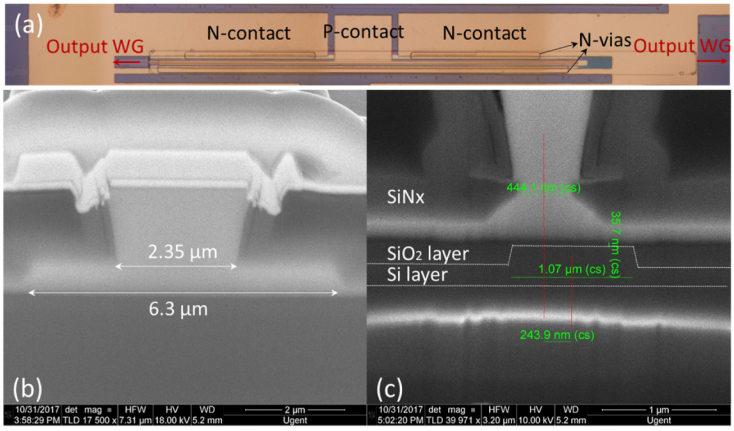

Fig. 8. (a) Top-view microscope image of a transfer-printed DFB laser, (b) FIB cross section image in the middle of the DFB laser, (c) FIB cross section image near the III-V/Si taper tip, showing a misalignment of less than 250 nm.

4. Device characteristics

The laser characterization was carried out on a temperature-controlled stage. A Keithley 2401 current source was used to bias the devices through a pair of DC probes. The optical power is collected by a standard single mode fiber through a fiber-to-chip grating coupler, which has a maximum coupling efficiency of −8 dB at 1550 nm. The collected optical power is split by a 3 dB coupler with one branch feeding a power meter and the other one connected to an optical spectrum analyzer. The optical power coupled to the waveguide was obtained by calibrating out the loss introduced by the grating coupler and the fiber-optics. Figure 9(a) shows the I-V curve of a typical DFB laser with a 300 µm long grating at room temperature with a differential resistance of 15 Ohm at 70 mA. The P-I curves are shown in Fig. 9(b). As the temperature increases from 20°C to 50°C the threshold current increases from 18 mA to 30 mA. The maximum single-sided waveguide-coupled output power is above 2.2 mW. Figure 9(c) shows a superposition of the DFB spectra at 25°C, showing single mode operation up to 70 mA drive current with a minimum side mode suppression ratio (SMSR) of 40 dB. The lasing wavelength shows 3.5 nm red shift when the laser bias varies from 20 mA to 70 mA, as shown in the inset of Fig. 9(c). As shown in Fig. 9(d), the lasing wavelength at 60 mA bias current shows a red shift of 2.5 nm when the stage temperature increases by 30°C, while the SMSR is unaffected. From these measurements we can deduce a thermal impedance of the III-V-on-silicon DFB of 290 K/W.

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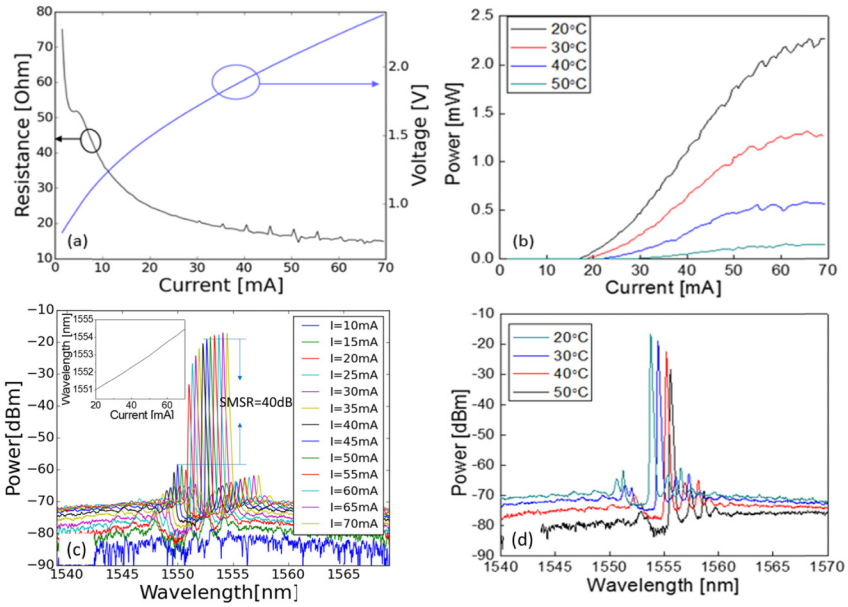

Fig. 9. Performance of the fabricated DFB laser. (a) V-I curve and differential resistance, (b) P-I curve at different temperatures, (c) Superposition of the output spectra at different bias currents, the inset shows the laser wavelength evolution as a function of current (d) Wavelength shift as a function of the stage temperature.

5. Conclusion

A III-V-on-Si DFB laser based on transfer-printing-based integration was demonstrated in this work. Single mode operation with more than 40 dB SMSR and a single-sided waveguide-coupled power up to 2.2 mW were achieved for bias currents up to 70 mA. This demonstration illustrates the potential of integrating III-V active devices by means of transfer printing. With advantages such as significantly improved material usage, the capability of wafer scale integration and the possibility of integrating multiple coupons/devices based on different materials, transfer-printing-based integration is expected to play a vital role in the fabrication of integrated photonics circuits in the future.

Funding

European Union's Horizon 2020 Research and Innovation Programme Grant No 645314 (H2020 TOPHIT project); Science Foundation Ireland Grant 12/RC/2276 (IPIC).

Acknowledgments

The authors would like to thank Liesbet Van Landschoot for the FIB cross-sections. We are grateful to K. Thomas for epitaxy system support.