Digitally Programmable Voltage-Mode Universal Biquadratic Filter

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ABSTRACT

A single input multi-output voltage mode universal biquadratic filter has been presented. The circuit incorporates digital programmability employing three plus-type differential voltage current conveyors (DVCCs), two grounded capacitors and three resistors. The circuit exhibits high input impedance realizes all the standard filter functions having orthogonal control of cut-off frequency and quality factor. Parameter tunability is achieved by the use of a 3–bit digital control word. The proposed circuits are amenable for monolithic integration by virtue of the fact that only grounded capacitors are employed. Circuit simulations using PSPICE are in perfect agreement with the theoretically predicted results.

General Terms

Digitally Programmable, Universal Biquadratic Filter.

Keywords

Digital Control, Digitally Controlled Differential Voltage Current Conveyor, DC-DVCC, Programmable Circuits.

1. INTRODUCTION

There has been a myriad of applications that involve realization of active transfer functions employing current conveyors, which have received a considerable amount of research attention [1].The continuous-time analog filter is a ubiquitous circuit component in a vast variety of applications including, but not limited to, noise rejection & signal separation in industrial and measurement circuits, feedback of phase & amplitude control in servo loops, smoothing of digitally generated analog signals, audio signal shaping & sound enhancement, channel separation & signal enhancement in communication electronics [1]–[14].

Active filter design generally employs one (or more) active building block and passive components like capacitors and resistors; inductors being avoided due to their incompatibility with the standard CMOS fabrication process. The active element may be one of the following: operational amplifier, second generation current conveyor (CCII) [9], operational trans-conductance resistance amplifier (OTRA) [8], fully differential current conveyor (FDCCII) [4], third generation current conveyor (CCIII) [11], differential voltage current conveyor(DVCC) [5],[6], [10], [12]. Circuit design using each of these building blocks has its own associated advantages and limitations with the DVCC offering the highest amount of flexibility and simplicity in analog electronic circuit design.

Voltage-mode active filters exhibiting high input impedance are of great interest as a number of cells can be easily cascaded for the realization of the higher order filters. However, it needs to be mentioned that the advantage of easy cascading can only be obtained in voltage-mode active filters which exhibit high input impedance [2-3].In this paper, digitally programmable DVCC-based implementations for voltage-mode universal biquadratic filter has been presented. All standard filter functions can be simultaneously realized which enhances the circuit utility in terms of its usage and reducing the overall cost of the circuit.

This paper is organized as follows. Section 2 presents a brief review of existing works on the realization of active filters. Section 3 contains an explanation of the operation of the Digitally-Controlled DVCC (DC-DVCC).Section 4 deals with details of the proposed universal biquadratic filter along with the design equations. Section 5 presents the results of computer simulations of the proposed circuit using PSPICE program. Some concluding remarks appear in section 6.

2. EXISTING METHODS

Analog filter design using a variety of active building blocks has been an active area of research for the past two decades. Operational amplifier was the active element of choice during the earlier stages of development. Later, the advent of current conveyors signaled the era of mixed-mode and current-mode signal processing. Since there has been a significant amount of technical literature available on the subject, it is not possible to attempt a thorough review of all the related works. Therefore, a survey of some of the recently published works is presented in this section. The DVCC was introduced by Elwan & Soliman and its application in continuous-time filters was also discussed [10]. Adawy, Soliman & Elwan later proposed another analog building block *viz.* the Fully Differential Current Conveyor (FDCCII) and several applications in electronic filters were also presented [7].One significant feature of the filters designed using FDCCII was the possibility of obtaining fully-differential processing. Cakir, Cam & Cicekoglu put forward an all-pass configuration employing a single OTRA [8]. Minaei & Ibrahim employed the DVCC for implementing a general topology for obtaining current-mode first-order APF [12]. A third-generation current conveyor (CCIII) was utilized to yield a trans-admittance type first-order filter [11]. Chiu *et al.* reported voltage-mode universal biquadratic filter simultaneously realizing all the standard functions all-pass, high-pass, band-pass, band-reject and low-pass filter sections based on DVCC, which forms the background for the present work. [13]. Minaei & Ibrahim presented a mixed-mode universal filter based on the KHN-biquad topology employing DVCCs [11]. Another voltage-mode all-pass filter using DVCC as the building block is attributed to Minaei & Yuce [5]. More recently, Maheshwari *et al.* used the FDCCII to realize cascadable all-pass/notch filters employing only grounded capacitors as the passive elements [4].

3. DIGITALLY PROGRAMMABLE DVCC

Since its introduction by Sedra& Smith in 1970, the Current Conveyor (CCII) has proved to be a very versatile analog building block that can be used to implement a wide variety of analog signal processing applications[14]

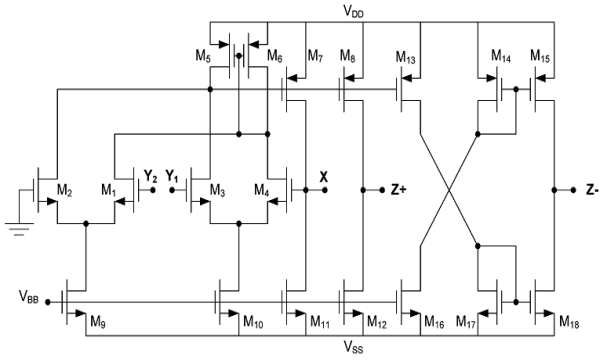

Fig. 2. CMOS implementation of DVCC (asdfgh, 2009)

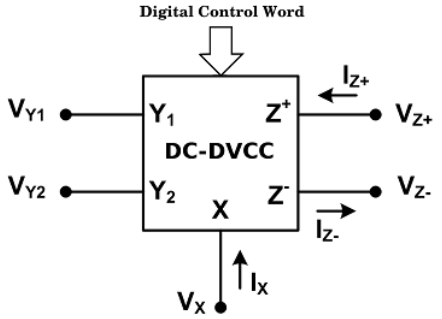

Fig. 1. Electrical symbol of DC-DVCC[14]

However, when it comes to applications demanding differential or floating inputs like impedance converters and quadrature oscillators which require two highinputimpedance terminals, a single CCII is not generally sufficient. To overcome this shortcoming, the Differential Voltage Current Conveyor (DVCC) was first introduced by Pal, and later developed by Elwan&Soliman[8].The DC-DVCC, shown in Fig.1,is essentially a 5-terminal block defined by the following relations:

While the voltage on the X-terminal follows the difference in voltages of terminals Y1 and Y2, a current injected at the X-terminal is replicated by a factor *k*to the Z-terminals. For the Z+ terminal, the direction of the conveyed current is the same as that of the current flowing in the X-terminal whereas for the Z- terminal, the current flows in the opposite direction. Ideally, *k* is unity. One possible CMOS realization of the

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z_+} \\ I_{Z_-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ k & 0 & 0 & 0 & 0 \\ -k & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z_+} \\ V_{Z_-} \end{bmatrix} \quad (1)$$

DVCC is shown in Fig. 2 [14]. As can be seen, the current at Z+ port will be the same as the current in the X terminal and the current at the Z-terminal will have the same magnitude but opposite direction as the X port current. To obtain a digitally controlled DVCC (DC-DVCC) from a DVCC, the technique is to control the current transfer gain parameter *k* of the DVCC by replacing the Z terminal transistors of the DVCC with transistor arrays associated with switches [13]. The gain parameter *k* can take values from 1 to (2*n*– 1), where *n* represents the number of transistor arrays.

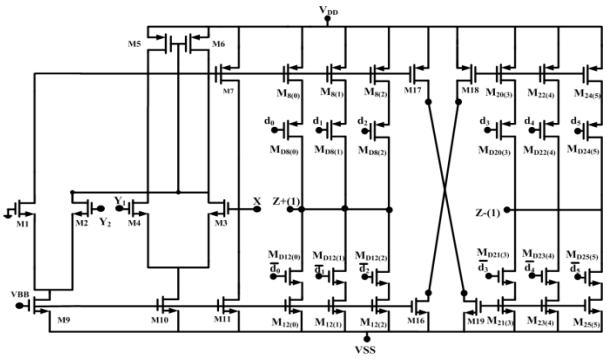

Fig. 3. CMOS realization of Digitally Controlled DVCC with gain *k*[14]

Actually, the transistor arrays implementa current summing network (CSN) at the Z terminal. Thecircuit of DC-DVCC obtained after suitable modifications inthe circuit of Figure 2 is presented in Figure 3 [13]. The CSNconsists of *n* transistor pairs, whose NMOS and PMOS aspectratios are given by:

$$\text{PMOS} \qquad \left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_7 \quad (2)$$

$$\text{NMOS} \qquad \left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{11} \quad (3)$$

Therefore, the current at the Z terminal, assumed flowing outof the DC-DVCC, can be expressed by

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{11}) \quad (4)$$

Therefore, the proposed DC-DVCC provides a current transfer gain equal to:

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{11})}{(I_7 - I_{11})} = \sum_{i=0}^{n-1} d_i 2^i \quad (5)$$

Parameter d_i represents the digital code-bit applied to the *i*-th branch in the CSN. Depending upon its value, it enables or disables the current to flow in that particular branch. It isinstructive to note the numbering of the transistors in the CSN.Transistors labeled $M_{8\,(i)}$and $M_{12\,(i)}$refer to the PMOS andNMOS transistors in the CSN that have been put there in theplace of their counterparts of Fig. 2.. Transistors $M_{D8\,(i)}$and$M_{D12\,(i)}$are the actual digital control transistors as the digitalcontrol bits d_0, $d_1$and $d_2$are applied at their respective gateterminals

4. PROPOSED CIRCUITS

This section presents the proposed DVCC-based voltage-mode universal biquadratic continuous-time filters with electronic control of filter parameters *viz.*gain and cut-off frequency. The circuit implementation employing DC-DVCC has been depicted in Fig. 4.The circuit has an advantage of using grounded capacitors that makes it feasible for integrated circuit implementation. The circuit has single input multi output configurations realizing all the standard filter functions *i.e.* low pass, high pass, band pass, band-reject and all-pass filter.

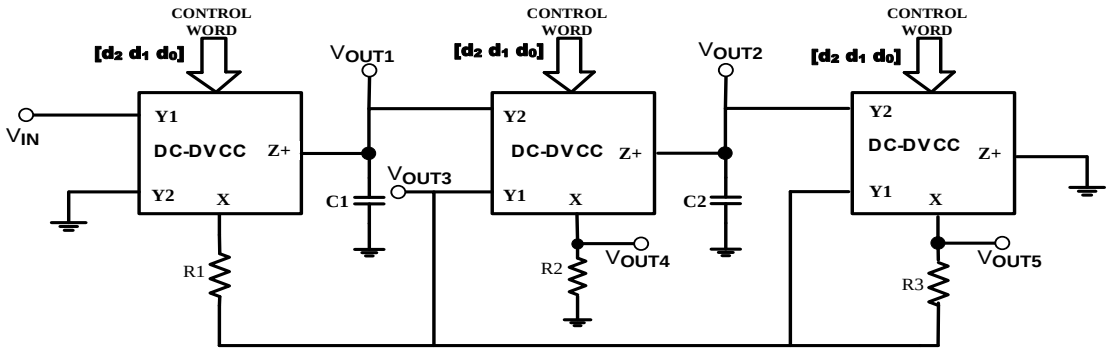

Fig. 4: DP-DVCC-based voltage-mode universal biquadratic continuous-time filters

The expression for the filter functions can be expressed as:

Low Pass (LPF)
$$\frac{V_{OUT1}}{V_{IN}} = \frac{\frac{k_1k_2}{C_1C_2R_2R_3}}{s^2 + \frac{sR_1k_2}{C_2R_2R_3} + \frac{k_1k_2}{C_1C_2R_2R_3}} \quad (6)$$

Band Pass (BPF)
$$\frac{V_{OUT2}}{V_{IN}} = \frac{\frac{sk_1k_2}{C_2R_2}}{s^2 + \frac{sR_1k_2}{C_2R_2R_3} + \frac{k_1k_2}{C_1C_2R_2R_3}} \quad (7)$$

Band Reject (BRF)
$$\frac{V_{OUT3}}{V_{IN}} = \frac{s^2 + \frac{k_1}{C_1C_2R_2R_3}}{s^2 + \frac{sR_1k_2}{C_2R_2R_3} + \frac{k_1k_2}{C_1C_2R_2R_3}} \quad (8)$$

High Pass (HPF)
$$\frac{V_{OUT4}}{V_{IN}} = \frac{k_1s^2}{s^2 + \frac{sR_1k_2}{C_2R_2R_3} + \frac{k_1k_2}{C_1C_2R_2R_3}} \quad (9)$$

All Pass (APF)
$$\frac{V_{OUT5}}{V_{IN}} = \frac{s^2 - \frac{sk_1k_2}{C_2R_2} + \frac{k_1}{C_1C_2R_2R_3}}{s^2 + \frac{sR_1k_2}{C_2R_2R_3} + \frac{k_1k_2}{C_1C_2R_2R_3}} \quad (10)$$

From equations (6) through (10) it can be seen that a low-pass response is obtained from $\mathbf{V_{OUT1}}$, a band-pass response is obtained from $\mathbf{V_{OUT2}}$, a notch response is obtained from $\mathbf{V_{OUT3}}$, a high-pass response is obtained from $\mathbf{V_{OUT4}}$, and if $R_1 = R_3$, all-pass response is obtained from $\mathbf{V_{OUT5}}$. The resonant angular frequency,ω_o, and the quality factor, Q, are given by:

Cut-off Frequency:
$$\omega_O = \sqrt{\frac{k_1k_2}{C_1C_2R_2R_3}} \quad (11)$$

Quality Factor:
$$Q = \frac{1}{R_1}\sqrt{\frac{k_1}{k_2}\frac{R_2R_3C_2}{C_1}} \quad (12)$$

Thus, the proposed circuit is capable of realizing all filter functions, that is, high-pass, band-pass, low-pass, notch, and all-pass filters simultaneously. Both ω_o and Q can be orthogonally controlled by $R_2$and/or R_3 and R_1.The circuit exhibits high input impedance which allows for easy cascadability of many similar stages of such filters to obtain higher order filters.Moreover, the proposed circuit has the following features: uses only plus-type DVCCs that simplify thecircuit configuration, orthogonal controllable of $\omega_o$and Q and the use of only grounded capacitors, which aresuitable for integrated circuit implementation.

5. SIMULATION RESULTS

The proposed circuits were simulated in PSPICE to ensure that the expected functionality is indeed obtained. The CMOS implementation of DC-DVCCin Fig. 3 employs TSMC 0.25µm CMOS technology process parameters. Fig. 5(a),(b), (c), (d) and (e) represents the simulated amplitude-frequency responses and phase-frequency responses for the low-pass($\mathbf{V_{OUT1}}$), band-pass($\mathbf{V_{OUT2}}$),notch($\mathbf{V_{OUT3}}$), high-pass ($\mathbf{V_{OUT4}}$) and all-pass ($\mathbf{V_{OUT5}}$) filters, respectively, designed with f_o=100KHz, C1=C2= 0.159nF and R1= R2= R3=10kΩ. It is obvious that the proposed circuit is capable of realizing all filter functions, that is, high-pass, band-pass, low-pass,notch, and all-pass filters simultaneously.

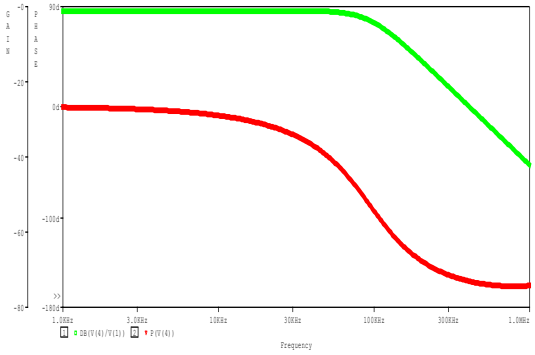

Fig. 5(a): Simulated magnitude and phase response for low pass filter with control word 1 [d_2 d_1 d_0 = 0 0 1] selected.

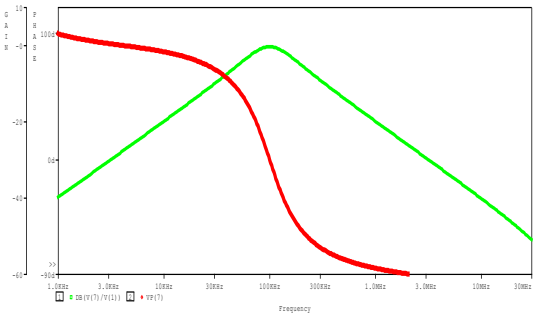

Fig. 5(b): Simulated magnitude and phase response for band pass filter with control word 1 [d_2 d_1 d_0 = 0 0 1] selected.

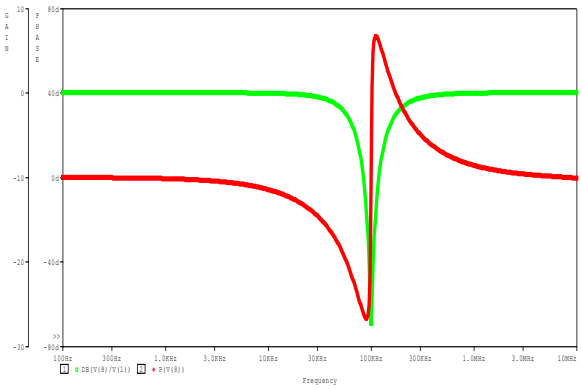

Fig. 5(b): Simulated magnitude and phase response for band reject filter with control word 1 [d_2 d_1 d_0 = 0 0 1] selected.

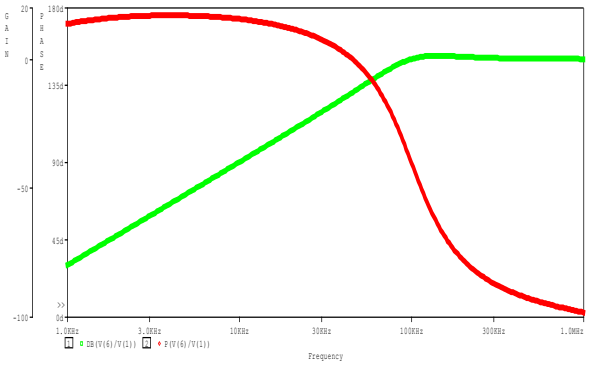

Fig. 5(d): Simulated magnitude and phase response for high pass filter with control word 1 [d_2 d_1 d_0 = 0 0 1] selected.

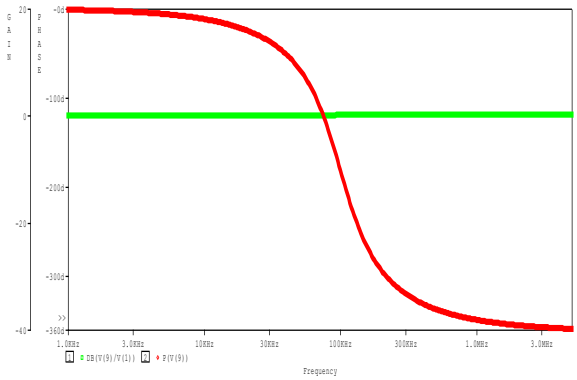

Fig. 5(e): Simulated magnitude and phase response for all pass filter with control word 1 [d_2 d_1 d_0 = 0 0 1] selected

Fig. 6, Fig. 7,Fig. 8 and Fig. 9 show resultant waveforms for LPF, BPF, BEF and HPF respectively for different control words by changing the associated bits where each bit corresponds to a particular binary weight when varied from [0 0 1] to [1 1 1]. Fig. 10(a) and Fig 10(b) depicts the variation in the APF magnitude response and phase response respectively when the 3 bit digital control word is changed from [0 0 1] to [1 1 1].

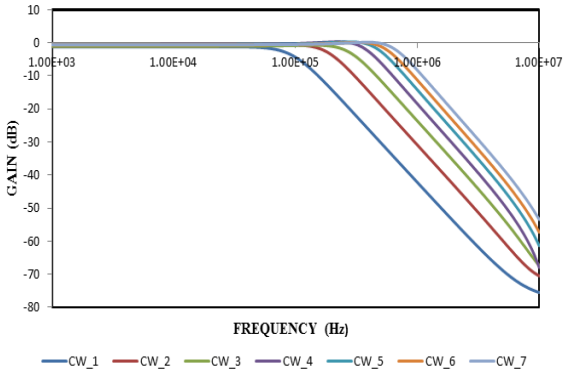

Fig. 6. PSPICE simulation result for the proposed digitally programmable LPF

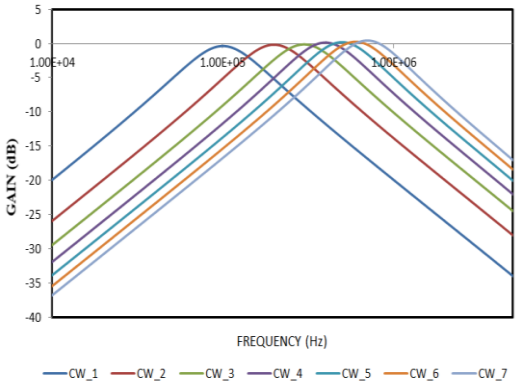

Fig. 7. PSPICE simulation result for the proposed digitally programmable BPF

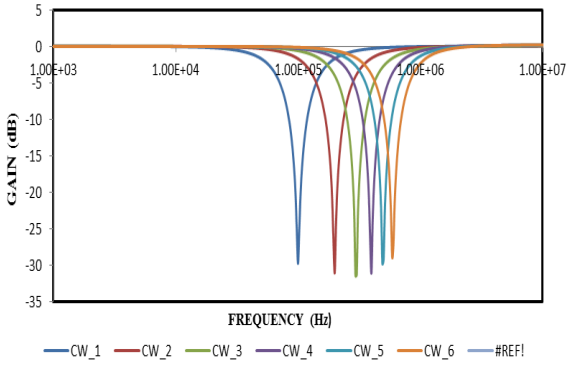

Fig. 8. PSPICE simulation result for the proposed digitally programmable BEF

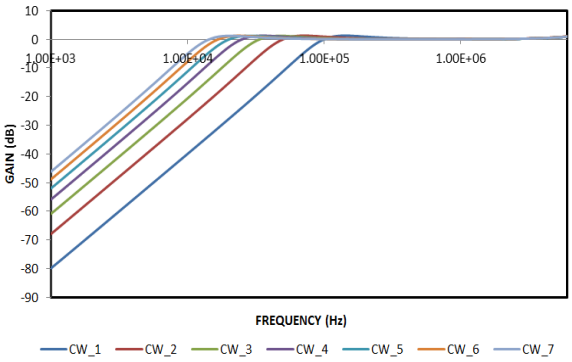

Fig. 9. PSPICE simulation result for the proposed digitally programmable LPF

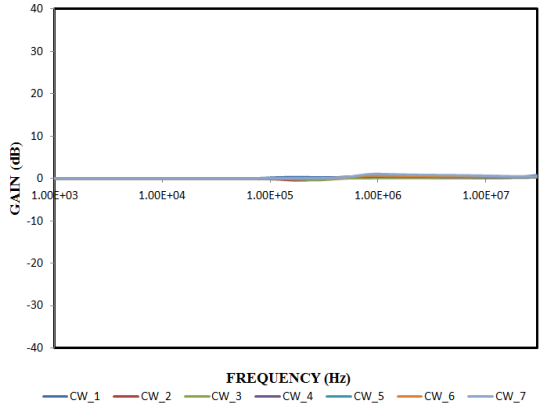

Fig. 10(a): PSPICE simulation result for the proposed digitally programmable APF(Magnitude Response)

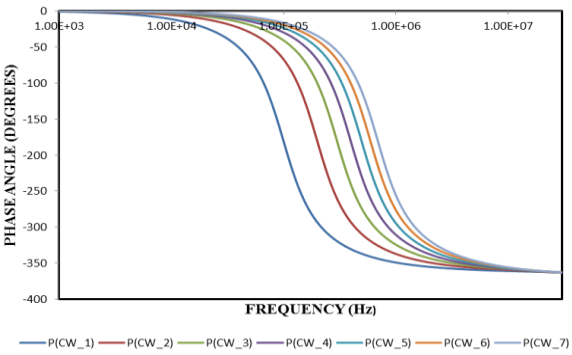

Fig. 10(b): PSPICE simulation result for the proposed digitally programmable APF(Phase Response)

Furthermore, Fig. 11, Fig. 12 and Fig. 13 illustrate the variation in control frequency with different control words. All the plots are in excellent mathematical conformity with the transfer functions given in equations (6) through (10). The cut-off frequency is found to vary from 98.22KHz to 705.32 KHz for low-pass filter,98.52KHz to 716.122KHz for band-pass filter,14.12KHz to 98.16 KHz for high-pass filter, 99.526 KHz to 703.12 KHz forthe band-reject filter by changing the control word from [0 0 1] to [1 1 1]. All the proposed circuits are compatible with contemporary CMOS processes as only MOSFETs and grounded resistors and capacitors are employed to realize all the standard filter functions.

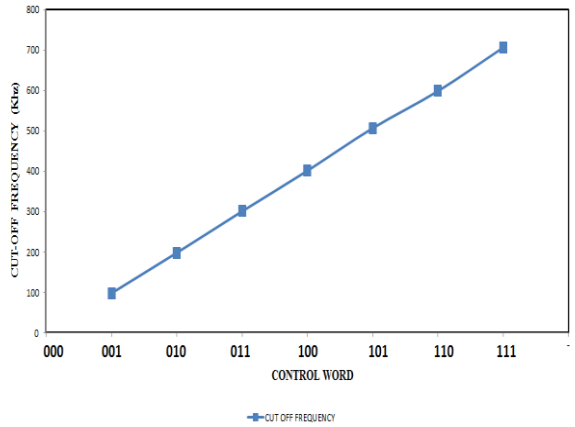

Fig. 11: Variation of cut-off frequency of the proposed LPF with digital control word

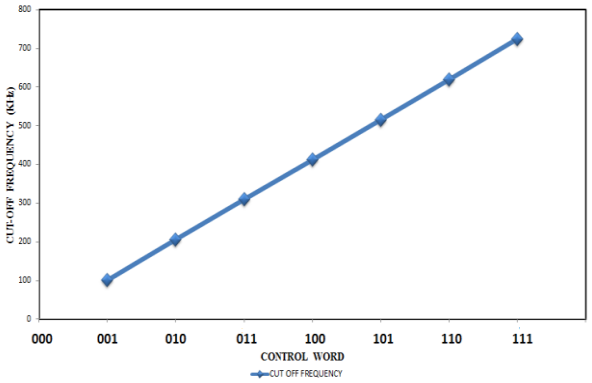

Fig. 12: Variation of cut-off frequency of the proposed BPF with digital control word

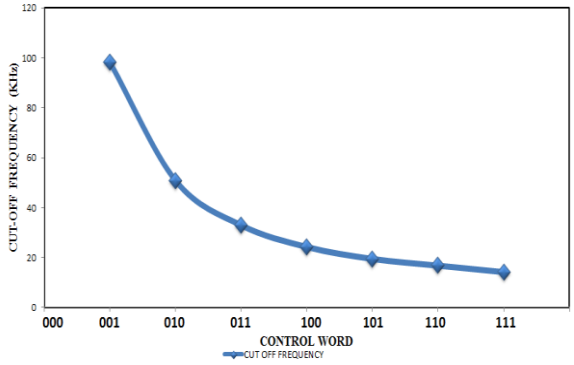

Fig. 13: Variation of cut-off frequency of the proposed HPF with digital control word

6. CONCLUSION

In this paper, a new digitally controllable voltage-mode universal biquadratic filter based on DVCC was presented. Digital tuning has been achieved by the variation of 3-bit digital control word. Standard low-pass, band-pass, band-reject, high pass and all-pass filterfunctions were obtained. PSPICE simulations were carried outto ascertain the working of the proposed filters and the resultsare found to match with the theoretical results.

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