Architecture of a Modular IEEE 802.15.4a Ultra-Wideband Transmitter

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***Abstract*— As part of a multi-channel, multi-band evaluation platform for future wireless sensor network applications, an IEEE 802.15.4a standard conform transmitter is investigated. The paper gives an overview of our transmitter concept and ultra-wide band signals according to IEEE 802.15.4a. It analyzes the system design aspects of the transmitter for high flexibility such as modularity and independency of dedicated modules from bandwidth and center frequency. The architecture of each module is described in detail and references to alternative solutions are given.**

I. Introduction

High-resolution positioning, high-precision ranging, and wireless sensor networks (WSNs) belong to the most important applications of today's ultra-wide band (UWB) systems. In particular, monitoring (e.g. area, fire and habitat monitoring), object tracking (e.g. location of patient devices, miner or animal tracking), and clinical surveillance attracted the attention of not only researchers, but also of medicine, military, and public safety groups.

In 2007, IEEE published the 802.15.4a "Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs): Alternate PHYs" which is an international standard for devices intended for WPANs, providing an ultra-low complexity, ultra-low cost, ultra-low power consumption alternate PHY for IEEE 802.15.4 with enhanced ranging capabilities, in particular with accuracies of one meter or better [1], [2].

This standard may be applied to WSNs which consist of a usually large number of sensors (nodes) enhancing the necessity of low-complexity, low-power devices. One can distinguish between nodes that operate as full-function devices (FFDs) that could be used for coordination or as a relay, and reduced-function devices (RFDs) that e.g. collect environmental data and send them to a FFD, either directly or via other nodes. Besides the strict energy constraints and the necessity of low-cost devices, WSNs offer challenges such as high resistance to fading and interference, scalability, good wall and floor penetration, low cost, and small size, whereas the extent of these requirements is application dependent. The resistance to fading and the good wall and floor penetration is already ensured by choosing ultra-wideband technology for the sensor networks [3].

The scope of this paper is to introduce an UWB transmitter for an IEEE 802.15.4a standard-conform platform for WSN applications. Compared to transceivers or transmitters for the same standard like [4] and [5], our transmitter shall be highly modular and flexible instead of energy efficient and integrable. The intended application is a reference transmitter as part of a research and development platform for measurement experiments like assessment of time of arrival (TOA) algorithms or precision and resolution determination in UWB tracking and positioning systems. In the next section, the paper gives a short introduction into typical IEEE 802.15.4a UWB transmit signals and shows a solution for their generation. Starting with Section III we give an overview of our transmitter concept and describe each transmitter module in detail in sections III to VI. In Section VII we conclude.

II. Signals in IEEE 802.15.4a PHY and Signal Generation

The IEEE 802.15.4a is intended for low-range, low-data-rate WPANs. Therefore, using time-hopping impulse radio (TH-IR) as proposed by IEEE enables us to design and build UWB systems with high performance and low to moderate complexity [6]. Although IR can operate in baseband, IEEE 802.15.4a systems typically operate in the $3-10\,\mathrm{GHz}$ frequency band. There are several channels defined. Each channel is assigned a number and is distinguished by its center frequency and bandwidth. Different bit rates are defined for each channel ranging from 0.1 to $27.24\,\mathrm{Mbit/s}$ as well as different code rates and mean pulse repetition frequencies (PRFs). These setup parameters have to be selected by the user. Each data bit from the MAC layer is first Reed-Solomon (RS) encoded. Afterwards, each bit is systematically mapped onto data symbols with two bits each by a convolutional encoder. These bits are then used to form the actual transmitted symbols. One bit determines the position of a pulse burst, the other selects the sign of the spreading sequence used in the burst.

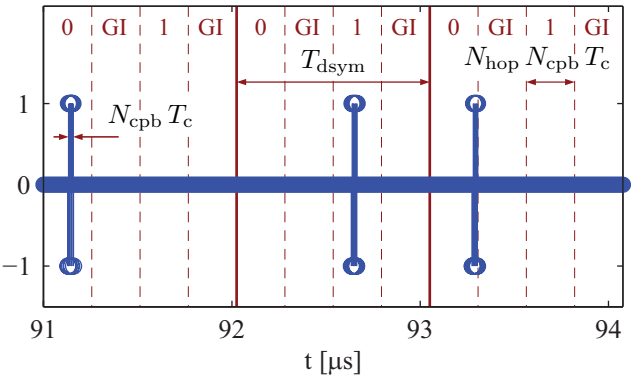

Fig. 1. Three data symbols of an IEEE 802.15.4a sample signal.

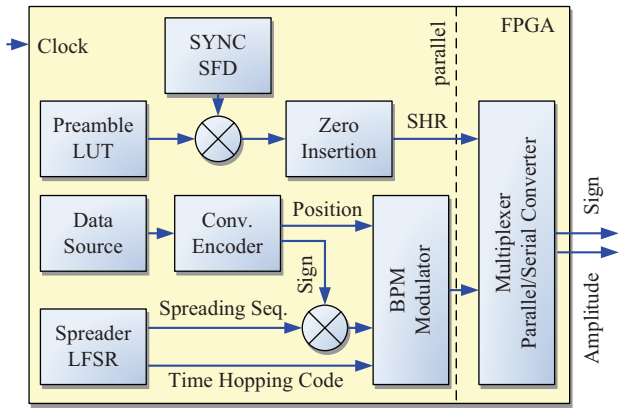

Fig. 2. Block diagram of the symbol source.

The overall modulation scheme is called burst position modulation - binary phase shift keying (BPM-BPSK). It can be broken down into ternary chip symbols, each element of the alphabet $\mathcal{A} = \{-1, 0, +1\}$ which are transmitted at a chip duration T_{c} of approximately 2 ns. Figure 1 gives an example of such a BPM-BPSK signal. Each data symbol with length T_{dsym} is divided into four periods with length $N_{\mathrm{hop}}\,N_{\mathrm{cpb}}\,T_{\mathrm{c}}$. According to the BPM the burst is active in the first or the third period depending on the position bit of the data symbol. The remaining periods are used as guard intervals (GIs) to compensate for multi-path delay spread. The actual position of the burst inside the selected period is defined by a time hopping sequence to mitigate multi-user interference. In the example given, each data symbol is $512\,T_{\mathrm{c}} = 1025.64$ ns long and each burst consists of $N_{\mathrm{cpb}} = 16$ active BPSK modulated pulses. This leads to a mean PRF of 15.6 MHz and a bit-rate of 0.85 Mb/s incorporating the encoding.

Figure 2 shows our proposed symbol source which will be implemented on a Xilinx Virtex-4-FX20 field programmable gate array (FPGA). The underpart generates the data symbols. The data source produces either random test data, information from a higher MAC layer, or information brought to the FPGA by an external source. This block also performs the RS encoding. It is followed by a convolutional encoder, resulting in two output bits per data bit. A linear feedback shift register

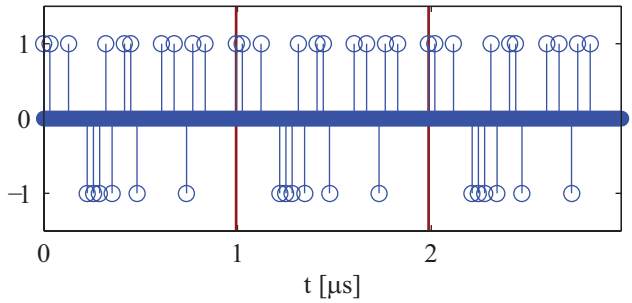

Fig. 3. First three preamble symbols of an IEEE 802.15.4a sample signal.

(LFSR) generates the spreading sequence used for each burst and also the time hopping sequence [7]. While the spreading sequence is multiplied with the sign bit, the BPM modulator uses the position bit to insert zeros before and after the burst where necessary. The result is a symbol stream of the alphabet $\mathcal{A}$ at the peak PRF of 499.2 MHz with a very low duty cycle (i.e. most of the symbols are zeros).

Each IEEE 802.15.4a PHY service data unit (PSDU) block is preceded by a preamble (synchronization header, SHR), and a PHY header (PHR). The first is used for synchronization and for determining the TOA in ranging mode, while the latter carries information about the actual transmission parameters used in the PSDU. The PHR is encoded in a similar way as the PSDU – although with a more restricted set of symbol/bit rates. It can therefore also be generated by the data source shown in Figure 2.

The SHR is not modulated using BPM-BPSK like the PHR and PSDU bits. A ternary code sequence from $\mathcal{A}$ with length 31 or 127 is spread by inserting a setup dependent number of zeros. This sequence is first read from a look up table (LUT). The SYNC part of the SHR plainly repeats the sequence which equals to multiplying it with $+1$. Afterwards, in the start-of-frame delimiter part (SFD) of the SHR this sequence is multiplied with another sequence from the alphabet $\mathcal{A}$. The repetition count for the SYNC part is later indicated in the PHR. The SFD sequence depends on the other transmission parameters and uses -1, 0, $+1$ for the multiplication. After the insertion of zeros the overall structure of the SHR is similar to the PHR and PSDU modulated symbols: The resulting symbols are from the alphabet $\mathcal{A}$, the chip rate is 499.2 MHz. However each preamble symbol is only 993.59 ns long. Figure 3 shows the first three preamble symbols of a typical IEEE 802.15.4a signal.

Inside the Virtex-4 all data mentioned so far is processed in parallel to lower the internal symbol rate while achieving the required bit rate. A multiplexer combines the resulting data from SHR, PHR, and PSDU. This is then parallel/serial converted at two RocketIO ports of the FPGA – once for the sign of each symbol, and once for the absolute value.

III. Overview of the Transmitter Concept

The previous section discussed UWB signals in the IEEE 802.15.4a standard and our proposed way of their gen-

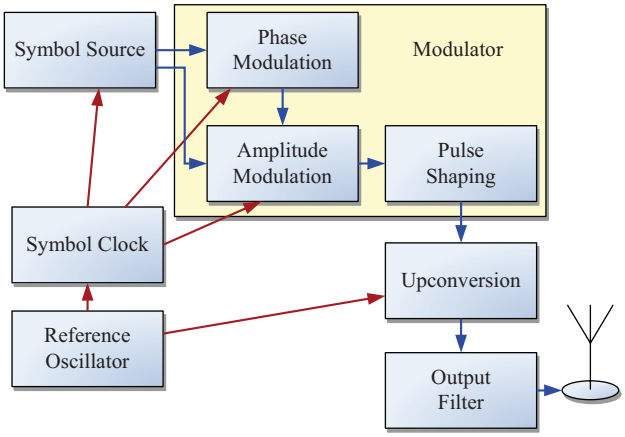

Fig. 4. Overview of the transmitter architecture.

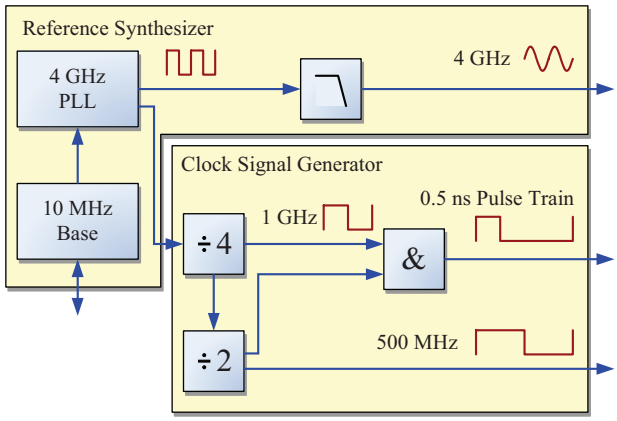

Fig. 5. Reference oscillator and symbol clock signals derived for channel 4 (frequency values are rounded).

eration. This section deals with the overall transmitter concept which includes the signal generation block already described. Our concept consists of eight building blocks, as it can be seen in Figure 4.

Each block can be realized in different ways to achieve the same overall behavior. The signal generation block described in Section II for example could be replaced by an arbitrary signal generator (ARB) or a bit pattern generator. It needs two outputs for the sign and the amplitude of each symbol. The symbol rate needs to be 499.2 MSymbols/s, and the memory depth 12.7 MSymbols per UWB frame for the maximal frame length. Each symbol consists of 2 bits. Since the symbol rate is not a common rate like 500 MSymbols/s, it has to be applied externally. Due to the modularity of our transmitter a comparison of all these realizations can be easily accomplished.

A symbol clock serves as the basis for all necessary clock and pulse signals. It is locked to a reference oscillator which also provides the upconversion local oscillator (LO) signal. LO and clock signal generation are described in Section IV.

The modulation is performed in five steps. At first, according to the sign bit, one of two pulse templates is chosen for each pulse during the phase modulation. Then the amplitude modulation uses only the amplitude bit to suppress or pass the pulses. Then these pulses are shaped in correspondence with the IEEE 802.15.4a standard by the pulse shaping network. Section V describes these steps in more detail. Next, the pulse sequence is upconverted to a channel dependent center frequency. The resulting signal is finally bandlimited and transmitted. The last two steps are described in Section VI.

IV. Local Oscillator and Clock Signals

Our IEEE 802.15.4a transmitter is designed for channel 4 which has a bandwidth of 1331.2 MHz and is located around a center frequency of $f_c = 3993.6$ MHz. This is the output frequency of the reference oscillator. For the mandatory channel 3 the reference oscillator is simply changed to 4492.8 MHz. The symbol clock has a PRF of 499.2 MHz. In our design the reference oscillator at 3993.6 MHz is divided by 8 to yield this clock signal. For channel 3, 4492.8 MHz is divided by 9. All other signals are deduced from the same reference signal by division. This eliminates the need for further synchronization inside the transmitter among the different clocks. It therefore reduces the overall complexity.

The reference oscillator is a fractional-N phase locked loop (PLL) synthesizer [8], [9], based on the ADF4153 from Analog Devices [10]. Two outputs are available, one providing a lowpass filtered sinusoidal signal, while the other outputs directly the signal from the voltage controlled oscillator (VCO). The synthesizer's output is phase locked to a 10 MHz oven controlled crystal oscillator. Optionally this 10 MHz signal can be applied externally and is also available at an SMA connector to synchronize other measurement equipment with the UWB transmitter. The left side of Figure 5 illustrates the reference oscillator and the 10 MHz oscillator.

The unfiltered 3993.6 MHz signal is first divided by 4 in two stages to yield a 499.2 MHz rectangular signal and is then divided by 2. The latter rectangular signal is the symbol clock for the signal source and the modulator. This signal is also logically 'and' concatenated with the 998.4 MHz signal which results in a pulse train with 0.5 ns pulse width. These signals and their generation are shown in Figure 5.

One of the main design objectives of the synthesizer is to provide highly stable, jitter free clock and LO signals. In an alternate future modification an adjustable pulse width of the pulse train might be of interest.

V. Modulation and Pulse Shaping

The modulator has to deal with a combination of amplitude and phase modulation. In each chip interval T_c there is either a positive, a negative, or no pulse, at a peak PRF of 499.2 MHz. These three states are encoded by an amplitude bit and a sign bit by the signal source.

The IEEE 802.15.4a standard actually proposes BPM-BPSK modulation for the PSDU. However, the signal source and the usage of ternary symbols at the PRF completely subsumes this behavior: The BPM inserts zeros where required, so it can be considered to be amplitude modulation or rather on/off keying (OOK). The BPSK modulation only determines

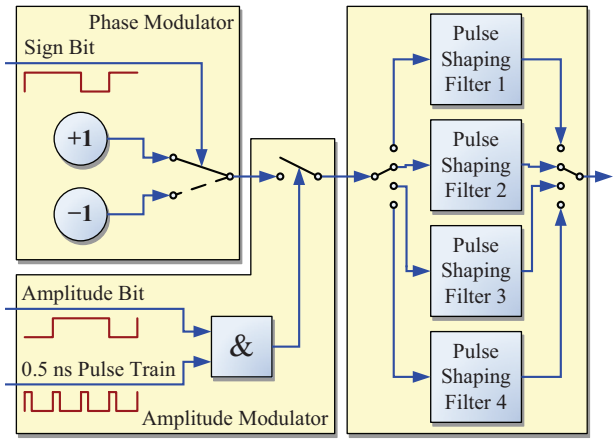

Fig. 6. Baseband modulator.

the sign of the output signal. The synchronization preamble does not use BPM-BPSK modulation but is again covered by the concatenation of amplitude and phase modulation as described in Section II.

For each chip interval T_c the phase modulator chooses a positive or negative voltage in accordance to the sign bit which is then active for the complete period. In Figure 6 this voltage is indicated by $+1$ and -1.

The amplitude bit from the signal source either suppresses or passes pulses of the $0.5\,\text{ns}$ pulse train from the clock generator. This is accomplished using a logical 'and' gate. In the second part of the amplitude modulator, the output signal from the 'and' gate controls an analog switch after the output of the phase modulator. The switch must not be operated during a voltage transition at its input. This is ensured by the delay times of the logic gates in the clock generator and the amplitude modulator respectively, and the fact that the pulse is shorter then the overall chip period.

The succeeding pulse shaping filter has to shape the more or less rectangular signal to fulfill the requirements of the IEEE 802.15.4a standard. The filter has to take all distortions introduced by the dividers, the logic gates, and the switches into account and may not assume an ideal rectangular input pulse. Therefore, it is necessary to optimize the filter components regarding the measured output of the baseband modulator. This optimization and the design of the passive pulse shaping filter can be done according to [11].

According to Figure 6 there are several different pulse shaping filters. The output signal of this modulator chain is a IEEE 802.15.4a compliant baseband signal and not dependent on the center frequency. It can be used for all channels with the same bandwidth. The channel assignment is then performed by the upconverter module. However, not all channels have the same bandwidth. For each channel the correct pulse shaping filter is chosen. The correct choice also depends on the width of the input pulse train from the clock signal source, which has to be taken into account.

VI. Upconversion and Output Stage

IEEE 802.15.4a operates in three frequency bands which are split into different channels. Except the sub-gigahertz band (250 to 750 MHz), all other frequency bands need a frequency shift to their respective center frequency. Therefore, the final stage is an upconverting mixer using the LO signal readily provided by the reference oscillator. To assure a IEEE 802.15.4a compliant operation, considering the power constraints and general practical aspects, the upconversion mixer has to provide

- high linearity,
- high port-to-port isolation,
- low power consumption and low LO drive,
- low conversion loss,
- high spurious rejection,
- and by all means broadband operation.

Of course optimizing all of these properties independently is impossible. Increasing the LO power level for example decreases the conversion loss, but at the same time increases the noise figure. Similarly, a double-balanced mixer architecture offers high spurious rejection, broadband operation and high port-to-port isolation at the cost of greater LO power requirements and higher conversion loss [12], [13]. Since broadband operation and high isolation are essential in our transceiver architecture a very good trade-off would be given by an active double-balanced mixer topology.

Commercially available broadband mixers with integrated matching can be found which are small, low-cost, broadband, and single-ended. But they often show poor port-to-port isolation and high conversion losses. An alternate way is to use a surface mounted device with good performance and provide the balanced-to-unbalanced and visa verse transformations and matching externally. One suitable device for up- and down-conversion is the LT5560 by Linear Technology, which is a broadband low-power active mixer. The data sheet promises high port-to-port isolation, a conversion gain of $2.4\,\text{dB}$, typically, supply current adjustable with a single resistor, and input third order intercept point at $9\,\text{dBm}$ for a supply current of $10\,\text{mA}$. The block diagram of the upconverter circuit is shown in Figure 7.

The $50\,\Omega$ unbalanced input pulse is transformed to $50\,\Omega$ balanced by the radio frequency (RF) pulse transformer TP-101 by M/A-COM. Its frequency range is from $500\,\text{kHz}$ to $1.5\,\text{GHz}$ with a very low insertion loss of $0.4\,\text{dB}$, typically. Also the 10-90% rise time of $0.18\,\text{ns}$ is short enough for our narrow-pulse application. The LO input may be driven single-ended. Hence, no unbalanced to balanced transformation is needed at this point. The balanced output port has to be converted to unbalanced again, since the succeeding transmitter components require unbalanced inputs. A possible solution is the broadband balanced-to-unbalanced (BALUN) transformer BD3150L50100A00 by Anaren Microwave. It covers a frequency range from 3.1 to $5\,\text{GHz}$ with an insertion loss of $1.1\,\text{dB}$, an unbalanced port impedance of $50\,\Omega$, and a balanced port impedance of $100\,\Omega$. External matching is also

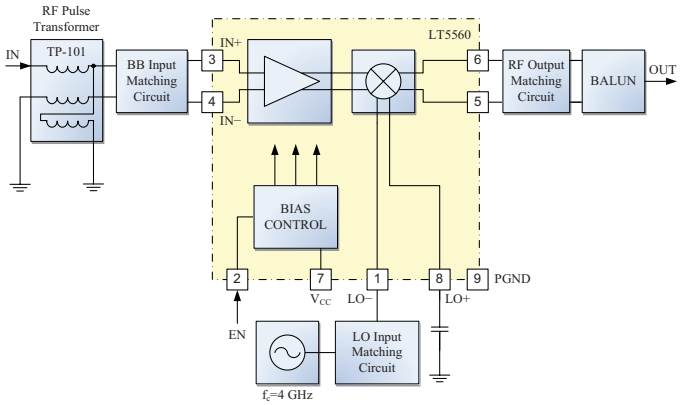

Fig. 7. Block diagram of the frequency converter circuit.

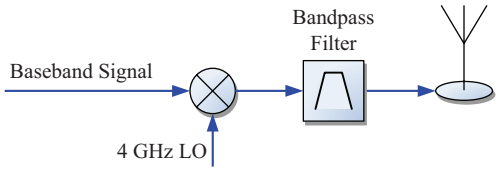

Fig. 8. Output stage of the transmitter.

necessary at every port. A guideline and the list of frequency-dependent complex impedances for every port is provided by the manufacturer. The upconverter can be used for the complete IEEE 802.15.4a low band.

After the upconversion, a final bandpass filter suppresses higher harmonic emissions by the mixing process and ensures compatibility with the spectral mask of IEEE 802.15.4a. Special care has to be taken to ensure flat group delay and avoid transient ringing. [14] and [15] give examples of suited filters using microstrip and coplanar waveguide (CPW) techniques.

Finally, the signal is transmitted by the antenna. Distortions due to the antenna – especially derivation – are taken into account by the modulation and pulse shaping modules. Figure 8 gives an overview of the elements of the output stage.

VII. Conclusion

The IEEE 802.15.4a is a recently published UWB standard for use in low data rate WSNs and WPANs. As part of our research and development platform, we present a transmitter for use in a various range of applications. These include WSNs, high-precision tracking and high-resolution positioning. Due to its modularity and since most modules are center frequency independent, the transmitter can be used for all channels of the IEEE 802.15.4a standard. The modularity also allows the rapid assessment of new algorithms, or testing of different hardware components. The challenges of all utilized blocks are analyzed in this paper and a detailed description is given.

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