Synthesis of Dual-\(V_T\) Dynamic CMOS Circuits

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Abstract
Main source of power dissipation for dynamic CMOS circuits is due to charging and discharging of intrinsic capacitances, commonly referred to as switching power. As switching power dissipation is proportional to the square of supply voltage, lowering the supply voltage is the most effective way to reduce switching power dissipation. However, the reduction of switching power by lowering the supply voltage takes place at the cost of performance. In order to maintain the performance, it is necessary to scale down the threshold voltage. But, as the threshold voltage is scaled down, the subthreshold leakage current increases dramatically leading to large increase in leakage power dissipation. Recent research has revealed that with the gradual shrinking of device sizes, the leakage power dissipation is becoming more and more dominant, and it is likely to become comparable to switching power dissipation in future generation VLSI circuits. This has motivated us to develop suitable technique for the reduction of leakage power dissipation in dynamic CMOS circuits, a problem, which has not been addressed by any researcher. This paper proposes a technique for containing the leakage power using two threshold voltages (dual-\(V_T\)) in the realization of circuits. Necessary care has been taken such that the dual-\(V_T\) dynamic circuits can be kept in standby mode and dissipates small leakage power. Substantial reduction in leakage power has been demonstrated without compromise in performance for both domino and nora style of realizations.

Keywords: Logic synthesis, dynamic circuits, domino logic, nora logic, unate decomposition, leakage power, low power, high performance, dual-\(V_T\).

1. Introduction
Dynamic CMOS circuits have a number of potential advantages compared to its full-complementary static CMOS counterpart, such as, lower transistors counts, higher speed, low-power, short-circuit power free and glitch-free operation, etc. These properties make dynamic CMOS circuits very attractive for the realization of low-power, high-performance systems. Dynamic CMOS circuits can be realized in one of the two popular forms - domino [1] and nora [2]. In domino CMOS circuits, pull-down evaluation network is implemented with nMOSFETs and output of one dynamic domino stage is connected through a static CMOS inverter to the next stage. On the other hand, dynamic nora is inverter free. Here dynamic stages are alternated with pull-down nMOSFETs network and pull-up pMOSFETs network. Both the logic styles are free from clock-skew problem [3], when more than one dynamic stages are cascaded. However, dynamic circuits suffer from two limitations - charge sharing and synthesis paradigm for circuit realization. Charge sharing problem in a dynamic domino gate is illustrated in Fig 1(a). In the evaluation phase, the load capacitance either remains in the charged state or discharges to zero logic level through pull-down network, depending on the input to the pull-down network. Suppose, input to the pull-down network is such that the pull-down network is “off” and hence load capacitance \(C_L\) remains in charged (high) state. But, the charge stored in \(C_L\) may get redistributed to charge the internal node capacitances in the pull-down network (Fig 1(a)) and if the amount of charge drained is large enough, then it can alter the logic level at the output. A weak pMOS transistor (called keeper transistor) can be added to replenish the charge lost in the evaluation period, as shown in Fig. 1(b)-(c). The keeper transistor provides steady current from other sources to compensate the charge loss due to leakage. However, the keeper transistor results in some reduction in performance due to introduction of the parasitic capacitance by the drain of keeper pMOSFET and the additional current that the pull-down network must fight during evaluation. For these reasons, keeper devices are generally designed with low doping concentration (weak conductivity) and with minimum dimension. It can be noted that there is no charge-sharing problem in pull-up networks of pMOSFETs in dynamic nora circuits and hence no keeper transistors are required in pull-up networks of pMOSFETs in nora circuits (Fig. 1(d)).

Another limitation of the dynamic CMOS circuits is that it can implement only non-inverting logic functions. This necessitates the realization of the complements of internal signals through separate cones of logic using complements of primary inputs resulting in significant area overhead. Therefore, the conventional synthesis paradigms used for static CMOS, which implicitly assume that the complement of any internal node is available using a single inverter, cannot directly be applied to the synthesis of domino (or nora) circuits. To alleviate this problem, unate decomposition of logic functions has been proposed [6], where functions are expressed in terms of positive and negative unate functions only.

In recent years, power dissipation has emerged as the key issue for the design of both high performance as well as hand-held portable systems. As switching power is proportional to the square of supply voltage (\(V_{DD}\)) and static power is directly proportional to it, supply voltage reduction has the most profound effect on power consumption of CMOS circuits. However, as supply voltage is lowered, there is degradation in
performance, which should be compensated by scaling down the threshold voltage \((V_T)\). For example, with a supply voltage of 1.0V, the threshold voltage should be scaled down to about 0.2V to get adequate performance. Unfortunately, reducing \(V_T\) results in an exponential increase in the leakage power. Main component of the leakage power is due to the subthreshold leakage current and it is becoming an increasingly dominant component of overall power consumption in deep sub-micron technologies [7]. Presently, development of the process technology for dual threshold voltage (dual-\(V_T\)) circuit technique has been known, where instead of a single threshold voltage, two threshold voltages can be used - low threshold voltage (low-\(V_T\)) to maintain the performance while high threshold voltage (high-\(V_T\)) to reduce the leakage power dissipation.

In this paper, we have proposed an approach for the synthesis of delay-constrained dual-\(V_T\) dynamic CMOS circuits. Two-level unate decomposition technique proposed in [6] and [8] has been used here for the synthesis of dynamic CMOS circuits. We have developed techniques for the assignment of low-\(V_T\) and high-\(V_T\) to transistors (dual-\(V_T\) assignment) such that the leakage power dissipation is reduced without compromise in performance. To analyze dynamic CMOS circuits realized with our approach, we have proposed estimation models to calculate delay, switching power and leakage power dissipations.

Remaining part of the paper is organized as follows. An overview of dynamic CMOS circuit synthesis is discussed in Sec. 2. The basic approach of dual-\(V_T\) assignment in dynamic CMOS circuits is presented in Sec. 3. Estimation models to calculate delay, switching power and leakage power dissipations in dual-\(V_T\) dynamic circuits are given in Sec. 4. Section 5 provides the implementation issues. Experimental results are given in Sec. 6.

2. Synthesis of Dynamic CMOS Circuits

A major limitation in the synthesis of dynamic domino/nora logic is that it implements only non-inverting logic. Hence complements of internal signals are to be realized through separate cones of logic using complements of the primary inputs, thus resulting in a significant area overhead. To overcome this limitation, several research works have been reported [4]-[6]. In [4], an approach to perform technology independent optimization and technology mapping for synthesizing dynamic CMOS circuits using domino cells has been proposed. The approach [4] assumes a circuit in multilevel decomposed form, converts the circuit into unate using standard Bubble Pushing algorithm and then optimizes the unate circuit using unate optimization procedure based on extraction/factoring, substitution, elimination and don’t care optimization. As a task of technology mapping, the approach follows the general tree-by-tree mapping approach [9], [10] and without using any standard cell library. The approach in [4] has been found to give good results in terms of delay and area. However, the said approach adopts computationally expensive Bubble Pushing algorithm and not applicable for large circuits. Another approach has been reported in [5] to synthesize dynamic domino circuits. This approach starts with an optimized circuit based on output phase assignment technique [11]. The optimized circuit is decomposed into a forest of trees to perform technology mapping. The approach [5] proposed on-the-fly domino cell mapping satisfying the width (number of transistors in parallel) and length (number of transistors in series) as it was done in [4]. Further, the approach [5] proposed multi-output domino cells and dynamic programming framework to reduced the total number of cells to be used. According to the reported results in [5], some circuits have area overhead; this is because of logic replications to obtain inverters logic as necessary.

In [6], [8] we have proposed a novel approach for synthesizing dynamic CMOS circuits using domino as well as nora logic gates. The approach is based on the two-level unate decomposition of logic functions. As this approach is adopted in this paper for dual-\(V_T\) assignment, it is briefly outlined in this section.

Two-level unate decomposition of a switching function \(f\) can be expressed as

\[
f = \sum P_i \cdot N_i
\]

where, \(P_i\) = is positive unate function (all literals are in non-complemented form) and \(N_i\) = is a negative unate function (all literals are in complemented form). The generic structures of dynamic CMOS circuits based on two-level decomposition with domino logic and nora logic are shown in Fig. 2(a) and Fig. 2(b), respectively. The keeper transistors are not shown for simplicity. Details of the algorithm to obtain two-level unate decomposition is given in details in [6], [8].

**Example 1.** Let us consider a Boolean function

\[
f_1 = \sum (3,5,7,8,11,12,14,15)
\]

\[\begin{align*}
(a) \quad \text{Domino CMOS circuit} \\
(b) \quad \text{Nora CMOS circuit}
\end{align*}\]

**Fig. 2** Dynamic CMOS circuits based on two-level unate decomposition
Following the algorithm in [6], the two-level unate decomposition of the function can be given as

\[ f_i = (x_1 + x_2 x_3 (x_4 + x_5)) + (x_2 x_1 + x_4 x_3) \cdot 1 \]

Two-level dynamic CMOS realization for functions of large number of variables using the unate decomposition approach as mentioned above may not be suitable for practical implementation, because of existence of a large number of transistors in series and parallel in gates. There is a constraint (to realize circuits of reasonable delay) on the length and width of a practical gate. By length we mean the maximum number of series transistors in a gate. When the number of transistors in series increases (this is the case when a product term consists of a large number of variables), on-resistance of gate increases and thereby affecting the delay of the gate. Increase in the number of transistors in parallel (width) proportionally increases (this is the case when a large number of product terms are there in the logic) the drain capacitance of a gate, which in turn increases the delay time as well as the dynamic power consumption. It is observed that the delay of a gate drastically increases when there are more than four transistors in series [4]. In order to reduce the delay, there should be at most 4 transistors in series. Similarly, we must restrict the number of transistors in parallel to five in order to check the delay as well as dynamic power consumption due to load capacitance [4]. To satisfy length and width constraints, we propose another decomposition step, where each node in the two-level decomposed circuit is further broken down into intermediate nodes till each node satisfy the length and width constraints. We term this decomposition as the cell-based multilevel decomposition [8]. To minimize the number of nodes, we first extract all kernels and perform kernel-based decomposition [10]. After the kernel-based decomposition is over, each node is examined whether it satisfies the length and width constraints or not. If the length and width constraints are not satisfied, then we carry out the cell-based multilevel decomposition. The cell-based multilevel decomposition is better illustrated with the example 2. In our approach, this cell-based multilevel decomposition accomplishes the task of technology mapping. It can be noted that, our technology mapping is not based on any library of standard gates; instead it does on the fly [4], [5] generation of cells satisfying length and width constraints.

3. Dual-V\textsubscript{T} Assignment

We propose the assignment of low threshold voltage (low-V\textsubscript{T}) and high threshold voltage (high-V\textsubscript{T}) to the transistors in dynamic logic gates in such a way that the delay remains same as in case of all low-V\textsubscript{T} design, but reduces subthreshold leakage current significantly. To understand our approach, it may be noted that unlike the static CMOS gates, dynamic gates exhibit fixed transition direction, that is, output remains at high (low) or move from high (low) to low (high) under the control of pull-down network of nMOSFETs (pull-up network of pMOSFETs). Moreover, the precharge time is relatively less than that of the evaluation time. The smaller precharge time can be exploited to reduce the subthreshold leakage current. Our basic approach is to assign low-V\textsubscript{T} to all transistors, which are likely to switch in the evaluation period and assign high-V\textsubscript{T} to all transistors, which may switch in the precharge period. The transistors, which are likely to switch in the precharge period are shown in shaded regions in Fig. 3 for the three types of dynamic gates. High-V\textsubscript{T} can be assigned to those transistors without affecting the performance. Remaining transistors switch in evaluation period and hence will be assigned with low-V\textsubscript{T}. With this assignment, the precharge time is increased, as high-V\textsubscript{T} devices perform the precharge operation and evaluation time remains unchanged, because low-V\textsubscript{T} devices perform evaluation operation. The increase in precharge time will not affect the performance, since only evaluation time is in the critical path.

With the dual-V\textsubscript{T} assignment proposed above, the leakage current is controlled in the following manner. In the precharge period the leakage current passes through low-V\textsubscript{T} transistors and in evaluation period, the leakage current passes through high-V\textsubscript{T} transistors or low-V\textsubscript{T} transistors depending on the output logic in the evaluation period. Moreover, when a circuit is in the standby mode, there should not be any loss of data due to leakage. This implies that the circuit should be in evaluation phase in the standby mode. This is accomplished by asserting clock signal at high level in standby mode. To avoid loss of data due to charge leakage, when a circuit stays in standby mode for longer duration, a keeper transistor is used at each output node to replenish the loss of charge due to leakage through the intrinsic capacitors.

4. Estimation Models

We have developed models to estimate delay and power dissipations in dynamic CMOS circuits realized in domino and nora logic styles. These models are discussed in the following subsections.

4.1 Delay Estimation

We propose RC-delay model to calculate the delay in a dynamic cell. For a dynamic domino circuit, the worst-case delay is the propagation delay due to the evaluation time in the cascaded pull-down networks (PDNs). The evaluation delay time for a PDN is decided by the discharge time of parasitic capacitances in the PDN. Figure 4 shows various parasitic capacitances in dynamic domino and nora cells. Let, \( n_i \) be the number of transistors in the longest chain in the network. The worst-case evaluation delay then in a PDN can be given as:

\[ t_{\text{pDNE}} = t_1 + t_2 + t_3 + t_4, \]

where \( t_1 = \text{discharge time of } C_L \text{ through the longest chain (Fig. 4(a))} \)

\[ 0.69(n_i R_n + R_d) C_L \]  \hspace{1cm} (1)

\[ t_2 = \text{discharge time of } C_P \text{ (Fig. 4(a))} \]

\[ 0.69 R_c C_P \]  \hspace{1cm} (2)

\[ t_3 = \text{discharge time of all internal capacitances} \]

\[ 0.69 \sum_{i=1}^{m} \sum_{j=1}^{n_i} (R_{x_i} + R_{n_i}) 2 C_{dh} \]  \hspace{1cm} (3)
Here, \( n_i \) is the number of transistors in the \( i \)-th chain and \( C_P = 2C_{dn} \)

\[
t_d = \text{delay in the buffer} = 0.69C_{inv}(R_p + R_n)/2
\]

(4)

In case of nora logic, \( t_d = 0 \), as there is no buffer in the PDN networks in nora logic.

The worst-case evaluation delay in a pull-up network (PUN) in a nora circuit is the time of charging the various capacitances in the network: 

\[
t_{PDN} = t_1 + t_2 + t_3
\]

(5)

where, \( t_1 = \) charging time of the capacitance \( C_L \) at output (Fig. 4(b))

\[
t_2 = 0.69(R_p + nR_p)C_L
\]

(6)

\[
t_3 = \text{charging time of internal node capacitances} = 0.69 \sum_{i=1}^{m} \sum_{j=1}^{n} (jR_p + R_n)2C_{dp}
\]

(7)

Here, \( C_p = (m+1)C_{dp} \)

Once the evaluation delay of each dynamic cell is known, the delay in any path can be calculated as the sum of evaluation delays of all dynamic cells in that path and delay of the circuit is the delay in the critical path.

4.2 Power Estimations

In dynamic CMOS circuits, major sources of power dissipations are the switching power due to transition of output from one level to another and leakage power due to subthreshold leakage current in ‘off’ transistors. Models for estimating these power dissipations are presented below.

**Switching power**

For a given dynamic cell there are several points where power dissipation occurs. Figure 5 shows a dynamic cell and various power consuming points in it. Here, \( P_1 = \text{power to charge and discharge capacitance} C_L \) at load, \( P_2 = \text{power to charge and discharge} C_p \), \( P_3 = \text{power to charge and discharge all internal capacitances} \), and \( P_4 = \text{power at inverter’s output} \), that is, at \( C_{inv} \).

**Switching power at \( C_L \)**

Switching power at \( C_L \) occurs due to charging and discharging the load capacitance \( C_L \) of a dynamic cell. The switching power at \( C_L \) with operating clock frequency \( f \) can be given as

\[
P_1 = E(X)C_LV_{DD}^2 \cdot f
\]

(8)

where, \( E(X) = \alpha_0 \cdot \alpha_1 \) is the transition probability at the output and \( \alpha_0 \) is the probability that the output is 0 and \( \alpha_1 \) is the probability that the output is 1. For a dynamic logic with PDN, the output will make a 0 to 1 transition in the precharge phase only if the output was discharged by the PDN in the evaluation phase. The transition probability for a PDN is therefore, \( E(X) = \alpha_0 \). Similarly, for a dynamic logic with PUN, the output will make a 1 to 0 transition in precharge phase only if the output was charged to 1 by the PUN in the evaluation phase. Hence, the transition probability for a PUN is \( E(X) = \alpha_i \).

**Switching power at \( C_p \)**

It may be noted that the capacitance at node 2 (Fig. 5) will be charged, if the PDN is ON. Hence, switching power dissipation at node 2 can be expressed as given below:

\[
P_2 = \alpha_i C_p V_{DD}^2 \cdot f
\]

(9)

However, in case of PUN, the switching power at \( C_p \) is given by

\[
P_2 = \alpha_0 C_p V_{DD}^2 \cdot f
\]

(10)

**Internal switching power**

There is a source of power consumption due to charging and discharging the internal node capacitances inside the logic cell. The total dynamic power consumed internally is:

\[
P_3 = \sum_{i=1}^{m} \sum_{j=1}^{n} \alpha_{ij} 2C_x \left[V_{DD} - V_{T x}\right] V_{DD} \cdot f
\]

(11)

where, \( V_{Tx} = V_{in} \) if the transistor is in p-network else it is \( V_{in} \), and \( \alpha_{ij} \) is the switching probability of the internal node \( x_{ij} \). \( C_x = C_{dp}(C_{dp}) \), if the network is PDN (PUN).

Switching power at static CMOS inverter node \( C_{inv} \) can be expressed as below:

\[
P_4 = \alpha_0 C_{inv} V_{DD}^2 \cdot f
\]

(12)

As the nora logic is inverter free, this component is not present in case of dynamic nora circuits.

**Leakage power**

When the circuit is in active mode, transistors though which subthreshold leakage currents flow in different dynamic cells are shown in Fig. 6. It is shown that in domino cell, subthreshold leakage currents flow through \( m_1 \) and \( m_3 \) in precharge period and in evaluation period through \( m_1 \) and \( m_3 \) and \( m_4 \), if the output logic is ‘1’, else through \( m_3 \) (Fig. 6(a)). In dynamic nora circuits, the subthreshold leakage current flows through \( m_3 \) in precharge period and through \( m_i \) in evaluation period depending on the output logic of the network (Fig. 6(b) and Fig. 6(c)). In addition to that, when the output logic is ‘0’ in case of domino gate, there is a leakage current in the PDN (Fig. 7) due to one or more stack(s) of off transistors. Similarly, there are leakage currents in PDN and PUN of nora gates if output logic is ‘1’ and ‘0’, respectively.

Expression for subthreshold leakage current can be obtained from BSIM3V3. Suppose, \( I_{sub}(m) \) denotes the
subthreshold leakage current through a transistor \( m \) when it is OFF. Suppose \( I_{\text{PDN}} \) (\( I_{\text{PUN}} \)) denotes the leakage current in the PDN (PUN). Then leakage current in precharge period \( I_{\text{pre leakage}} \) say, is given by:

In dynamic domino/nora cell

\[
I_{\text{pre leakage}} = I_{\text{sub}}(m)
\]  

Similarly, the leakage current in evaluation period, \( I_{\text{eval leakage}} \) is given by:

In dynamic domino cell

\[
I_{\text{eval leakage}} = \alpha_1(I_{\text{sub}}(m_1)+I_{\text{sub}}(m_2)+I_{\text{sub}}(m_3))+\alpha_0(I_{\text{sub}}(m_4)+I_{\text{PDN}}) \tag{13a}
\]

In dynamic nora cell with pull-down network of nMOSFETs

\[
I_{\text{eval leakage}} = \alpha_0 I_{\text{sub}}(m_1) + \alpha_1 \cdot I_{\text{PDN}} \tag{14b}
\]

In dynamic nora cell with pull-up network of pMOSFETs

\[
I_{\text{eval leakage}} = \alpha_1 I_{\text{sub}}(m_1) + \alpha_0 \cdot I_{\text{PUN}} \tag{14c}
\]

Now, the total leakage current is given by,

\[
I_{\text{leakage}} = 0.5(I_{\text{eval leakage}}+I_{\text{pre leakage}}) \tag{15}
\]

Leakage current in a PDN or PUN can be calculated considering the stacks of off transistors [13].

Equation 15 gives the leakage power dissipation in a dynamic cell when the circuit is in active mode of operation. When the circuit is in standby mode, leakage current that flows in a domino cell is same as in evaluation period, that is, \( I_{\text{leakage}} = I_{\text{eval leakage}} \).

Once the leakage current in each cell is known, the leakage power dissipation in a circuit can be obtained as

\[
I_{\text{leakage power}} = \sum I_{\text{leakage}} \cdot V_{DD} \tag{16}
\]

5. Implementation

We have implemented our algorithm on SUN Ultra Sparc 10 system and using C++ programming embedded with STL and GTL of ATT. The synthesis of dynamic CMOS circuits starts with partitioning an input circuit in BLIF format resulting smaller sub-circuits. Each sub-circuit is then transformed into PLA form (in terms of minterms) and disjoint decomposition is carried out to contain non-overlapping minterms only. After preprocessing the input, our tool decomposes a Boolean function into a set of positive and negative unate sub-functions based on the algorithm MUD [6]. It should be noted that, algorithm MUD can handle a single logic function at a time, whereas a circuit is in general multi-output in nature. This problem has been sorted out by extracting one function at a time from the stacks of off transistors [13]. During the multilevel decomposition, for the constraints of a cell, we have chosen \( \text{length} = 4 \) and \( \text{width} = 5 \). After this multilevel decomposition is over, our tool produces final netlist of synthesized circuit.

Values of transistor parameters are extracted using BSIM3V3 model and for 0.18µm technology as a particular instance. The effective channel length of the transistor is taken as 0.18µm and the gate oxide thickness is taken as 40Å. For simplicity, all transistors are assumed to have the same channel length of 0.18µm, while the channel widths for nMOSFETs and pMOSFETs are assumed to be 0.54µm and 1.62µm, respectively. The channel width for the keeper pMOSFET is assumed as 0.54µm. The subthreshold swing coefficient \( \gamma \) is taken as 1.44 and the body effect coefficients \( \eta \) and DIBL coefficients \( \delta \) are 0.03 and 0.21 for nMOSFETs and 0.02 and 0.11 for pMOSFETs, respectively.

For the calculation of power, the transition activity has been assumed to be 0.3 for all inputs. Although we have assumed that transition activity is 0.3, it can be as low as 0.1 in many situations, leading to smaller switching power requirement. For the active mode and standby mode of circuit, temperatures are assumed as 110°C and 25°C, respectively. The supply voltage is assumed 1.0V and zero biased low threshold voltage and high threshold voltage used in our experiments is 0.2V and 0.5V, respectively. It has been experimented that, threshold voltage increases by about 0.8mV for every 1°C decrease in temperature; hence threshold voltages in standby mode is about 68mV higher than the corresponding threshold voltages in the active mode.

6. Experimental Results

We have tested our approach with ISCAS benchmark circuits and experimental results are presented in Table 1 and Table 2. Energy requirements for the benchmark circuits based on domino logic are shown in Table 1. Delays of domino circuits are shown in Column 2 of Table 1. In Column 3 of Table 1, switching energy requirements of the circuits are given. Requirements of leakage energy in active mode of the operation of the circuits with single-V\(_T\) and dual-V\(_T\) realizations are shown in Column 4 and Column 5 of Table 1, respectively. In Column 7 and Column 8 of Table 1, requirements of leakage energy in standby mode of the operation are given for the circuits with single-V\(_T\) and dual-V\(_T\) realizations, respectively. Percentage reduction in leakage energy in dual-V\(_T\) dynamic domino circuits with respect to their single-V\(_T\) counterparts are shown in Column 6 and Column 9 of Table 1 in active mode and standby mode of the operations, respectively. It is observed that, on the average, in dual-V\(_T\) dynamic domino circuits 92% and 75% leakage power can be reduced in active mode and standby mode, respectively.
Energy requirements in dynamic nora circuits are shown in Table 2. Delay and switching energy requirement in dynamic nora circuits are presented in Column 2 and Column 3, respectively. Leakage energy requirement in single-VT and dual-VT dynamic nora circuits in active mode of the operation is given in Column 4 and Column 5 of Table 2, respectively. In standby mode of the circuits, requirement of leakage energy in single-VT and dual-VT realizations of dynamic nora circuits are presented in Column 7 and Column 8 of Table 2, respectively. Percentage reduction in leakage energy in dual-VT dynamic nora circuits with respect to single-VT realizations of the same in active mode and standby mode of the operations are shown in Column 6 and Column 9 of Table 2, respectively. It is observed that, dual-VT dynamic nora circuits require, on the average, 85% and 81% less leakage power compared to single-VT dynamic nora circuits in active and standby mode of operations, respectively.

### Table 1: Energy requirements for dynamic domino circuits

<table>
<thead>
<tr>
<th>Bench marks</th>
<th>Delay (ns)</th>
<th>Switching energy (fJ)</th>
<th>Leakage energy (fJ) in active mode</th>
<th>Leakage energy (fJ) in standby mode</th>
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<td>C432</td>
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### Table 2: Energy requirements for dynamic nora circuits

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### Conclusion

In this paper we have proposed an algorithm for the synthesis of dual-VT dynamic domino and nora circuits. The synthesis of dynamic domino and nora circuits is based on two-level unate decomposition. Low and high threshold voltages are assigned to the transistors in such a way that the performance of the circuits remain same as in case of all low-VT design, but leakage power dissipation is reduced significantly. Experimental results show that the percentage reductions in leakage energy in dual-VT dynamic domino and nora circuits are, on the average, 92% and 85% respectively, in the active mode and 75% and 81% respectively, in the standby mode. Our approach is therefore found to be very effective for battery-operated hand held portable systems, where battery life is of prime importance and it is very effective in reducing leakage power in active and standby modes.

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### Reference