# 0.1 μm InP HEMT MMIC Fabrication on 100 mm Wafers for Low Cost, High Performance Millimeter-Wave Applications

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**Abstract**

**Northrop Grumman Space Technology (NGST) has recently initiated process development for fabricating 0.1 μm InGaAs/InAlAs/InP High Electron Mobility Transistor (HEMT) MMICs on 100 mm InP substrates. Successful development of this process will further reduce costs for InP HEMT MMICs and rival those of GaAs-based HEMT MMICs, including GaAs-based metamorphic HEMT technology, with superior performance. Production capability has been demonstrated in three core areas: epitaxial material growth using Molecular Beam Epitaxy (MBE), frontside processing in NGST's 100 mm MMIC production line, and backside processing in NGST's 100 mm backside production line with final wafer thickness of 75 μm. In this paper, we will present recent data and progress on NGST's 0.1 μm InP HEMT MMIC LNA process on 100 mm InP substrates.**

## INTRODUCTION

InP-based High Electron Mobility Transistor (HEMT) MMIC technology is leveraging for future high volume, low cost, high performance millimeter-wave applications. Cutoff frequencies $f_t$ as high as 400 GHz have been demonstrated with InP-based HEMT devices [1-2]. Applications requiring operating frequencies up to 200 GHz and beyond include wireless and optical communications, passive imaging, and atmospheric sounding for next-generation weather satellites [3]. The inherent properties of the InGaAs/InAlAs/InP material system provide high electron mobility, high saturation velocity, and high sheet carrier density. These material properties allows for achievement of superior high frequency and low noise performance from HEMT devices [2]. For the past 15 years, NGST has been developing InP HEMT technology for space, military and commercial applications. NGST's high reliability 0.1 μm InGaAs/InAlAs HEMT MMIC technology on 75 mm InP substrates is flight qualified and has been inserted into several millimeter-wave flight communications and sensor applications [4-5]. A key in expanding the usage of InP HEMT MMICs is lower fabrication costs through larger diameter InP substrates and enhancements to the production process for higher circuit yield and performance. NGST's process development for 100 mm InP HEMT MMICs was accomplished in NGST's 100 mm MMIC manufacturing line, which also produces the 100 mm GaAs HBT, InP HBT, and GaAs HEMT MMIC technologies.

## FABRICATION PROCESS

### *Epitaxial Material Growth*

The InP HEMT epitaxial layer structures shown in Figure 1 were grown on 100 mm semi-insulating InP substrates by molecular beam epitaxy (MBE) at NGST. The InP HEMT layer is single-side delta-doped and includes a 60% indium channel. Room temperature Hall measurements typically show mobility of 10,000 $cm^2/Vs$ and channel electron carrier density of $3.5x10^{12}$ $cm^{-2}$.

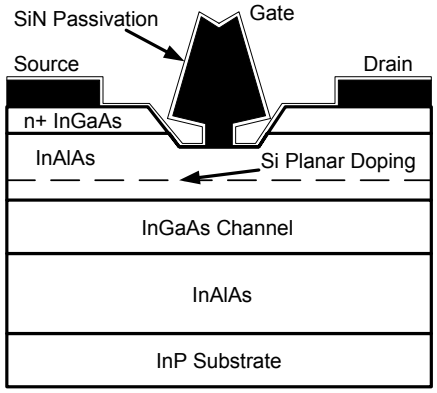



Figure 1. Cross-section diagram of an InGaAs/InAlAs/InP HEMT for low noise amplifier applications.

The MBE growth of 100 mm InP HEMT wafers takes advantage of the scalability property in the MBE process. These wafers can be produced on multi-wafer MBE systems, on both 3x4-inch platform and 7x4-inch platforms. Shown in Figure 2 is a plot of the resistivity for the 3x4-inch platform, showing excellent uniformity of 1%. These wafers

share all of the advantages found for GaAs growth on multi-wafer platforms: lower defect levels, improved crystal quality due to superior vacuum, and reduced wafer-to-wafer variability. The MBE growth of HEMT structures on InP also is a high throughput process that does not require the long growth times involved in metamorphic buffer growth on GaAs substrates. Consequently, the epitaxial cost of the two approaches is comparable. The growth on InP is free of the cross-hatch surface morphology found in the metamorphic buffer growth approach, which will offer inherent advantages as gate length is decreased.

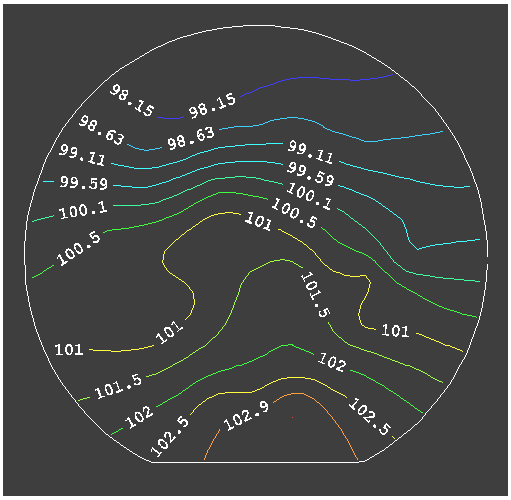



Figure 2. Resistivity plot for the 3 x 4-inch platform, showing excellent uniformity of 1%.

*Frontside Fabrication Process*

The frontside process development includes several enhancements over the 75 mm process. Examples of these enhancements include; (a) Flexibility for fabricating MIM capacitors other than our standard 300 pF/mm$^2$ capacitors, (b) increased throughput in the electron beam lithography process on 100 mm wafers, and (c) a methodology for a flexible multiple-layer stepper reticle to reduce NRE costs by more than 40% for process development, production qualification, and commercial production. The 100 mm InP HEMT process was designed to take advantage of the maturity of the processes developed for GaAs and InP HBT and GaAs HEMT MMIC fabrication in NGST's 100 mm flexible manufacturing line. Greater than 80% of the InP HEMT process is shared with our 100 mm GaAs HEMT process and 60% is shared with our 100 mm HBT process. This minimizes the number of processes that need to be maintained, further reducing cost.

All lithography levels are defined with I-line technology with the exception of the 0.1 μm T-gate process which is defined by electron beam lithography using a bi-layer (PMMA, P(MMA-MAA)) process. The EBL exposure process takes advantage of the tight registration control of the I-line stepper to minimize the number of EBL alignment sites. An ammonia-based image reversal process has been developed for metal lift-off steps in the 100 mm line. The image reversal process has been optimized to allow sub-micron metal features and 2 μm line and space pitch. Tight CD control of the metal lift-off lithography process has been achieved with 0.5% CD uniformity across a wafer and within 0.8% uniformity across a twenty five-wafer lot.

The frontside process retains key features of our GaAs and InP HEMT MMIC 75 mm processes including a baseline 60% InGaAs channel HEMT structure (InP HEMT), PECVD silicon nitride passivation, 300 pF/mm$^2$ MIM capacitors, 100 Ω/sq NiCr thin film resistors, and two levels of metal interconnect with the second level having air bridges. The burnout voltage of the MIM capacitors is greater than 100 volts. The ohmic contact resistance of the source and drain contacts is typically 0.13 Ωmm.

The frontside fabrication process flow is shown in Figure 3. In the 100mm InP HEMT process, fabrication of the MIM capacitor is started at the beginning of the MMIC process prior to the completion of the HEMT device using a double-layer nitride process. In addition, the feed pads to the gate fingers are optically printed by I-line exposure. This differs from our 75 mm process, where both the gate fingers and pads are exposed by electron beam lithography. This enhancement allows the EBL system to expose a 100 mm wafer in approximately the same amount of time as for a 75 mm wafer. Our process also offers 100 nm silicon nitride passivation of the T-gate HEMT devices. Figure 4 shows an end view SEM photograph of the InP HEMT 0.1 μm $\pm$ 0.005 μm T-gate. The gate recess was controlled by a wet-etch process.

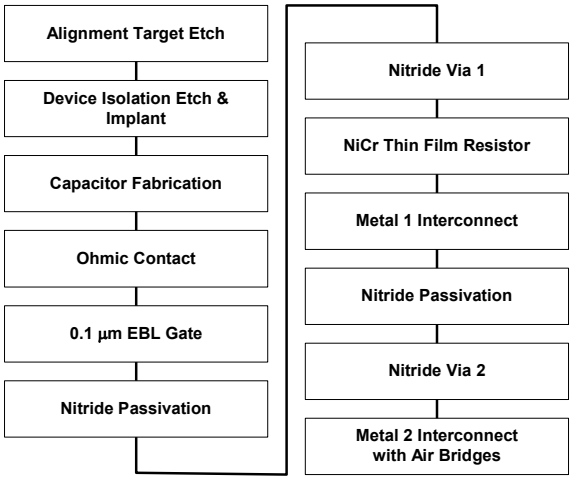
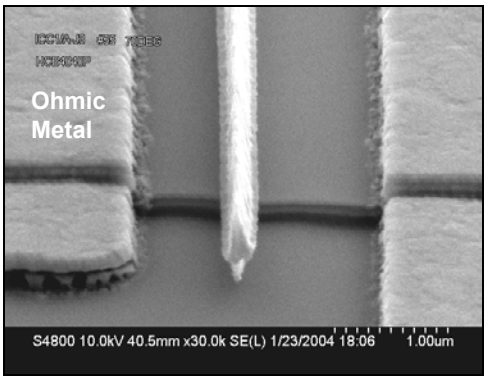
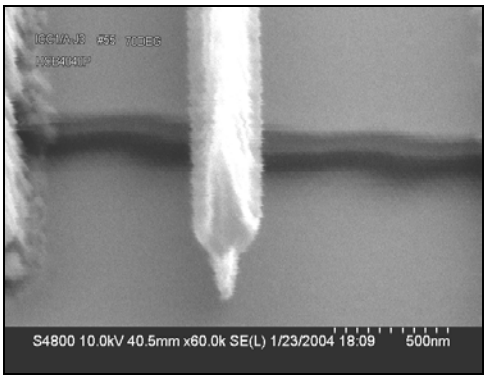



Figure 3. 100 mm 0.1μm InP HEMT Frontside fabrication process flow diagram.




(a)




(b)

Figure 4. End view SEM of the InP 0.1 µm T-gate on 100 mm wafer. (a) 30KX magnification. (b) 60KX magnification.

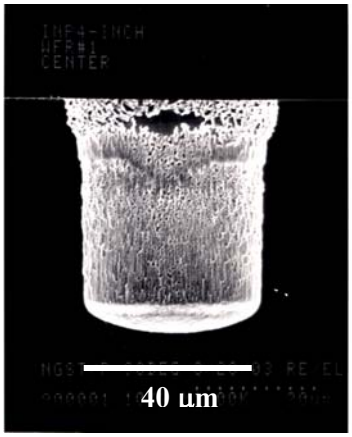



Figure 5. SEM cross-section of the InP backside through via.

*Backside Fabrication Process*

In the backside process, the 100 mm InP substrates are bonded to 109 mm sapphire substrates. The wafers are thinned to a final thickness of 75 µm (3-mil) using mechanical grinding. An RIE system is used to dry etch the backside through-substrate vias (See Figure 5) using a hydrogen bromide based gas mixture. The through vias connect the backside metal ground plane to the frontside device and circuit elements. The RIE system has the capability to etch three 100 mm wafers at a time and is completely automated with cassette-to-cassette wafer handling. The etch uniformity is within ± 3% across a three wafer batch. The RIE throughput is approximately 48 wafers/day with 100% via yield. The thinned substrates are demounted for chip dicing. Both the bonding and demount operations have been optimized to allow successful, residue free demounts in 2 hours.

## DEVICE PERFORMANCE

*DC Characteristics*

Device and passive element parameters are monitored at several in-process steps. Figure 6 shows the wafer average DC device parameters of $G_{mp}$ (Peak transconductance), $I_{max}$ (Drain current measured at $V_g$ = 0.4 V), and $V_{gp}$ (Gate voltage at $G_{mp}$) measured at 1 V drain bias for eighteen 100 mm InP HEMT wafers fabricated over seven wafer lots. The wafer average is based upon a minimum of thirty sites measured across each 100 mm wafer. The measurements were made on devices with 80 µm periphery at the post nitride via 1 step.

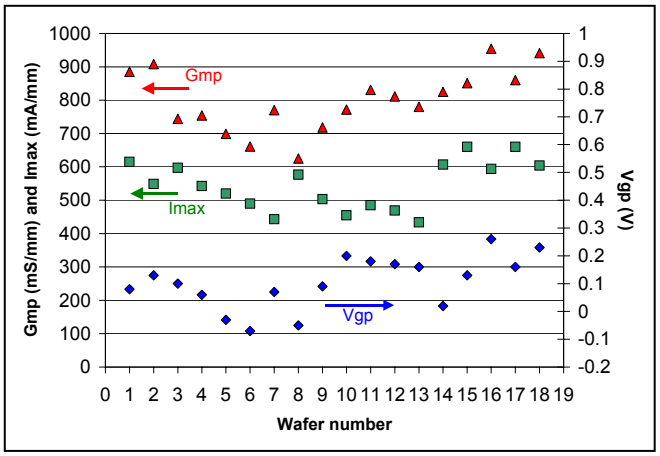



Figure 6. Wafer average DC device parameters of $G_{mp}$, $I_{max}$, and $V_{gp}$ for eighteen 100 mm InP HEMT wafers. Devices have 0.1 µm gate length and 80 µm periphery.

From the data in Figure 6, the wafer average $G_{mp}$ is 800 mS/mm, the wafer average $I_{max}$ is 545 mA/mm, and the wafer average $V_{gp}$ is 0.1 V. The higher $G_{mp}$ for recent wafers (Wafers 11-18 in Figure 6) is credited to improved gate length and recess width control, and to reduced ohmic contact resistance. Within an individual wafer, the typical sigma for $G_{mp}$, $I_{max}$, and $V_{gp}$ is 66 mS/mm, 41 mA/mm, and 0.06 V, respectively. DC device functional yield is typically greater than 95%. Device $f_t$ is in excess of 190 GHz.

*RF Characteristics*

An example of MMIC performance on 100 mm InP substrates is shown in Figure 7 for a 2-stage balanced Ka-band LNA. This Ka-band LNA has noise figure less than 2.4 dB and with greater than 17 dB associated gain over the frequency band 27-39 GHz. This performance is comparable to that achieved on the 75 mm InP HEMT process line at NGST [5]. RF yield across the 100 mm wafer based on a 3 dB noise figure spec at 33 GHz was as high as 72% with 495 out of 684 sites passing. The standard deviation of noise figure and gain at 33 GHz across a wafer was 0.26 dB and 0.84 dB, respectively. A micrograph of the 20-stage Ka-band LNA is shown in Figure 8.

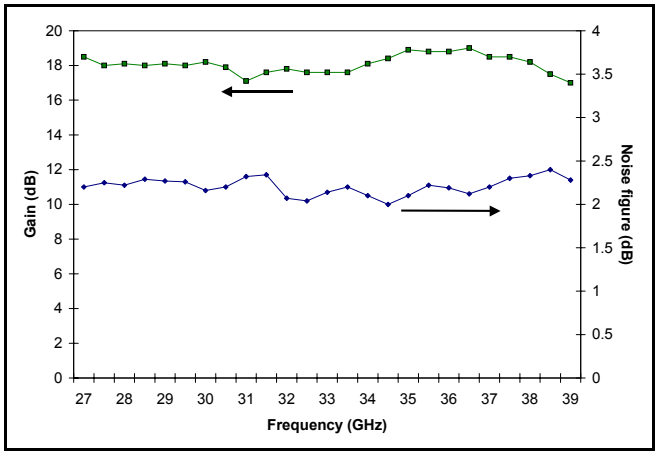



Figure 7. Noise figure and associated gain of a 0.1 µm InP HEMT Ka-band 2-stage balanced LNA fabricated on 100 mm InP substrate.

## CONCLUSIONS

We have successfully developed processes for fabricating 0.1 µm InGaAs/InAlAs/InP HEMT MMICs on 100 mm InP substrates. Manufacturability of InP HEMT MMICs has been demonstrated in three core areas: MBE epitaxial material growth and in both frontside and backside processing. Good DC and RF electrical performance have been obtained with average $G_{mp}$ of 800 mS/mm and $f_t$ greater than 190 GHz and with acceptable yield. Additional characterization of the InP HEMT devices and W-band MMICs are on-going. The scaling to 100 mm InP substrates and shared processes with the HBT and GaAs HEMT technologies results in lower fabrication costs. Further process optimization will enhance the robustness of the 100 mm InP HEMT MMICs. These factors will enable wider acceptance of InP HEMT technology for next generation applications.


## ACKNOWLEDGEMENTS

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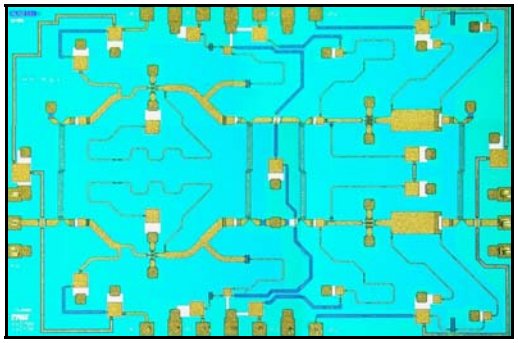

Figure 8. Micrograph of a Ka-band 2-staged balanced MMIC LNA operating over 27-39 GHz fabricated by 0.1 µm InP HEMT technology on 100 mm InP substrate.

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## ACRONYMS

HEMT: High Electron Mobility Transistor
LNA: Low Noise Amplifier
MBE: Molecular Beam Epitaxy
MMIC: Monolithic Microwave Integrated Circuit
MIMCAP: Metal-Insulator-Metal Capacitor
NRE: Non-Recurring Engineering
RIE: Reactive Ion Etch