Evolvable Hardware

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Harnessing all of the intrinsic data-processing power of electronic devices is impossible through traditional circuit design. While complex physical processes involving electronic, thermal, and quantum phenomena underlie the operation of the devices, standard circuit design methodology appropriately mandates a level of abstraction in which most of these phenomena are safely ignored. In this work, we investigate the possibility that enhanced data processing capabilities exist in previously neglected classical degrees of freedom of a circuit [1].

Design that explicitly incorporates the full phase space of electronic devices into the standard design methodology is fraught with problems: noise, fabrication margins, and poorly understood interactions between the various physical degrees of freedom of the system, which conspire to make a conventional approach difficult. Our approach, instead, uses reconfigurable hardware in conjunction with a genetic algorithm (GA) to search for an optimal circuit configuration based on performance evaluated in hardware. In this approach, many of the limitations of traditional design are removed because the algorithm search is based on the input-output performance and can use all degrees of freedom in the system. Our specific goal is to test these ideas by generating an analog-to-digital converter, using hardware evolution of a reconfigurable circuit controlled by a GA.

The reconfigurable circuit consists of "Totally-Reconfigurable Analog Circuit" chips from Zetex, interfaced with passive circuit elements and each other through switch arrays. Our use of switch arrays in this way departs from past work [2] and provides a way to scale the device to much larger levels of complexity. We have demonstrated the operation of our system by realizing an evolved frequency doubler on a stand-alone TRAC. We are currently working on incorporating switch arrays and digitally programmable passive elements into the system to exploit the larger phase space of the complete reconfigurable circuit.

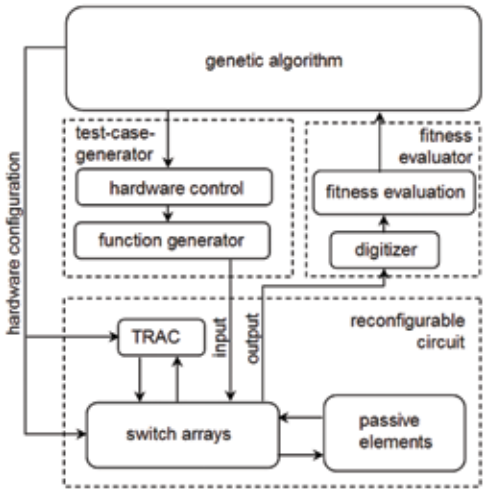

Figure 1: System representation for automated circuit design using an evolvable hardware approach. TRAC and switch configurations are generated by the genetic algorithm. These configurations are then tested using a sequence of test cases, and a fitness is assigned to each particular configuration. The fitness is used to select appropriate configurations for ensuing generations of the algorithm.

REFERENCES:

[1] Thompson, A., "An Evolved Circuit, Intrinsic in Silicon, Entwined with Physics," in T. Higuch, M. Iwata, W. Liu (eds.) *Proc. Of the 1st Int. Conf. on Evoltable Systems: from Biology to Hardware,* LNCS, vol. 1259, Springer-Verlag, pp. 390-405, 1997.

[2] Ozsvald, I., "Short-Circuiting The Design Process: Evolutionary Algorithms for Circuit Design Using Reconfigurable Analogue Hardware," Masters Thesis, University of Sussex, 1998.