Modeling, Measurement and Mitigation of Crosstalk Noise Coupling in 3D-ICs

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Abstract—Faraday cages have traditionally been used to provide isolation from electromagnetic fields. In this paper, we describe the use of Faraday cages for reducing crosstalk in 3D ICs. We validate our methodology with a combination of simulation and measurements from fabricated prototype designs. Measurement and simulation results show that the crosstalk between the transmitter and receiver reduces by about 75dB up to 10GHz by using a Faraday cage in combination with tier-to-tier isolation, which is one of best performance reported so far. We further develop a lumped equivalent model for crosstalk with and without a Faraday cage. There is good agreement between measurement, 3D electromagnetic simulation and lumped circuit simulation.

I. INTRODUCTION

3D ICs provide an attractive alternative to traditional two dimensional integrated circuits (2D ICs). In the case of homogeneous integration (i.e., same technology), they provide increased computational power with reduced wiring and additionally, provide the possibility of heterogeneous integration (i.e., different technologies) that may be more suitable for RF and mixed-signal circuits. In this paper we focus on mixed-signal (RF/analog/digital) design in CMOS 3D ICs. Such 3D ICs allow for the integration of full systems that include RF circuits with significant digital signal processing capability. However, for such integration to be feasible it is critical to provide sufficient isolation between the sensitive analog/RF circuits and the digital circuits. Noise injected by digital circuits into the substrate can severely degrade the performance of RF/analog circuits.

Over the years, in 2D planar ICs a number of techniques for reducing crosstalk via the substrate has been developed. Guard rings around a noise source provide a low resistance path to AC ground and minimize the amount of noise injected into the substrate. Well-designed guard rings can suppress the amount of coupling at frequencies below 1GHz, but have proven to be quite ineffective above 3GHz [1]. Deep trench technologies have shown isolation that is better than 40dB for 0.5-20GHz, but result in fairly complex processes [2]. Patterned ground shields under inductors improves isolation for RF circuits by an additional 25dB [3]. Other noise isolation technologies that perform well at frequencies below 1GHz, include triple well, on-chip decoupling and buried oxide. The isolation frequency performance can be increased to approximated 10GHz by using SOI technology with a high resistivity substrate [4].

In this paper, we present and verify noise isolation in 3D ICs by using separate tiers and Faraday cages (FC). The design and implementation are based on a 0.18 µm fully-depleted silicon-on-insulator (FDSOI) technology shown in Fig. 1 [5], [6]. The three active tiers, with three metal layers each, are first individually fabricated using a FDSOI CMOS process. The resistivity of each tier is about 2000 Ohms-cm. The handling wafers of the top two tiers are then removed and these tiers are flipped over and integrated with the bottom tier by using intertier vias. Faraday cages have traditionally been used to block-out external EM fields. We evaluate the efficacy of using such cages in 3D ICs. It is critical to note that Faraday cages are not possible in traditional 2D ICs because metal layers are only available above the active devices. In the MITLL 3D IC technology FCs can be created by using metal layers in any two tiers and using the inter-tier vias to complete the sides of the Faraday cage.

The paper is organized as follows. In Section II we describe the test chip and the experimental and simulation setup for the different coupling conditions in detail. Section III provides measurement and simulation results. Section IV presents a lumped model of the coupling effects based on physical parameters, simulations and calculations. Section V provides some concluding remarks.

II. EXPERIMENTAL & SIMULATION SETUP

3D ICs allow for significant digital signal processing to be available in close proximity to analog/RF circuits which is of great interest for future programmable and cognitive radios. However, the close proximity also introduces the potential problem of noise coupling. In the next subsections we explore an experimental setup that confirms the coupling problem and also identify techniques that are valuable for their mitigation.

A. Experimental Setup

Fig. 2 shows the microphotograph for a 5mm × 2.5mm test chip that was used to investigate noise coupling in 3D ICs. Test structures without Faraday cages on tier 3, displayed in Fig. 2...
RESULTS AND DISCUSSIONS

Fig. 2: Micrograph of test die (a) test structures without Faraday cage on tier 3 (b) test structures with Faraday cage on tier 3 (c) de-embedding structures

(a), are used as a reference for test structures with Faraday cages on the same tier. The transmitter (TX) and receiver (RX) sections in this experiment use identical inductors. The transmitter consisted of four inductors at different distances from the receiver. The distances between transmitter inductor centers and receiver inductor centers are 710µm, 510µm, 435µm and 430µm. The thickness of metal layers 1-3 on the tier 3 are all 630nm. All inductors are based on a square spiral structure where metal 3 is used to form the coil and metal 2 is used for the underpass. Inductors for test structures in Fig. 2 (a) have 3.25 turns with an inner diameter of 88µm, and the width and the spacing of the spiral are 10µm and 4µm respectively. The inductors are configured as a one-port device with the other port connected to ground. The ground ring serves as a current return path, and is at a fixed distance of 100µm away from the outer diameter of the inductor.

The test structures with Faraday cages (FC) on tier 3 are shown in Fig. 2 (b). The test structures for the TX and RX are identical except for the Faraday cage. The two set of structures, with and without Faraday cage, are on opposite sides of the chip. We ensure that the distance between the TX center and RX center remained unchanged with and without the FC. For this experiment, the FC consists of the back metal ($BM_1$) on tier 3, the back metal ($BM_1$) on tier 2 and intertier vias between tier 3 and tier 2. It is important to note that creating this FC does not involve any additional fabrication steps. The two different kinds of Faraday cages are shown in Fig. 3.

For our experiment, we use the measured $S_{21}$ as the figure of merit for isolation. Measurements were done from 50MHz to 10GHz with the help of an Agilent 8719Es two-port network analyzer for the test structures shown in Figs 2(a) and 2(b). The network analyzer is configured to perform broadband measurements. Probe calibration was done using CASCADE’s 101-190 substrate using a Short-Open-Load-Thru technique. De-embedding structures shown in Fig. 2(c) were used to eliminate the influence of the transition region between the probe, probe contact and the device under test.

B. Electromagnetic Simulation Methodology

Not all test cases could be verified via the test setup above. Therefore, to complete the picture we supplement the measurements from the experimental setup with full-wave electromagnetic (EM) simulations. EM simulations were validated via measurements and will be used to guide future isolation structure design. Ansoft HFSS was used for our EM simulations [7].

The solid model used within HFSS for the FDSOI CMOS 3D IC is shown in Fig. 4. The details of the structures used to simulate noise coupling correspond to the test structures shown in Fig. 2 (a) and (b). Two other simulation structures are also discussed; one is that of test inductors on the different tiers (tier 3 and tier 2) with/without Faraday cages; another one is the same structure as shown in Fig. 2 (b) except that the Faraday cage uses patterned top and bottom plates. All inductor design parameters are exactly the same as those shown in Fig. 2(a) and (b).

III. RESULTS AND DISCUSSIONS

Fig. 5 shows measured and simulation results for the reference structures in Fig. 2 (a). The graph plots the measured $S_{21}$ with the probes in the air and measured and simulated values of $S_{21}$ at different separations between the two structures. The separation between the structures is varied from 430µm to 710µm. We note a good matching between measurement and simulations. Additionally, we note that increasing the distance between TX and RX by about 200µm reduces the crosstalk only 5dB at 1GHz. Clearly, distance alone is not the solution.

Fig. 6 shows the measurement and simulation results for the structures in Fig. 2 (b). We note that that magnitude of crosstalk is much lower (on average 30dB) than shown in Fig. 5. However, these results include the effects of the metal connection between the inductors and the pads that were used for testing purposes but were outside the Faraday cages, which unfortunately also contribute to crosstalk. In fact, the metal connection outside the Faraday cage is the primary contributor to the increase in crosstalk with frequency. Unfortunately, it is not possible to make measurements without these interconnections. We note that there is a good agreement with measurement and simulations at higher frequencies. The discrepancy at lower frequencies (below 2.5GHz) can be attributed to the crosstalk between the probes in the air. We also note that, unlike the results in Fig. 5, spacing between the structures has very limited impact on the crosstalk.
As we are unable to eliminate the connection to the outside for our FC measurements and we have validated the close agreement between measurement and simulation results, we can now use HFSS as a tool to show the real impact of these cages. Fig. 7 shows the simulation results for inductors that are similar to the ones shown in Fig. 2(b) but are completely enclosed within a Faraday cage. In comparison to the measurement results shown in Fig. 5 the crosstalk is reduced by an additional 100dB, which is the highest value ever reported. The slight increase in crosstalk with frequency is due to a combination of numerical precision and port to port coupling during simulations.

A solid Faraday cage provides excellent isolation, however, the image current induced by the magnetic field in the solid surface of the Faraday cage flows in opposite direction and will reduce the total inductance and Q (i.e., Eddy current effect). Orthogonally slotting the top and bottom plates can be used to eliminate this effect without reducing the isolation properties [3]. The slots, which should be smaller than the operation wavelength, act as an open circuit to the induced current. To evaluate this property we pattern the top and bottom of the Faraday cage, Fig. 9(a) shows a simplified equivalent circuit used for modeling each single spiral inductor [12]. The spiral inductor structure is represented by an inductance $L_s$, a series resistance $R_s$, the coupling capacitance $C_p$ and resistance $R_c$. The parallel parasitics result from a combination of oxide capacitance $C_{ox eff}$, representing the capacitance value of the oxide layer in each tier between the inductor and the top of silicon substrate. The substrate parasitics are represented by $R_{sub}$ and $C_{sub}$. The value of each of the elements in the equivalent circuit is optimized to match the measured results. As seen in Fig. 9(b) there is there is extremely good matching between measured and modeled parameters.

To evaluate the coupling effects between two inductors with/without Faraday cages, a simple lumped element equivalent circuit is shown in Fig. 10. This noise coupling effect (crosstalk) is modeled by an RC path ($R_{cp}/C_{cp}$). Expressions of equivalent elements $R_{cp}$ and $C_{cp}$ have been derived for...
Fig. 9: (a) Equivalent circuit model for inductors from Fig 2; (b) Modeled data (dotted line) and measurement data (solid line) from 1GHz to 10GHz.

![inductor diagram]

Fig. 10: The lumped equivalent circuit for the crosstalk between two inductors without Faraday cage in [9], [13], [14] and are included here for completeness.

\[ R_{cp} = \left[ K_1 \frac{\pi \varepsilon_0 \sigma_{si} W}{4 \ln (\frac{\pi (d-W)}{t})} + 1 \right]^{-1} \]  
\[ C_{cp} = \left[ K_1 \frac{\pi \varepsilon_0 (\varepsilon_{si} + 1)}{4 \ln (\frac{\pi (d-W)}{t})} + 1 \right] W \]  

Here \( K_1 \) is the fringing factor. For our test structures without a Faraday cage \( K_1 \) is equal to 1.37 for \( d = 430 \mu m \).

V. CONCLUSIONS

In this paper, we model and measure noise coupling in 3D ICs. We also develop a new technology for reducing this

Fig. 11: Lumped circuit simulation results for different structures (\( d = 430 \mu m \)). Good agreement between lumped circuit simulation data, measured data and HFSS simulation data. The dotted line is lumped circuit simulation data crosstalk. To validate our model and our design techniques we used a combination of simulation and measurement results from inductors (implemented on different tiers) with and without Faraday cages. We use the structure without a Faraday cage as our reference. Measurement and simulation results show that isolating either the TX or RX alone reduces the noise coupling by 75dB. However, enclosing both the TX and RX in Faraday cages reduces the noise coupling by an additional 25dB. We also developed and verified a simplified lumped equivalent circuit model for noise coupling. In 3D ICs the use of Faraday cages, combined with placing the RF/analog circuits and digital circuits on separate tiers, results in extremely good noise isolation. This allows us to fully integrate system that have both sensitive analog/RF circuits and require significant digital signal processing. Additionally, it is well known that noise isolation decreases at higher frequencies, therefore 3D ICs using Faraday cages may be the preferred process technology for high performance mixed-signal systems in the future.

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REFERENCES