1. Introduction

The layout patterning of standard-cell-based ASICs is carried out by the photo-lithography using the photo-mask. Resolution enhancement technologies such as OPC (Optical Proximity effect Correction), are widely used for the patterning of sub-quarter-micron rule LSIs. The photo-mask cost has been dramatically increased due to the complex figure layout after the OPC. From these reasons, it has been hard to make low-volume production LSIs at low cost. Therefore, we think that another production method must be established for low-volume production LSIs.

An FPGA (Field Programmable Gate Array) which can be electrically customized after manufacturing is a popular solution. However, the unit cost of an FPGA is relatively high, because FPGAs are inferior to standard cell-based ASICs in area, speed and power consumption. It was reported that the speed performance and the power-consumption of FPGAs are 3.2–4.3 times and 12 times larger than that of ASICs respectively, in 90-nm CMOS circuit design [1]. The chip area of FPGAs is also reported to be 40 times larger than that of ASICs. These results suggest that the FPGAs cannot be applied to the battery-operated mobile system, because of its high power consumption.

Recently, various mask programmable devices such as structured ASICs are proposed as other solutions for the mask cost problem [2], [3]. The number of photo-mask layers for logic-programming should be reduced in order to decrease the mask cost. Some via-programmable devices have been proposed for this purpose.

The via-programmable logic device “eASIC” [4] is commercially available, however, “SRAM” programmable LUT (Look Up Table) is used as a logic element. Therefore, the chip-area and the dynamic-power of eASIC will be considerably larger than that of standard ASICs. “Mask” programmable logic elements have been studied in VPGA (Via Programmable Gate Array) [5], and VCC (Via Configurable Cell) [6], [7]. Mask programmable LUT and gate-array structure are used as logic elements in these devices.

In this paper, we will propose a novel via-programmable logic device VPEX (Via Programmable logic device using Exclusive-or array), whose logic element consists of complex-gate type Exclusive-OR (EXOR) and Inverter (NOT). The logic element of VPEX has the advantage in area, speed, and power-consumption, compared to other logic elements such as LUT or SOP (Sum-Of-Product). Furthermore, it is outstanding point of VPEX that a D-FlipFlop can be composed of 5 logic elements. In addition, the layout of via-layer is optimized in order to decrease EB direct writing time.

This paper is organized as follows. In Sect. 2, we introduce the electron beam (EB) direct writing technique. The logic element (LE) of VPEX and the D-FlipFlop composed of 5 LEs are discussed in Sects. 3 and 4. The routing architecture of VPEX and the experimental routing program are shown in Sect. 5. After introducing the circuit performance using VPEX in Sect. 6, we will summarize and conclude this study in Sect. 7.

2. EB Direct Writing Technique

In this section, we discuss about the cost and the throughput of Electron Beam (EB) direct writing. And we also explain reason why we select “via” layer as a programming layer.
2.1 The Chip Cost Using EB Direct Writing

Firstly, we discuss about the chip cost using EB direct writing compared to photo-lithography. In general, the chip cost using photo-lithography is prohibitively expensive in a low-volume production due to the initial photo-mask cost. Figure 1 shows the lithography cost using ArF photolithography and EB direct writing in Ref. [8]. While the cost of photo-lithography decreases with increasing chip production volume, the cost of EB direct writing is constant. Therefore the EB direct writing cost is relatively lower than the photo-lithography cost in low-volume production LSIs. For example, if the EB throughput is more than 3 wafers/hour, we should use EB direct writing for the chip whose production volume is less than \( \sim 500 \) K unit.

2.2 Throughput of EB Direct Writing

The lithography cost of EB direct writing is strongly dependent on the EB throughput. The EB writing time \( T \) per 1 wafer is estimated in the following equation.

\[
T = N_s \times (T_s + T_e) + T_o
\]

In this equation, \( N_s \) is a "EB shot" number for 1 wafer. "EB shot" means the number of writing figures. If the original figure in the EB data is larger than maximum EB shot size, the figure is divided into multiple "EB shot." The typical maximum shot size is 5 \( \mu \)m square. \( T_s \) is a settling time for each EB shot, \( T_e \) is an exposure time, and \( T_o \) is an overhead time such as wafer-loading or chip-alignment. \( T_s \) and \( T_o \) are defined by the specification of EB writing machine, and \( T_e \) is defined by resist sensitivity and EB current density. We will decrease shot number \( N_s \) in order to decrease EB writing time \( T \). We can greatly decrease \( N_s \), by applying "character projection (CP)" lithography [8]. In this method, multiple figures within the 5 \( \mu \)m square can be delineated by single EB shot like a "stamp." The "stamp" is called as "CP mask," and the number of "CP mask" is limited by the specification of EB machine. There are some studies [9]–[11] in which the standard cells should be delineated by "CP mask" in order to get high throughput by EB direct writing.

2.3 Via Patterning Using EB Direct Writing

The important point in lithography is the patterning resolution. In the EB direct writing, the resolution is degraded by the large pattern-area-density, which is defined as the area density within \( \sim 10 \mu \)m square, due to the EB proximity-effect and the coulomb-interaction. That is to say, the hole patterns such as contact or via layer have better resolution than the line patterns like metals. Hole patterns are also advantageous in stitching accuracy as shown in Fig. 2. Long figures such as metal wiring have to be stitched at every maximum EB shot size. The patterns at the stitching boundary tend to be degraded due to the stitching error. On the other hand, there is no stitching for hole layers because every figure is isolated.

The shot number \( N_s \) is also important point. According to our study, the number of figures in contact layer is about 10 times as much as in via layer for the typical layout data. Therefore, we select "via" layer as a programmable layer in order to get higher resolution and throughput.

3. Logic Element of VPEX

3.1 The Structure of Logic Element (LE)

In this section, we will explain the detail of logic element used in VPEX architecture. Figure 3 shows the cross-sectional structure of VPEX. The logic function of each LE is programmed by via-1 layer. The main routing layers are metal-3 and metal-4, and the wirings between LES are programmed by via-3 layer. All layers other than via-1 and via-3 are fixed structure, so the mask data of these layers are common for various VPEX products.

Figure 4 shows the circuit schematic and the layout of logic element (LE) used in VPEX. The layout rule is 0.18 \( \mu \)m CMOS technology. Single LE consists of complex-gate-type EXclusive-OR (EXOR) gate and inverter (NOT). We divide EXOR gate into AOI and NOR gate in order to create various logic functions. These three gates are connected each other by selecting some of 40 via-1 holes which are illustrated in Fig. 4(b). Multiple holes within 5 \( \mu \)m area
can be exposed by a single “CP mask” as we mentioned in Sect. 2.2. Dashed-rectangles in the layout indicate “CP mask” area, therefore each logic function can be defined by two EB shots.

The programmable logic functions are 12 kinds; NOT, BUF, all 2-inputs logic functions (NAND, NOR, AND, OR, bubble AND, bubble OR, EXOR, EXNOR) and two 3-inputs functions (AOI21 and MUXI), as illustrated in Fig. 5. The gate delay is 1–3 stages depending upon logic functions. For example, the NAND gate has 1-stage delay, and the EXNOR gate has 3-stage delay.

The number of required “CP mask” for implementing 12 logic functions is calculated as follows. The layout of 9 vias in the left side can be programmed by 5 “CP mask,” because there are common layout for 12 logic functions. The input/output signals to/from VPEX LE are transferred to metal-3 (M3) layer above EXOR area. If the via-1 pattern layout on EXOR area is changed, input/output M3 wire assignment can be changed as shown in Fig. 6. We prepared two via-1 patterns at each logic function to increase the flexibility in the wiring. Therefore, the layout of 31 vias in the right side is prepared by 24 for 12 logic functions. Considering the vertically-flipped layout of the logic-element, the total number of “CP mask” patterns are 58 (= (5 + 24) x 2). This value is smaller than the maximum “character” patterns, which is 100 as shown in the EB direct writing machine specification [8].

3.2 The Comparison with Other Logic Element

LUT and SOP (Sum-Of-Product) are popular logic-programmable circuits which have been used in FPGA or PLD. The performance of VPEX logic elements is evaluated by comparing 2-input LUT and 2-input SOP as shown in Fig. 7.

The table below Fig. 7 shows the number of transistors and the logic gate delay. The logic element of VPEX has 12 transistors, and the gate delay is 1–3, which indicates the smallest area and the highest speed in these 4 logic elements. In order to clarify the advantage of VPEX logic element, the area, the gate delay and the power consumption are evaluated as shown in Fig. 8. The area is estimated by drawing the layout of LUT-1, LUT-2, SOP, and VPEX LE circuit. The wiring area is omitted in this test.
layout. The delay-time and the power-consumption are simulated by the HSPICE from Synopsys. We simulate EXOR, EXNOR, NAND, NOR, AND, and OR cells, and the average of all data were taken. VPEX performance is better than any other via-programmable devices. Especially, the power-consumption of VPEX LE is remarkably lower than other LEs. It is because that the operated gate capacitance is small in VPEX LE.

4. Cell Libraries Composed of Several LEs

4.1 D-FlipFlop Composed of 5 LEs

We described about the combination logic of VPEX in Sect. 3. In order to compose sequential-logic circuit such as a counter or a state machine, D-FlipFlops are required. In the most case of previous programmable-logic study, D-FlipFlops are prepared in addition to logic element. In general, the ratio of the number of D-FlipFlops to the number of combination logics depends upon the characteristics of a circuit. Then it was reported that many D-FlipFlops were wasted in the standard FPGA and the via-programmable logic [5] whose ratio is fixed. In the VPEX architecture, Scan D-FlipFlop with Reset (SDFFR) is configured by 5 LEs, as shown in Fig. 9. Each area surrounded by broken-line indicates one LE. Therefore, the ratio of SDFFRs/LEs can be changed according to circuit characteristics. Consequently, there is no waste of LEs and D-FlipFlops in VPEX at any circuits as same as the standard-cell based ASICs.

Table 1 shows the electrical characteristic of SDFFR. The setup and hold time of SDFFR on VPEX are almost same as that of standard cells (SCs). However, delay time is about 1.6 times larger than that of SCs. This is because, the SDFFR in SCs uses the transmission gate (TG).

4.2 Full-Adder Composed of 4 LEs

A Full Adder (FA) is frequently used in mathematical calculation circuit such as an adder or a multiplier. Therefore, we decided to register FA to VPEX library and try to reduce area and delay time. FA is configured by 4 LEs whose circuit is fixed as shown in Fig. 10. The critical path of FA in multi-bit adder is Cout from Cin. This gate delay is 2-stages, which is equal to the critical path delay in FA of Standard-cells as shown in Fig. 11. The delay of 4-bit adder composed of VPEX is compared to that of Standard cells shown in Table 2. These results indicate that the FA of VPEX can achieve speed performance comparable to the FA used in standard-cells implementations.
5. Routing Architecture of VPEX

5.1 Local Routing Architecture

The main routing layers are metal-3 (M3) and metal-4 (M4) in VPEX architecture. The wire structures are illustrated in Fig. 12.

The signal flow between M3 to M4 is connected by via-3 switch placed at the cross and end points. The layout of one logic element (LE) is composed of two area (NOT and EXOR area) as shown in Fig. 4. The M3 and M4 wires above NOT area and EXOR area are placed orthogonally. The input/output ports are extracted from M3 on EXOR area as shown in Fig. 6. A signal is transferred to horizontal direction by connecting M3 line above NOT area and M4 line above EXOR area, alternately. This structure is called as a “jumper structure” [12]. Additional vertical and horizontal lines named bridge wire (BW) are arranged at LE boundary for long distance wiring. BW is extended to 4 LE lengths and placed as a staggered placement.

Clock (CLK) lines and Reset lines are routed using metal-5 (M5) wires. Clock signal and Reset signal are transferred to M4 islands as shown in Fig. 12. When the LE is used as a Scan D-FlipFlop with Reset, M4 islands are connected to CLK and Reset signal wire through via-3.

5.2 Experimental Local Routing Tools

In order to evaluate the local routing resources and the circuit performance of VPEX, the experimental routing tool is developed. Figure 13 shows the VPEX design flow for digital ASIC. In the first step, HDL description is synthesized by the “Design Compiler” supplied from Synopsys. The target library used in logic synthesis is composed of 14 gate functions (NOT, BUF, NAND, NOR, AND, OR, bubble AND, bubble OR, EXOR, EXNOR, AOI21, MUXI, FullAdder and Scan D-FlipFlop with Reset) customized for VPEX.

Placement & Route (P&R) and GDS pattern generation of via-1 and via-3 need original CAD tool specialized for VPEX. Post-layout timing verification will be carried out by using commercially available CAD tools such as “Star-RC” and “Primetime” by Synopsys.

There are many commercial P&R tools for ASIC in which the routing layer is all metals and vias. We cannot apply these tools for VPEX, because the routing has to be carried out by only via-3 layer. So the original P&R tools have to be developed. The mapping (logic assignment to LE) in the following sample circuits is carried out by the temporal placement tool to evaluate routing tool, in which the total wire length should be minimized. So, we will discuss our original routing tools hereafter.

The routing path is searched by Lee’s maze routing algorithm [13]. The grid size for path search is the pitch of metal wire shown in Fig. 12. Compared to the “jumper structure” wire, the bridge wire (BW) should be kept for long distance wiring. So we applied two step searches: the first step is “Adjacent cell routing,” and the second step is “Normal maze routing.” Furthermore, if routing is not completed using two step search, there are re-routing step which change the priority of routing as shown in Fig. 14.

In the first “Adjacent cell routing” step, the shortest path between adjacent cells is searched without using BW, as shown in Fig. 15(a). This method is effective to reduce parasitic resistance and capacitance. In this first step, some
un-routed connections may be remained. In the second “Normal maze routing” step, the routing path of remained connection between adjacent cells and other connections, are searched using Lee’s maze routing algorism, as shown in Fig. 15(b). The maze method finds out routes including a detour, however, some connections may not route due to the pre-routed wiring resource. In this case, the un-routed connection is given a priority order. If the routing is failed by this priority procedure, we have to get back to the placement procedure, however, the routing was successfully finished for sample circuit in this algorithm. The results will be shown in the next section.

5.3 The Evaluation of Routing Resources

At first, the test P&R area composed of 256 LEs is prepared. The small sample circuits are mapped and routed by the experimental tools. The successful mapping results are demonstrated as shown in Table 3. The utilization is defined as the number of used LEs divided by the total number of LEs (= 256). Figure 16 shows the wire layout at the most congested part of 5 bit × 5 bit multiplier (utilization: 68%). Thick line is used wire and white circle is via-3. The two kinds of routing sample are high-lighted. The wire from A to B is routed with “Adjacent cell routing” method, and the wire from C to D is routed with “Normal maze routing” method. The experimental results show that the local wire resources and the performance of experimental wiring tool seem to be enough to configure small size practical circuits.

5.4 The Prospect of Global Architecture

The global architecture of VPEX will be changed according to the number of metal wiring. In this section, we will introduce the preliminary architecture for 5-metals process, as illustrated in Fig. 17.

In order to realize large circuit using VPEX, the buffering of clock signal and long-wire signal will be needed periodically. So, the Logic Array Block (LAB) which contains hundreds of LEs, are adopted in order to place the buffers and long distance wires between LABs. These wires are named as “bus wires,” and M3 and M4 metals between LABs are used. These “bus wires” can be connected to external inputs and outputs pins. M5 wires are used as power lines (VDD, GND) and clock (CLK) and Reset lines. The detail of global architecture will be studied in the future work.

6. Circuit Performance Evaluation of VPEX

In this section, the circuit performance of VPEX is compared to ASICs using full-set standard cells at the point of area, delay and power. The ASIC circuit is designed with 0.18 µm rule and the P&R was carried out by “Silicon Ensemble” from Cadence. The delay performance and dynamic power-consumption were calculated using HSPICE simulation by Synopsys. The input of multiplier and the clock of counter are operated at 100 MHz. Dynamic power-consumption was defined by average power of all input patterns. The result is shown in Table 4. The static power-consumption of VPEX is much smaller than that of FPGA, because there are no configuration SRAM cells.

mapped area of VPEX is about 4–5 times larger than that of ASIC. The delay and the power-consumption of VPEX are about 1.3–1.6 and 2–2.4 times larger than that.

Fig. 15 The schematic diagram of 2 step routing.

Table 3 Mapping example of VPEX using original P&R tools.

<table>
<thead>
<tr>
<th>modules</th>
<th>utilization</th>
<th>FF</th>
<th>cell</th>
<th>IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>A part of hammering decoder</td>
<td>54%</td>
<td>15</td>
<td>63</td>
<td>23</td>
</tr>
<tr>
<td>5×5 multiplier</td>
<td>68%</td>
<td>0</td>
<td>175</td>
<td>20</td>
</tr>
</tbody>
</table>

Fig. 16 Wire congestion in the center of 5 bit × 5 bit multiplier.

Fig. 17 The preliminary global architecture of VPEX for 5-metals.
of ASIC. The increased delay and power-consumption of VPEX are due to the large parasitic capacitance and resistance of metal wiring, because VPEX has a fixed metal structure which contains redundant wiring.

The performances of FPGA [1] are also written in Table 4 in comparison with ASIC and VPEX. The digital circuit developed by FPGA can be fabricated with 1/10 area, 1/3 delay and 1/5 power by using VPEX.

Table 4: The performance comparison between VPEX with ASIC.

<table>
<thead>
<tr>
<th>modules</th>
<th>Performance</th>
<th>ASIC</th>
<th>VPEX</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>4x4 multiplier</td>
<td>Speed</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>(μs/slow)</td>
<td>1.07</td>
<td>1.30</td>
<td>2.07</td>
</tr>
<tr>
<td></td>
<td>Power</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>(μs/slow)</td>
<td>1.30</td>
<td>1.28</td>
<td>1.96</td>
</tr>
<tr>
<td>decimal counter</td>
<td>Area</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>(100MHz)</td>
<td>Speed</td>
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<td>1.00</td>
<td>1.00</td>
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<tr>
<td></td>
<td>(μs/slow)</td>
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<td>2.37</td>
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<td></td>
<td>Power</td>
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</tr>
<tr>
<td></td>
<td>(μs/slow)</td>
<td>2.35</td>
<td>2.35</td>
<td>2.35</td>
</tr>
</tbody>
</table>

*FPGA performance is derived from reference [1].

7. Summary and Conclusion

In this paper, we proposed the novel architecture of via-programmable logic device named VPEX. The logic element (LE) of VPEX is composed of the combination of EXOR and NOT gates. The Single LE can output 12 logic functions including all 2-input logic functions.

The area, the speed and the power consumption of VPEX LE is compared to two 2-input Look Up Table (LUT) and 2-input Sum Of Product (SOP). The VPEX LE has the best performance among 4 LEs. Scan D-FlipFlop with Reset (SDFFR) can be composed of 5 LEs. It is suggested that the VPEX is free from waste D-FlipFlops due to the unbalance of D-FlipFlop and combination logic. The size of LE is as small as 88 μm² in 0.18 μm CMOS rule. The layout of via-1 is optimized for EB direct writing, so 1 LE can be delineated by double EB shot using 58 “CP mask.”

The wire routing between LEs is programmed by via-3 layer. The routing result with 68% cell utilization is successfully demonstrated in the 5 × 5 multiplier circuit using original routing tool. The area, speed and power consumption is evaluated in comparison with standard-cell based ASICs and FPGAs. The area, delay and power of VPEX are 4–5, 1.3–1.6 and 2–2.4 times larger than that of ASICs. On the other hand, the area, delay and power of VPEX is as small as 1/10, 1/3 and 1/5 times that of FPGA. These results suggest that the VPEX architecture with EB direct writing is the best solution for small-volume production LSI.

We will make proto-type chip with VPEX and will compare the performance of VPEX with that of ASIC and FPGA. In addition, the global routing architecture and CAD tool will be developed for implementing large practical circuits.

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References


Akihiro Nakamura received his B.E. degree in Ritsumeikan University, Shiga, Japan in 2006. He is now a master student of Ritsumeikan University. He has been engaged in research on “Place and Route” tools for via-programmable device named VPEX.
Masahide Kawarasaki received his B.E. degree in Ritsumeikan University, Shiga, Japan in 2007. He is now a master student of Ritsumeikan University. He has been engaged in research on the design of via-programmable device named VPEX.

Kouta Ishibashi received his B.E. degree in Ritsumeikan University, Shiga, Japan in 2007. He is now a master student of Ritsumeikan University. He has been engaged in research on "Place and Route" tools for reconfigurable logic device named ePLX.

Masaya Yoshikawa is an associate professor in the Department of Information Engineering at the Meijyo University, Nagoya, Japan. He received his Ph.D. degree from Ritsumeikan University, Japan, in 2001. His research interests include LSI design, artificial intelligence, and parallel processing.

Takeshi Fujino was born in Osaka, Japan, on March 17, 1962. He received B.E. and M.E., and Dr. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1984, 1986, and 1994, respectively. He joined the LSI Research and Development center, Mitsubishi Electric Corp. in 1986. Since then, he had been engaged in the development of electron beam lithography process, and embedded DRAM circuit design. In 2003, he moved to Ritsumeikan University, Shiga, Japan, and currently he is a professor of department of VLSI system design. His research interests include SoCs using programmable logic, and its’ applications for network system.